Very High Carrier Mobility for High-Performance CMOS on Si(110) surface

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Very High Carrier Mobility for High-Performance CMOS on a Si(110) Surface

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***Abstract*—In this paper, we demonstrate CMOS characteristics on a Si(110) surface using surface flattening processes and radical oxidation. A Si(110) surface is easily roughened by OH^- ions in the cleaning solution compared with a Si(100) surface. A flat Si(110) surface is realized by the combination of flattening processes, which include a high-temperature wet oxidation, a radical oxidation, and a five-step room-temperature cleaning as a pregate-oxidation cleaning, which does not employ an alkali solution. On the flat surface, the current drivability of a p-channel MOSFET on a Si(110) surface is three times larger than that on a Si(100) surface, and the current drivability of an n-channel MOSFET on a Si(110) surface can be improved compared with that without the flattening processes and alkali-free cleaning. The $1/f$ noise of the n-channel MOSFET and p-channel MOSFET on a flattened Si(110) surface is one order of magnitude less than that of a conventional n-channel MOSFET on a Si(100) surface. Thus, a high-speed and low-flicker-noise p-channel MOSFET can be realized on a flat Si(110) surface. Furthermore, a CMOS implementation in which the current drivabilities of the p-channel and n-channel MOSFETs are balanced can be realized (balanced CMOS). These advantages are very useful in analog/digital mixed-signal circuits.**

***Index Terms*—Channel, cleaning, CMOS, flicker, mobility, MOSFET, noise, roughness, surface orientation.**

I. Introduction

THE miniaturization of MOSFETs has been able to increase the level of integration and performance of large-scale-integrated (LSI) devices. However, miniaturization in the critical dimension of integrated circuits is accompanied by a decrease in the thickness of the gate insulator films of metal–oxide–semiconductor transistors. Recently, the leakage currents of MOSFETs have mainly been composed of a leakage current through the gate insulator films and a drain leakage current. Therefore, suppression of the leakage current in ultralarge-scale-integrated (ULSI) devices is one of the crucial technologies for the improvement of ULSI devices. Recently, there have been many reports on high-k dielectric films for the gate insulator [1]–[4]. At the same time, the improvement of the current drivability of MOSFETs without shrinkage of the device scale is a very important alternative technological approach for realizing an increase in LSI performance. Some efforts on increasing device performance such as the development of strained silicon [5]–[8] and Fin-FET [9]–[11] have been reported. However, it is difficult to suppress the leakage currents because of the bandgap narrowing that accompanies germanium incorporation or the local high electric field concentration at the corner edge. Recently, a technology based on a Si(110) surface has been reported [12]–[16]. It has been reported that the hole mobility in the channel on a Si(110) surface is largest compared with any other surface [17]. This means that, with this technology, it is possible to increase the current drivability without changing the material and the device structure. However, the current gate formation technology cannot form high-quality insulator films on all surface orientations except for the Si(100) surface. In contrast, we have reported that very-high-quality gate insulators are formed on any silicon surface by microwave-excited high-density plasma oxidation/nitridation, and very low $1/f$ noise MOSFETs are realized using this oxidation/nitridation technology [12], [18].

In this paper, we demonstrate that the low noise balanced CMOS fabricated on a very flat Si(110) surface by using the five-step room-temperature cleaning and microwave-excited high-density plasma oxidation presents very promising performances and may be very useful for analog/digital mixed-signal circuits.

II. Experimental

Dual-gate MOSFETs on Cz-Si(100) and Cz-Si(110) surfaces are employed for this experiment. Gate oxides (5 nm) are formed by microwave-excited high-density plasma oxidation (radical oxidation) at 400 °C after modified RCA cleaning [19]–[21] and five-step room-temperature cleaning (shown in Fig. 1 [22]). As^+ and BF_2^+ (4×10^{15} cm^{-2}) ions are implanted into the gate poly-Si (300 nm) and source/drain regions after the gate formation for n-channel MOSFET and p-channel MOSFET, respectively. After the formation of an aluminum interconnect, hydrogen sintering is applied at 400 °C in $N_2/H_2 =$ 9/1 ambient.

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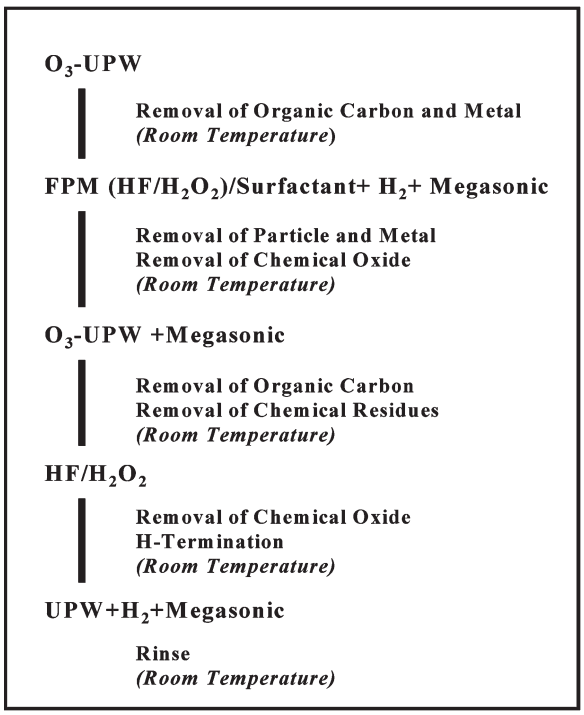

Fig. 1. Five-step room-temperature cleaning process. This cleaning method does not employ any alkali solution and does not etch the silicon surface [22].

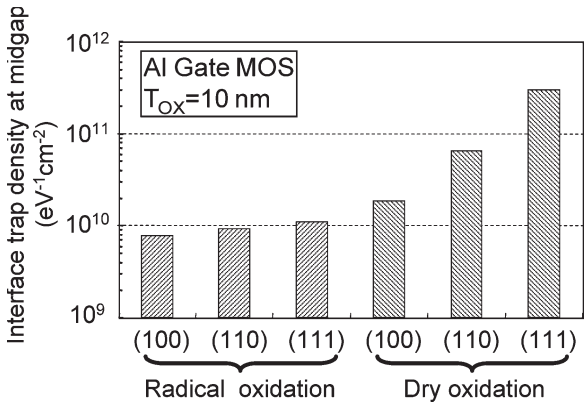

Fig. 2. Interface trap density at midgap of the SiO_2/Si interface formed by radical oxidation and thermal oxidation of Si(100), Si(110), and Si(111) surfaces.

The surface microroughnesses of the silicon surfaces is measured by vacuum scanning tunneling microscopy (STM) and atomic force microscopy (AFM) after the RCA and five-step room-temperature cleaning for evaluation of the surface flatness. The density of Si atoms dissolved in water is measured by inductively coupled plasma Auger electron spectroscopy after immersion in the water containing dissolved oxygen at various concentrations of 0 ppm (N_2 ambient), 8 ppm ($O_2/N_2 = 1/4$), and 32 ppm (O_2 ambient) and its correlation to the surface microroughness is evaluated.

III. Results and Discussions

We reported that the high-quality gate oxides can be formed by radical oxidation using microwave-excited high-density plasma [23], [24]. Fig. 2 shows the measured interface trap density at the Si/SiO_2 interface formed by radical oxidation (400 °C) and the conventional dry oxidation (900 °C) on Si(100)-, Si(110)-, and Si(111)-oriented surfaces [23], [24]. In this experiment, the interface trap density is evaluated by the quasi-static C–V method. It is well known that high-quality SiO_2 films and a Si/SiO_2 interface having a low interface trap density can be realized by thermal oxidation only on a Si(100) surface, as shown in Fig. 2. On the contrary, the results in Fig. 2 show that radical oxidation using microwave-excited high-density plasma can form the high-quality SiO_2 films and Si/SiO_2 interface having a low interface trap density on any of the three silicon surface orientations. In addition, it has been reported that this radical oxidation can form high-quality gate insulators even on a polycrystalline silicon surface [26]. These mean that every silicon surface can be applied in the LSI formation by using radical oxidation. In this experiment, the 5-nm gate oxides are employed. The interface trap density at the midgap of these 5-nm gate oxides is also about 1×10^{10} cm^{-2} eV^{-1}. Fig. 3 shows the drain current I_D–gate voltage V_G characteristics (drain voltage $V_D = -50$ mV) of p-channel MOSFETs whose gate oxides were formed by: (a) dry oxidation and (b) radical oxidation. In the case of dry oxidation, threshold voltages differ between Si(100) and Si(110) owing to the Si/SiO_2 interface traps and the fixed charge in the gate oxide. However, no threshold voltage difference appears between the MOSFETs on Si(110) and Si(100) whose gate oxide was formed by radical oxidation. This indicates that radical oxidation can be adequately employed for gate oxide formation on Si(110) surfaces as regards the bulk and interfacial quality of oxide. One of the most crucial problems on the Si(100) surface, which is currently used for LSI fabrication, is the very low current drivability of p-channel MOSFETs. Improving the current drivability of p-channel MOSFETs is thus very important. Fig. 4 shows the I_D–V_D characteristics of p-channel MOSFETs on (a) Si(100) and (b) Si(110). The current drivability of a p-channel MOSFET on Si(110) is three times larger than that on Si(100). Fig. 5 shows the channel direction dependences of the drain currents of n-channel and p-channel MOSFETs formed on Si(110). The vertical axes are absolute currents and currents normalized by that of a p-channel MOSFET on Si(100). All currents of n-channel and p-channel MOSFETs on Si(110) are much larger than that of p-channel MOSFETs on Si(100). This suggests that the CMOS property on a Si(110) surface is improved compared

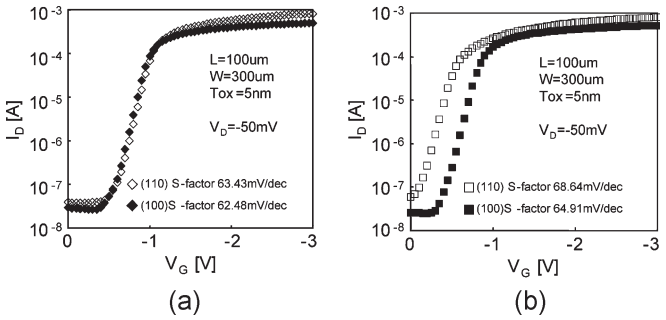

Fig. 3. I_D–V_G characteristics of p-channel MOSFETs. (a) The gate oxide was formed by dry oxidation. (b) The gate oxide was formed by radical oxidation.

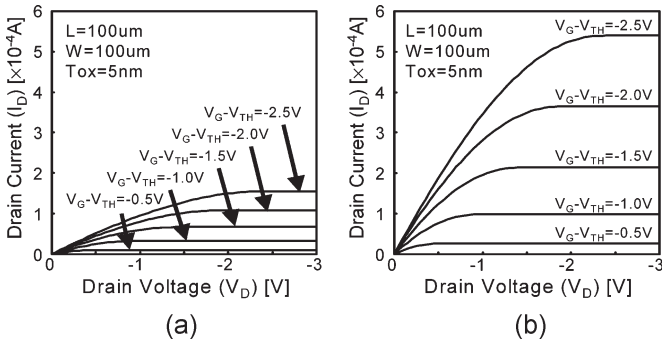

Fig. 4. I_D–V_D characteristics of p-channel MOSFETs on Si(100) and Si(110) surfaces.

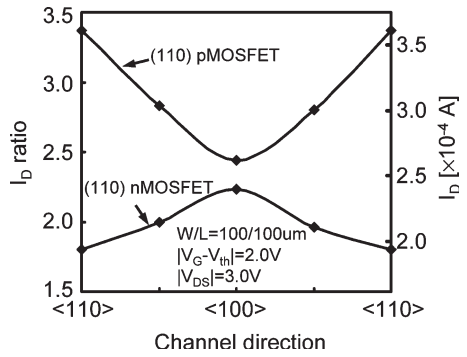

Fig. 5. Channel direction dependence on the drain current of n-channel MOSFETs and p-channel MOSFETs formed on Si(110). The vertical axes are absolute currents and currents normalized by that of p-channel MOSFET on Si(100).

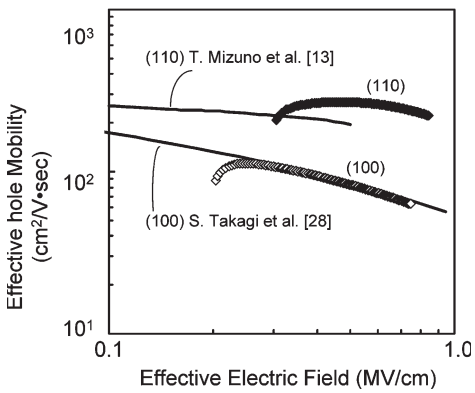

Fig. 6. Effective channel mobility $\mu_{\rm eff}$ in p-channel MOSFETs as a function of effective electric field $E_{\rm eff}$.

with that on a Si(100) surface. Unlike the drain currents on Si(100) that have a weak dependence on the channel direction [27], the drain currents on Si(110) have a strong dependence on the channel direction [17]. It should be noticed that the channel direction giving the maximum current of n-channel MOSFETs differs from that of p-channel MOSFETs by 90°. Then in the circuit design, the channel direction dependence of the drain current must be taken into account in the case of Si(110), unlike in Si(100). Fig. 6 shows the effective channel mobility $\mu_{\rm eff}$ as a function of the effective electric field $E_{\rm eff}$ in the p-channel MOSFET. $E_{\rm eff}$ is defined as $(Q_B + Q_i/\eta)/\varepsilon_{\rm si}$,

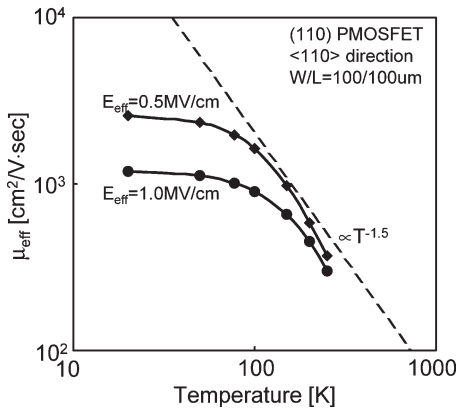

Fig. 7. Effective channel mobility $\mu_{\rm eff}$ as a function of the operating temperature T in the p-channel MOSFETs.

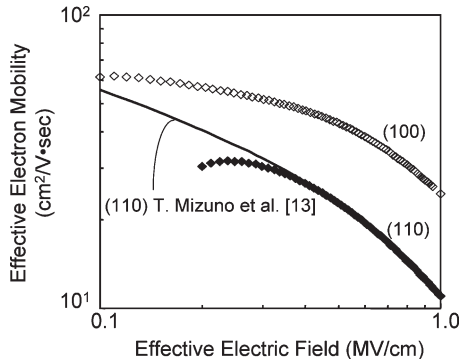

Fig. 8. Effective channel mobility $\mu_{\rm eff}$ in n-channel MOSFETs as a function of effective electric field $E_{\rm eff}$.

where the η of p-channel MOSFET is taken to be 3 [8], [28] and $\varepsilon_{\rm si}$ is the dielectric constant of silicon. As shown in Fig. 6, the $\mu_{\rm eff}$ of p-channel MOSFET on Si(100) is the same as the universal hole mobility [29]. The $\mu_{\rm eff}$ of p-channel MOSFET on Si(110) is much larger than that on Si(100) and is also larger than the value of $\mu_{\rm eff}$ on Si(110) previously reported [8]. It is considered that this enhancement of the $\mu_{\rm eff}$ of p-channel MOSFET is due to the high-quality oxides and Si/SiO_2 interface realized using radical oxidation. Fig. 7 shows $\mu_{\rm eff}$ as a function of the operating temperature T in the p-channel MOSFETs. In the region of temperature higher than 100 K, the effective hole mobility in the channel is proportional to $T^{-1.5}$ on Si(110), which means that the effective hole mobility is limited by phonon scattering. In addition, the $E_{\rm eff} - \mu_{\rm eff}$ characteristics of the n-channel MOSFETs are shown in Fig. 8. Unlike the case of p-channel MOSFETs, the $\mu_{\rm eff}$ value of n-channel MOSFET on Si(110) is the same as the reported $\mu_{\rm eff}$ on Si(110) [8] and is less than that on Si(100). Fig. 9(a) and (b) shows $\mu_{\rm eff}$ as a function of the operating temperature in the n-channel MOSFETs. The temperature dependence of $\mu_{\rm eff}$ is very small in the low-temperature region, as shown in Fig. 9(b), and the $E_{\rm eff}$ dependence of $\mu_{\rm eff}$ is high in the high-field region. In the relatively high electric field region, $\mu_{\rm eff}$ is defined as follows [28]:

$$\mu_{\rm eff}^{-1} = \mu_{\rm ph}^{-1} + \mu_{\rm SR}^{-1} \tag{1}$$

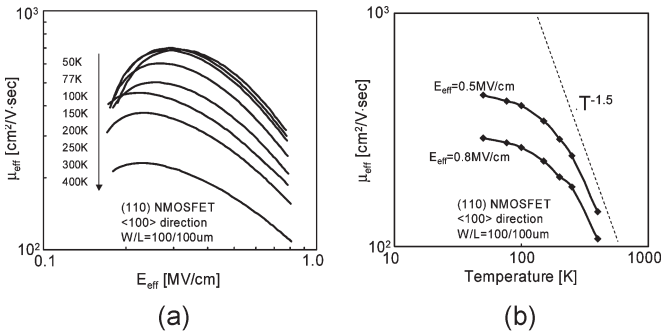

Fig. 9. Effective channel mobility $\mu_{\rm eff}$ as a function of (a) effective electric field $E_{\rm eff}$ and (b) operating temperature in the n-channel MOSFETs.

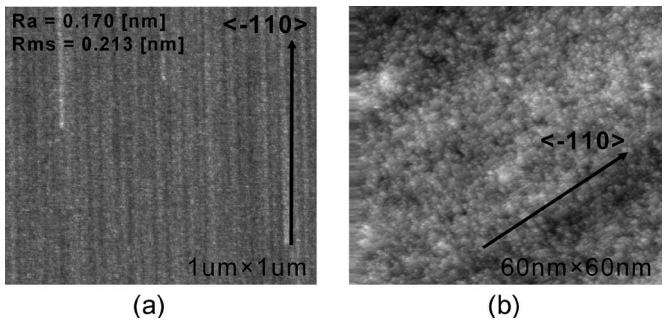

Fig. 10. (a) AFM and (b) STM images of the Si(110) surface after UPW final rinsing in RCA cleaning and diluted HF treatment.

where $\mu_{\rm ph}$ and $\mu_{\rm SR}$ are the mobilities limited by phonon scattering and surface roughness scattering, respectively. When the electron mobility is limited, the acoustic phonon scattering $\mu_{\rm eff}$ is proportional to $T^{-1.5}$. In the relatively high-temperature region, $\mu_{\rm eff}$ is not proportional to $T^{-1.5}$ in Fig. 9(b). This means that the electron mobility of n-channel MOSFETs on Si(110) is not limited by phonon scattering but by interface microroughness scattering. These results lead us to realize the importance of microroughness suppression. Fig. 10 shows (a) AFM and (b) STM images of the Si(110) surface after ultrapure water (UPW) rinsing following RCA cleaning and diluted hydrogen fluoride (HF) treatment. The lines indicating the $\langle -110\rangle$ direction on the Si(110) surface can be observed. This means that the etching on Si(110) occurs along the $\langle -110\rangle$ direction, which is oriented to Si(111) surface. Fig. 11 shows the average surface microroughness (Ra) and the density of silicon atoms dissolved in the water after immersion in UPW containing dissolved oxygen at various concentrations of 0 ppm (N_2 ambient), 8 ppm ($O_2/N_2 = 1/4$), and 32 ppm (O_2 ambient). The Ra values and the density of dissolved silicon atoms of the Si(110) surface are much larger than those of the Si(100) surface even after immersion in UPW. It is considered that an etching process that occurs on the silicon surface owing to OH^- ions in water causes the surface microroughness, and a Si(110) surface is much more sensitive to this effect than a Si(100) surface. This indicates that the surface microroughness on a Si(110) surface is caused by alkali solution ($NH_4OH/H_2O_2/H_2O = 0.05/1/5$) in RCA cleaning [20], [21] and causes the degradation of channel mobility in n-channel MOSFET. This implies that the technology used to suppress the generation of surface microroughness on

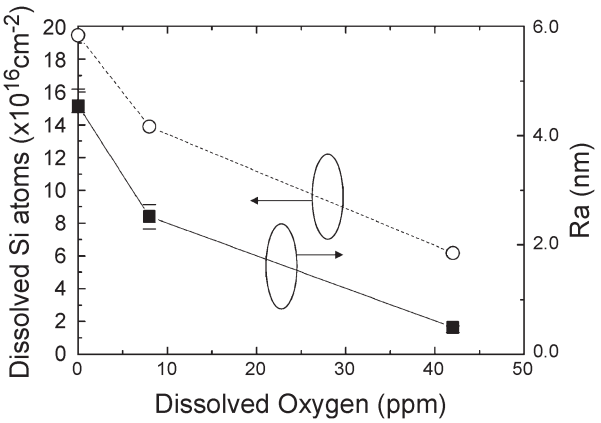

Fig. 11. Average surface microroughness (Ra) and the density of dissolved silicon atoms in water after immersion in water containing dissolved oxygen at various concentrations of 0 ppm (N_2 ambient), 8 ppm ($O_2/N_2 = 1/4$), and 32 ppm (O_2 ambient).

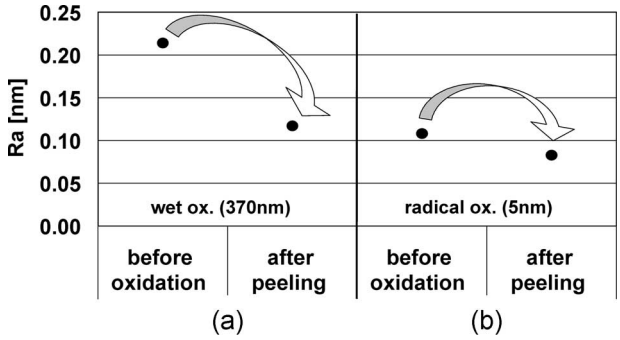

Fig. 12. Ra improvement for the Si(110) surface by wet oxidation at 1000 °C and radical oxidation.

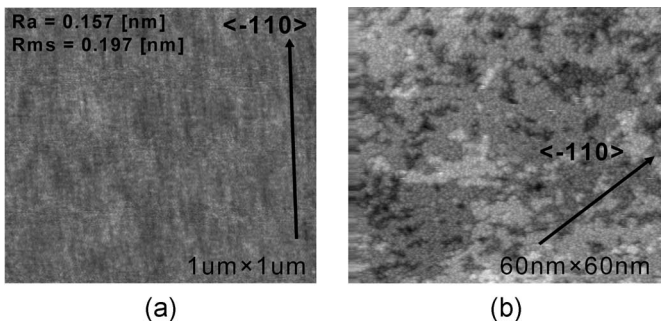

Fig. 13. (a) AFM and (b) STM images of the Si(110) surface after H_2-UPW + megasonic rinsing in five-step cleaning process after wet oxidation and radical oxidation.

Si(110) is much more important than that on Si(100). Fig. 12 shows the improvement of the Ra of a Si(110) surface brought by about wet oxidation at 1000 °C and radical oxidation at 400 °C. Both methods are isotropic oxidations of the silicon surface; as a result, the silicon surfaces are flattened by these oxidations. Fig. 13 shows (a) AFM and (b) STM images of the Si(110) surface after H_2-UPW + megasonic rinsing, which is part of the five-step cleaning process (shown in Fig. 1 [22]) employed in pregate-oxidation cleaning. Wide terraces are observed in the STM image. This means that the flat

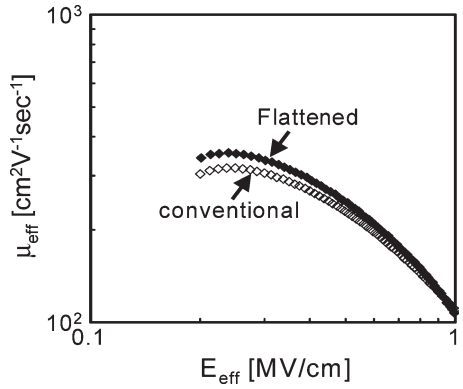

Fig. 14. $\mu_{\rm eff}$–$E_{\rm eff}$ characteristics of n-channel MOSFETs having a conventional and Si/SiO_2 flattened interfaces.

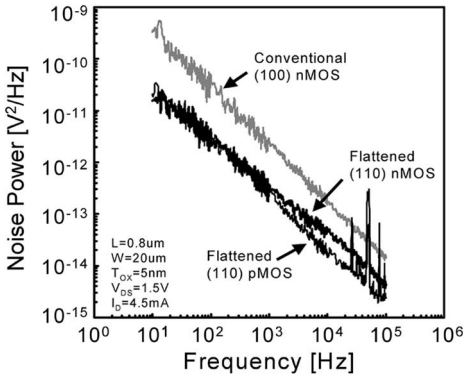

Fig. 15. Noise power as a function of frequency f. The noise power is proportional to $1/f$. The $1/f$ noise of p-channel MOSFET on Si(110) is one order of magnitude smaller, although its current drivability is the same as that of n-channel MOSFET on Si(100).

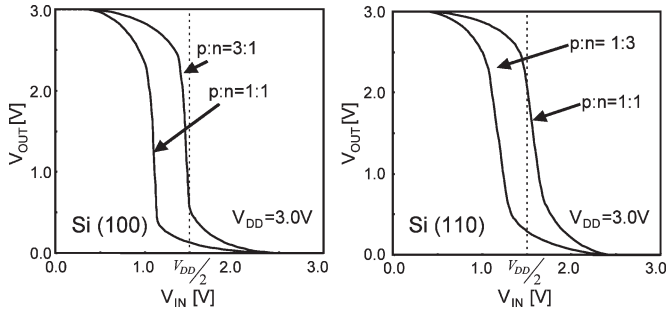

Fig. 16. Simulated $V_{\rm in}$–$V_{\rm out}$ characteristics of the CMOS inverter on Si(100) and Si(110) for various gate width ratios of p-channel MOSFET/n-channel MOSFET (p/n = 3/1, 1/1).

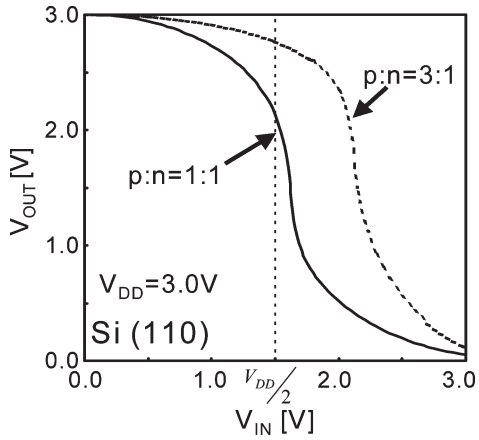

Fig. 17. Measured $V_{\rm in}$–$V_{\rm out}$ characteristics of the CMOS inverter on Si(110) for different gate width ratios of p-channel MOSFET to n-channel MOSFET (p/n = 1/1, 3/1).

surface in atomic order is realized by the flattening processes of high-temperature wet oxidation and radical oxidation, and the advanced cleaning process, which does not employ any alkali solution and does not etch the silicon surface. Fig. 14 shows the $\mu_{\rm eff}$–$E_{\rm eff}$ characteristics of n-channel MOSFETs having conventional and Si/SiO_2 flattened interfaces. The $\mu_{\rm eff}$ value can be improved by flattening the Si/SiO_2 interface. This means that trap charge reduction is realized by the surface flattening process. Fig. 15 shows the noise power as a function of frequency (f). The noise power is proportional to $1/f$. The $1/f$ noise of p-channel MOSFET on Si(110) is one order of magnitude smaller than that of n-channel MOSFET on Si(100), although current drivabilities are almost the same. We have reported that the $1/f$ noise can be reduced by a combination of surface flattening and radical oxidation [30]. These results support that the flattening processes and five-step room-temperature cleaning enable the realization of a very flat surface on Si(110).

Fig. 16(a) and (b) shows the simulated $V_{\rm in}$–$V_{\rm out}$ characteristics of the CMOS inverter on unbalanced CMOS, which is the same as the inverter on Si(100), and balanced CMOS, in which the current drivabilities of p-channel MOSFET and n-channel MOSFET are the same for various gate width ratios of p-channel MOSFET/n-channel MOSFET = 3/1, 1/1, 1/3. The inverter operates at $V_{DD}/2$ for p/n ratio = 1/1 and 3/1 on the balanced CMOS and unbalanced CMOS [Si(100)], respectively. On Si(100), the current drivability of n-channel MOSFET is about three times larger than that of p-channel MOSFET. The currents of both n-MOSFET and p-channel MOSFET are the same when the gate width of p-channel MOSFET is three times larger than that of n-channel MOSFET; as a result, the CMOS-on-Si(100) inverter operates at $V_{DD}/2$ for p/n ratio = 3/1. When the current drivabilities of n-channel MOSFET and p-channel MOSFET are the same, channel width adjustment is not needed. Fig. 16(b) shows that the balanced CMOS inverter operates at $V_{DD}/2$ for p/n ratio = 1/1. Fig. 17 shows the measured $V_{\rm in}$–$V_{\rm out}$ characteristics of the CMOS inverter on Si(110) for different gate width ratios of p-channel MOSFET to n-channel MOSFET (p/n = 1/1, 3/1). The CMOS inverter with p/n ratio = 1/1 begins to operate at almost $V_{DD}/2$. This indicates that the balanced CMOS is realized on a Si(110) surface. When the current drivabilities of a p-channel MOSFET and an n-channel MOSFET are balanced, the offset of output voltage in the analog switch can be reduced and a NOR circuit can be easily used for logic devices compared with the Si(100) unbalanced CMOS [25]. These results indicate that these MOSFETs fabricated on Si(110) can be applied not only to digital circuits but also to analog, RF, and mixed-signal circuits.

IV. Conclusion

We demonstrated CMOS characteristics on a Si(110) surface by using a surface flattening process, which involves a five-step room-temperature cleaning process and radical gate oxidation. By fabricating a device on a Si(110) surface, the characteristics of p-channel MOSFET on Si(110) are superior to those on Si(100), although the current drivability of n-channel MOSFETs fabricated on Si(110) is less than that on Si(100). It is noticed that the circuit layout must take into account the fact that the drain currents have a strong dependence on the channel direction and that channel direction giving the maximum current to n-channel MOSFETs differs from that giving the maximum current to p-channel MOSFETs by 90° [17]. The current drivability of n-channel MOSFET on Si(110) can be improved by the suppression of the surface microroughness by the flattening processes with high-temperature wet oxidation and radical oxidation and an advanced cleaning process, which does not employ any alkali solution and does not etch the silicon surface. Then, a balanced CMOS in which the current drivabilities of both n-channel and p-channel MOSFETs are balanced is realized on Si(110).

Furthermore, low $1/f$ noise in n-channel and p-channel MOSFETs can be realized by a combination of surface microroughness flattening and radical gate oxidation. These results indicate that these MOSFETs that are fabricated on Si(110) can be applied not only to digital circuits but also to analog, RF, and mixed-signal circuits.

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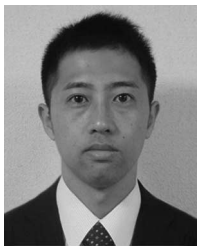

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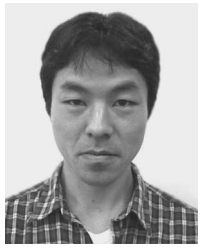

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