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Effects of N Distribution on Charge Trapping and TDDB Characteristics of N_2O Annealed Wet Oxide

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***Abstract*— Wet pyrogenic oxide of different thicknesses was annealed in N_2O ambient and the N concentration in the films was studied by using SIMS (Secondary ion mass spectroscopy). It was found that for a certain annealing time and temperature, the N concentration (at %) increases with decreasing the wet oxide thickness and the location of the peak of N is observed near the interface of nitrided oxide and Si substrate. On the contrary, after nitridation the concentration of H is higher in the thicker wet oxide of thickness 100 Å and also does not change much from the surface to the interface. For the thinner wet oxide of thickness 40 Å, the concentration of H is less and decreases toward the interface.**

Gate dielectrics were characterized using high-frequency and quasi-static measurements. After a constant current stress, a large distortion was observed for the N_2O annealed wet oxide of 98 Å whereas for the N_2O annealed wet oxide of 51 Å the distortion was small. With increasing stressing time, hole trap is followed by electron trapping for the wet oxide of 98 Å whereas for the N_2O annealed wet oxide of 51 Å, hole trapping increases a little at the beginning and then saturates. From the TDDB characteristics, a longer t_{BD} was observed for N_2O annealed wet oxide of 51 Å compared to 98 Å. From the experimental results, it can be suggested that the improved reliability of thin gate oxide is due to the large amount of N concentration near the interface only. Hence for the device fabrication process, if the wet oxide is nitrided in N_2O ambient, the reliability of gate oxide will be improved in the ultrathin region.

***Index Terms*— Hydrogen and nitrogen distribution, MOS capacitor, nitrided oxide, P- and N-MOSFET, SIMS, wet oxide.**

I. INTRODUCTION

THE role of nitrogen in ultrathin gate dielectrics is an important factor for deep submicron devices. It has been shown that the presence of nitrogen at the interface of nitrided oxide improves wear out properties with respect to Fowler–Nordheim and substrate hot carrier injections [1]–[3]. As a result, a great attention has been paid on nitrided oxide gate dielectrics to replace conventional SiO_2 grown in oxygen [4]–[13]. For nitridation of thin oxide, generally three processes are used: namely, NH_3 nitridation, N_2O and NO nitridation.

In the NH_3 nitridation process, a thermal oxide is grown and then nitrided in an NH_3 ambient. NH_3-nitrided oxides display improved properties compared to SiO_2 [10], [11] due to nitrogen incorporation in the dielectric close to the Si/SiO_2 interface. However, NH_3 nitridation incorporates hydrogen in the oxides which can reduce the reliability of the oxides [13]. Reoxidation of this film is required to reduce the hydrogen concentration [13]. Recently, N_2O-grown and N_2O-modified oxides have been investigated [5], [6]–[9], [12]. These oxides have demonstrated higher reliability and improved electrical characteristics; however these have insufficient nitrogen at the dielectric and silicon interface. To have sufficient nitrogen concentration to effectively suppress boron penetration [14] a much higher thermal budget is required in N_2O-based oxides.

Also, NO nitridation is used to nitride oxide. It has been shown that a much lower thermal budget is required for an NO process than an N_2O process to produce an oxynitride with useful properties. Actually, it is still controversial which is best between the N_2O and NO nitridation processes because the location of nitrogen in the oxide determines the reliability. If the nitrogen exists at the interface as well as in the bulk, it degrades the charge-to-breakdown characteristics [15].

In this study, we have studied wet oxide thickness dependence of nitrogen concentration and also effects of nitrogen distribution profiles on charge trapping and TDDB behavior were studied. It will be shown that with decreasing wet oxide thickness, for the same temperature and time, nitrogen concentration increases near the interface. By N_2O annealing, the electrical characteristics also improve with the decrease of wet oxide thickness.

II. EXPERIMENTAL

MOS capacitors and transistors were fabricated on p-type (100) orientation Si substrates with resistivity 10–20 $\Omega\cdot$ cm. In our study, all wafers were cleaned with standard RCA cleaning process, followed by an HF dip (1% diluted HF solution) to remove the native oxide and a rinse in de-ionized water. N- and P-well were formed for MOS capacitors and P- and N-channel transistors, respectively. After that, the active regions were defined by the conventional local oxidation of silicon (LOCOS) and channel doping was carried out using sacrificed oxide. Immediately before gate oxidation, the sacrificial oxide was etched away to remove the undesirable defects. Thin gate oxides with thickness ranging from 45 to 92 Å were grown at 750 °C by pyrogenic wet oxidation using the reaction of H_2 and O_2 to create H_2O. At the time of oxidation, the ratio of oxygen and hydrogen flow rates at atmospheric pressure was $1 : 1.8$. For nitridation, oxide films were annealed in 100% N_2O ambient for 5 min at 1000 °C. *In situ* phosphorous-doped

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polysilicon gate electrodes were deposited at 620 °C using CVD of PH_3 and SiH_4 for both n- and p-type capacitors and transistors. The thickness of doped polysilicon was 2000 Å and phosphorous concentration was 6×10^{20} cm^{-3}. After that gate electrodes were defined by photo lithography. The thickness of the gate oxide was determined by capacitance–voltage ($C-V$) measurement using dielectric constant of SiO_2 (3.85).

N- and P-MOSFET with nitrided wet oxide were also fabricated to study the reliability problems due to hot carrier effects. The fabrication process was same as for MOS capacitors up to the gate electrodes. After the gate electrode formation, n-LDD and p-LDD were formed by phosphorous and boron implantation, respectively. Sidewall spacers were processed using 1500 Å thickness TEOS. For n-channel transistors, source and drain were formed by Arsenic ion implantation and for p-channel transistors source and drain were formed by $B + BF_2$ ion implantation. Annealing was done at 850 °C to activate and distribute the implanted ion. A passivation layer was then deposited and contact holes were opened for connection. An aluminum layer was deposited and patterned. Finally, all the samples were sintered at 400 °C for 20 min in an H_2 ambient to form good ohmic contact. The experimental set-up used to test and stress the devices consisted of an HP4145B semiconductor parameter analyzer. During constant current stress for both polarities, the capacitors were in the accumulation mode.

To investigate the dependence of N distribution profile on wet oxide thickness, three different thicknesses of wet oxide were grown with the same process conditions as MOS capacitors except the N_2O annealing temperature was 900 °C and the nitridation time 10 and 30 min. Though the nitridation temperature is different from that used for the MOS capacitor, the purpose of studying the N distribution profiles is to observe the trend on how they vary on wet oxide thickness. The distribution of N profile was measured by a Evans-East SIMS systems.The depth of the interface of SiO_2 and Si is taken as that depth at which the O intensity drops to half the value of that in the flat part of its profile in the oxide. In this case, the actual thickness will differ from the value which is determined from the O intensity because the penetration of the primary ion beam into the sample was approximately 20 Å. Wet oxide thickness dependence of N_2O annealing conditions for SIMS samples and N at % at peak point after N_2O annealing are given in Table I.

TABLE I
Wet Oxide Thickness Dependence of N_2O Annealing Conditions for SIMS Samples and N at % at Peak Points Due to N_2O Annealing at 900 °C for 10 and 30 min

Sample No.	Initial wet oxide thickness(Å)	N2O annealing temp.and time of initial wet oxide	Final thickness after N2O annealing(Å)	N at % at peak points
CV-48	40	900°C , 10 min	61	0.70
CV-49	71	900°C , 10 min	89	0.57
S-3	101	900°C , 10 min	108	0.30
CV-50	40	900°C , 30 min	71	1.40
CV-47	71	900°C , 30 min	99	1.24
S-4	101	900°C , 30 min	118	0.76

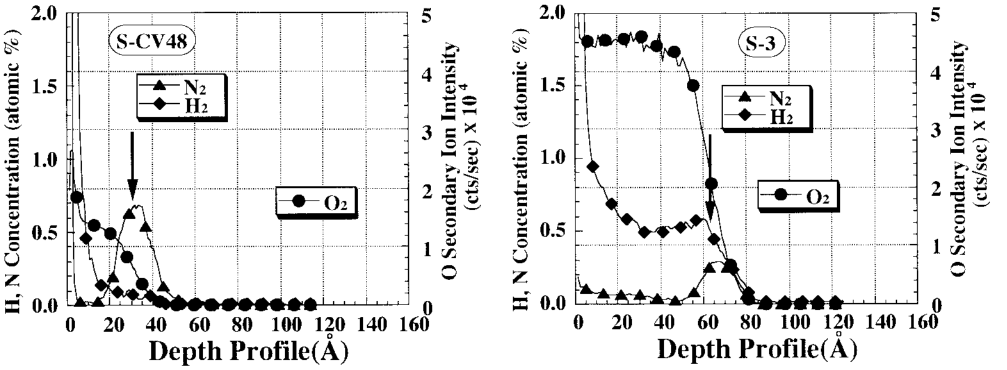
III. Results and Discussion

A. SIMS Analysis

Wet oxide thickness dependence of hydrogen and nitrogen depth profiles and concentrations after N_2O annealing was analyzed by SIMS. Fig. 1(a) and (b) shows the nitrogen and hydrogen profiles obtained in N_2O annealed wet oxide of initial nominal thicknesses of (a) 40 Å and (b) 100 Å, respectively. The measured thicknesses were 61 and 108 Å. The annealing time was 10 min and annealing temperature 900 °C. The nitrogen peak is observed near the interface in each sample but the maximum N concentration was observed for the N_2O annealed wet oxide of 61 Å and least was observed for the N_2O annealed wet oxide of 108 Å. It was observed that when the wet oxide thickness of 40 Å annealed in N_2O for 10 min, the N concentration near the interface was 0.70 at % whereas the value of N concentration was 0.30 at % in the 100 Å wet oxide. Also, when the wet oxide was annealed for 30 min in N_2O ambient, the N concentration was 1.4 and 0.7 at % for the wet oxide of 40 and 100 Å thicknesses, respectively (Table I). Also, the H concentration in at % is shown in Fig. 1(a) and (b). It is observed that H concentration was very less in wet oxide of thickness 40 Å whereas in wet oxide of 100 Å, the hydrogen concentration was distributed uniformly throughout the films. From the SIMS data, it is demonstrated that the N concentration increases with decrease of wet oxide thickness. On the other hand, H concentration decreases with decrease of wet oxide thickness. So to have a reliable gate dielectric for the ultra large scale integration, an oxide with less hydrogen which will suppress electron trapping as well as sufficient nitrogen at the interface which will replace the strained Si-O bond to Si-N, is necessary. In this study, we found that just by annealing wet oxide of 40 Å in N_2O got the required gate oxide with less hydrogen and more nitrogen compared to the wet oxide of thickness 100 Å. As the devices are scaled down to submicron level, the gate oxide thickness will also decrease. Hence nitridation of wet oxide in N_2O ambient will fulfill the desired requirements.

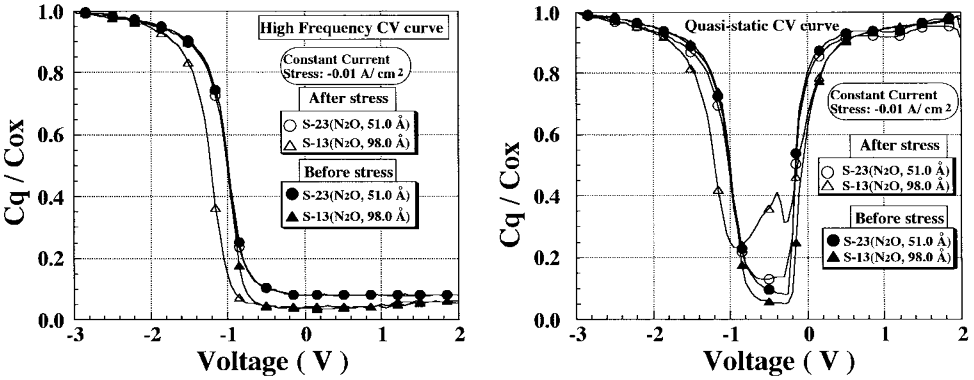
B. $C-V$ Characteristics

Fig. 2(a) and (b) shows the normalized high- and low-frequency quasi-static $C-V$ (QSCV) characteristics, respectively, before and after a constant current stress of -0.01 A/cm^2 for 100 s. The thicknesses of N_2O annealed wet oxide were 51 and 98 Å. The area of the capacitor was 0.01 mm^2 and during constant current stress, electrons were injected from the gate electrode to the Si substrate. Here, in Fig. 2(a) and (b), C_{ox} represents the maximum capacitance value when the capacitor was in accumulation mode and C_q represents the change of quasi-static capacitance with the change of gate voltage during measurements. Both for HFCV and QSCV measurements, the gate voltage was changed from



(a) (b)

Fig. 1. SIMS depth profiles of N_2O annealed wet oxide as a function of wet oxide thickness of (a) 40 Å and (c) 100 Å, respectively. The primary beam current was 25 nA and impact angle was 60°.



(a) (b)

Fig. 2. Normalized (a) high-frequency and (b) quasi-static $C-V$ characteristics of different thicknesses N_2O annealed wet oxide before and after the stress, respectively. The constant current stress was -0.01 A/cm^2.

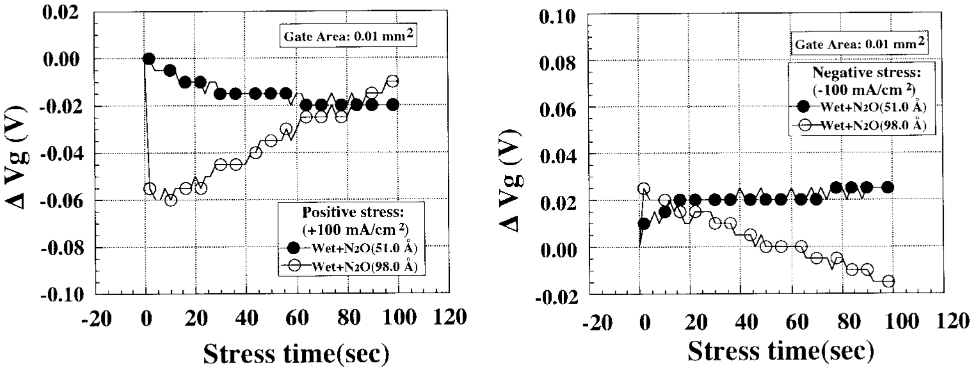
-3 to $+2$ V with a ramp rate of 0.05 V/s. The number of measured points were 101. In Fig. 2(a) before the stress, irrespective of wet oxide thickness, the HFCV curves do not vary. But after stress, the $C-V$ curves shifted to the negative direction with increasing thickness. Also, for QSCV before the stress [Fig. 2(b)] no distortion was observed with the variation of wet oxide thickness. But after the stress, a greater shift was observed in N_2O annealed wet oxide of thickness 98 Å and the least was observed in N_2O annealed wet oxide of 51 Å. The V_{fb} and N_{it} were calculated from the high- and low-frequency $C-V$ curves before and after the stress and are shown in Table II. It was observed that both the V_{ft} and N_{it} before the stress do not vary much with increasing thickness but after the stress compared to the N_2O annealed wet oxide of thickness 51 Å, the V_{fb} was shifted more to the negative direction as well as N_{it} increased for the N_2O annnealed wet oxide of thickness 98 Å. In case of N_2O annealed wet oxide of 51 Å, V_{fb} shifted to the negative and increased the N_{it} but both were small. As it was observed that in N_2O annealed wet oxide of 61 Å [Fig. 1(a)], the N concentration at the peak was more compared to the N_2O annealed wet oxide of 108 Å for the same N_2O annealing conditions, the improved V_{fb} and N_{it} for the N_2O annealed wet oxide of 51 Å may be due to sufficient nitrogen incorporation at the interface which acts as a barrier for generation of fixed oxide charge in the interface.

TABLE II
THE VALUE OF V_{fb} AND N_{it} (CALCULATED FROM THE $C-V$ MEASUREMENTS) BEFORE AND AFTER STRESS FOR TWO DIFFERENT THICKNESSES N_2O ANNEALED WET OXIDE

N_2O annealed wet oxide thickness(Å)	Vfb (Before stress)	Vfb (After stress)	Nit (Before stress)	Nit (After stress)
51	-0.9334	-0.9458	1.930×10^{9}	5.534×10^{10}
98	-0.9467	-1.2211	1.754×10^{10}	9.076×10^{11}

C. Charge Trapping Characteristics

A constant-current stressing method is used to investigate the high field charge trapping behavior of gate dielectrics of MOS capacitors with N_2O annealed wet oxide layers. In this method, a fixed constant current is forced through the N_2O annealed wet oxide using an 4145B semiconductor parameter analyzer. The voltage drop V across the dielectric is simultaneously monitored. It is known that an increase or a decrease in the absolute value of V indicates electrons or holes trappping, respectively, in the dielectrics [16]. Fig. 3(a)



(a) (b)

Fig. 3. Charge trapping characteristics of N_2O annealed wet oxide for (a) positive and (b) negative bias stress, respectively, as a function of stress time.

and (b) shows the charge trapping behavior of N_2O annealed wet oxide of different thicknesses under substrate and gate injection, respectively. The stress current density was 100 mA/cm^2 and stress time was 100 s. In Fig. 3(a) for +100 mA/cm^2 stress to the gate in the accumulation mode, ΔV_g of N_2O annealed wet oxide of 98 Å abruptly decreases at the initial stage of the stress, and increases thereafter. This indicates that hole trapping is followed by electron trapping. In N_2O annealed wet oxide of 51 Å, first decreases a little but immediately saturates. This finding strongly suggests that decreasing of hole trapping in the N_2O annealed wet oxide of 51 Å is due to the larger nitrogen incorporation in the thinner oxide films compared to thicker oxide of 98 Å. For gate electron injection, the shifting of ΔV_g for 51 Å N_2O annealed wet oxide sample is the same as positive bias stress whereas for N_2O annealed wet oxide of 98 Å, hole trapping is followed by rapid increase of electron trapping.

D. TDDB Characteristics

The TDDB characteristics under positive bias to the gate are shown in Fig. 4 for two different thicknesses N_2O annealed wet oxide. The constant current stress was +0.01 A/cm^2 and the used gate area for TDDB measurements was 0.1 mm^2. The time to 50% breakdown was calculated from the Fig. 4 (not shown) and was observed that the time-to-breakdown t_{BD} was a bit longer for the N_2O annealed wet oxide of 51 Å compared to the N_2O annealed wet oxide of 98 Å. Here, the lifetime shows increasing trend with decreasing N_2O annealed wet oxide thickness just like others [4]. From the charge trapping characteristics, it is known that the larger the rate at which hole or electron will be trapped in the oxide, the more rapid will be the breakdown. As the N_2O annealed wet oxide of 51 Å has the less hole trapping, for the same stress it should give longer time to breakdown and was happened. Also, it can be said that due to the larger N concentration in N_2O annealed wet oxide of 51 Å compared to the 98 Å oxide causes to lifetime to increase; possibly, due to the presence of fewer broken Si-O bonds resulting from a higher degree of strain relief due to more N incorporation [17], [18]. From the C–V, charge trapping, and the TDDB characteristics, it can be inferred that nitridation increases the reliability of gate dielectrics. It is understood from the experimental results that if wet oxide is annealed in N_2O ambient for sufficient nitrogen incorporation, even the gate oxide deposited at low temperature (at 750 °C), the reliability will not be degraded with decreasing thickness which is desirable for the future submicron devices.

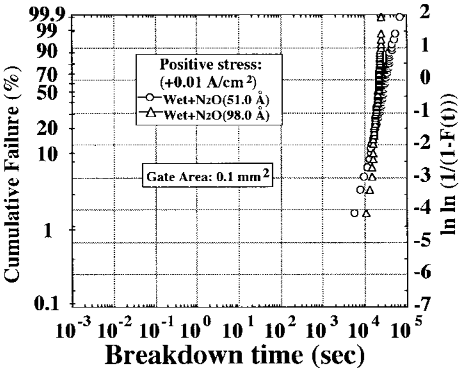
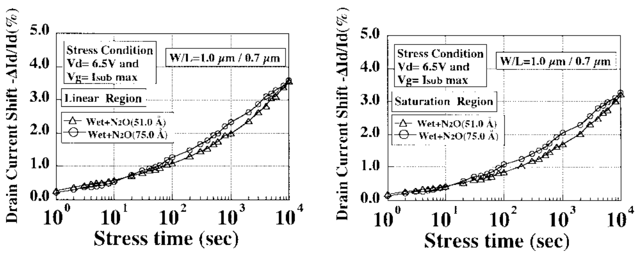


Fig. 4. Weibull plots of TDDB characteristics for two different thicknesses N_2O annealed wet oxide.



(a) (b)

Fig. 5. Degradation of the (a) linear drain currents (measured at $V_g = 1.65$ V and $V_d = 0.1$ V) and (b) saturation drain currents (measured at $V_g = 1.65$ V and $V_d = 3.3$ V), respectively as a function of stress time. The stress was done at $V_d = 6.5$ V and V_g at which $I_{\rm sub}$ was maximum.

E. Hot-Carrier Reliability

N-channel MOSFET's with two different gate oxide thicknesses were selected for hot carrier degradation tests. The gate oxide thicknesses were 51 and 75 Å and the channel length and width were 0.7 and 1.0 μm, respectively. The drain current was measured in the linear and the saturation region while gate voltage was 1.65 V. Fig. 5(a) and (b) shows the drain current shift of the n-MOSFET with N_2O annealed wet oxide of two different thicknesses. It was observed that for the same stress conditions, the drain current shift was small in n-MOSFET with N_2O annealed wet oxide of 51 Å compared to the N_2O annealed wet oxide of 75 Å. It is known that devices with nitrided gate dielectrics exhibit enhanced interface resistance against stress degradation due to the incorporation of interfacial nitrogen. As a reason, it is explained that nitrogen incorporation introduces a Si-N bonds (Si-N ~4.6 eV) [13], [19] in the interface and relaxes interfacial strained Si-O bonds [20]. In our experiments, from the SIMS results it was observed that N_2O annealed wet oxide of 61 Å has a higher N concentration than the N_2O annealed wet oxide of 108 Å for the same N_2O annealing conditions. Hence, the lower degradation of N_2O annealed oxide of 51 Å (Fig. 5) could be due to the higher amount of N incorporation which resists the generation of interface states and improves the transistor lifetime compared to the N_2O annealed wet oxide of 75 Å.

IV. CONCLUSIONS

Wet oxide thicknesses in the range of 40–100 Å were annealed in N_2O ambient and their physical and electrical characteristics were obtained. From the experimental results the following points can be concluded.

1) N concentration (at. %) depends on the wet oxide thickness i.e., with decreasing the wet oxide thickness from 100 to 40 Å, the N concentration increases from 0.3 to 0.7 at. % in the interface which was desired for the improvement of device reliability in the ultrathin region.
2) Due to the higher amount of N concentration in the interface of thin N_2O annealed wet oxide of thickness 51 Å, the ΔV_g was shifted less compared to the thick oxide of thickness 98 Å.
3) Also for the same reason, a longer t_{BD} was observed for the thin N_2O annealed wet oxide. Hence in the ultrathin region, N_2O annealing with appropiate temperature and time is necessary for the future device fabrication process.

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