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Improvement of Gate Oxide Reliability for Tantalum-Gate MOS Devices Using Xenon Plasma Sputtering Technology

Takeo Ushiki, *Student Member, IEEE,* Kunihiro Kawai, Mo-Chiun Yu, Toshikuni Shinohara, Kazuhide Ino, *Member, IEEE,* Mizuho Morita, *Member, IEEE,* and Tadahiro Ohmi, *Member, IEEE*

Abstract— **The effects of ion species in sputtering deposition process on gate oxide reliability have been experimentally investigated. The use of xenon (Xe) plasma instead of argon (Ar) plasma in tantalum (Ta) film sputtering deposition for gate electrode formation makes it possible to improve the gate oxide reliability. The Xe plasma process exhibits 1.5 times higher breakdown field and five times higher 50%-charge-to-breakdown ($Q_{\rm BD}$). In the Ta sputtering deposition process on gate oxide, the physical bombardment of energetic inert-gas ion causes to generate hole trap sites in gate oxide, resulting in the lower gate oxide reliability. The simplified model providing a better understanding of the empirical relation between the gate oxide damage and the inert-gas ion bombardment energy in gate-Ta sputtering deposition process is also presented.**

I. Introduction

WITH shrinking CMOS device dimension to deep-submicron range, advanced gate technology has become a paramount important concern. It has been widely studied that the dual-gate CMOS technology (n^+ poly gate for NMOS and p^+ poly gate for PMOS) is applicable to achieve low and symmetric threshold voltages ($V_{\rm th}$) for low voltage operation and salicide technologies provide low sheet resistance of gate electrode [1], [2]. For the dual-gate CMOS process, the scaling of thin gate oxide in VLSI technologies makes it difficult to suppress gate dopant (boron) penetration which causes $V_{\rm th}$ instability, degradation of gate oxide reliability and degradation of current drivability by polysilicon gate depletion [3], [4]. Several approaches have been studied to reduce the boron penetration by using of polysilicon microstructure effects [5] or nitridation effects of the gate oxide [6], [7]. In our understanding, all these methods increase the process complexity and cost, and thus it makes more and more difficult for semiconductor industry to continuously provide the new ULSI products to the marketplace for short turn-around-time (TAT).

In the course of searching for a new gate material which could take more important roles than the silicon-gate in terms of both performance and manufacturability, researchers at Tohoku University developed a process for synthesizing Ta films [8], [9] based on the Ultraclean Processing Concept [10], [11]. We found that Ta-gate MOSFET's exhibit excellent threshold voltage ($V_{\rm th}$)) adjustment for 1 V power supply voltage in both NMOS and PMOS by controlling the work function of the gate material (*Work Function Engineering*) [12], [13]. Moreover, we also found that Ta-gate electrode can achieve the required low sheet resistance below 0.2-μm line-width [8], [9]. The good chemical stability allows the process compatibility with the already-established Si-gate technology in respect of wet-chemical cleaning treatment. Other properties of Ta-gate, such as its X-ray absorbability and its high resistance to copper diffusion, also make it attractive as a gate material.

Concerning Ta film formation process, we have employed sputtering deposition method with low energy (<100 eV) inert-gas ion irradiation since it offers advantages in terms of low-temperature [14]. The process temperature for Ta-gate MOS fabrication must be 700°C or lower to suppress the thermal reaction between Ta-gate electrode and gate oxide [8], [9]. It is impossible for thermal chemical vapor deposition (CVD) process to deposit thin-Ta film on gate oxide at the temperature of 700°C or lower. The sputtering deposition method, in addition, makes it possible to precisely and simply control the crystallographic and electrical properties of Ta thin films grown on SiO_2 [15]. In previous work, however, the intrinsic breakdown field for Ta-gate MOS capacitors is relatively low compared to that for conventional *in-situ* phosphorus doped polycrystalline silicon (P-doped poly-Si) gate MOS capacitors in which the gate material was deposited by LPCVD [9]. In the case of sputtering deposition process, the gate oxide exposed to plasma is directory bombarded by energetic particles, including ions, electrons and photons, potentially causing damage to the gate oxide. From the standpoint of the yield and the reliability of real products, gate-metal sputtering deposition technology for lower plasma-induced gate oxide damage is

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T. Ushiki, K. Kawai, T. Shinohara, and K. Ino are with the Department of Electronic Engineering, Graduate School of Engineering, Tohoku University, Sendai 980-8579, Japan (e-mail: ushiki@sse.ecei.tohoku.ac.jp).

M.-C. Yu was with the Department of Electronic Engineering, Graduate School of Engineering, Tohoku University, Sendai 980-8579, Japan. He is now with Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan, R.O.C.

M. Morita was with the Department of Electronic Engineering, Graduate School of Engineering, Tohoku University, Sendai 980-8579, Japan. He is now with the Department of Precision Science and Technology, Graduate School of Engineering, Osaka University, Suita 565, Japan.

T. Ohmi is with the New Industry Creation Hatchery Center (NICHe), Tohoku University, Sendai 980-8579, Japan.

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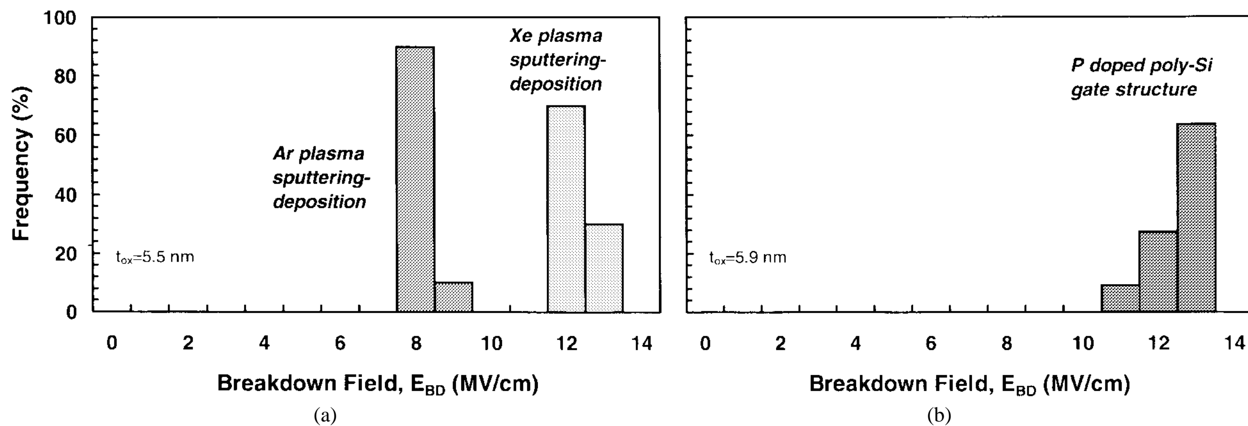

Fig. 1. Breakdown field histograms of (a) Ta-gate MOS capacitors for Xe plasma sputtering deposition or Ar plasma sputtering deposition and (b) P doped poly-Si gate MOS capacitors. Ta was deposited under the identical key parameters as the ion bombardment energy of 20 eV, the normalized ion flux of 13, the film growth rate of 20 nm/min at room temperature.

strongly required. The purpose of this paper is to demonstrate for the first time that a gate-Ta sputtering deposition process featuring low-energy (<100 eV) xenon (Xe) ion bombardment improves gate oxide reliability. We also describe the simplified model which provide a better understandings of the plasma-induced gate oxide damage dependence on the inert-gas ion species in sputtering deposition process.

II. Experimental

The samples used in this study were MOS capacitors and transistors on n-type 8–12 Ωcm (100) CZ silicon wafers and p-type 0.4–0.6 Ω·cm, respectively. The gate oxide was grown in dry oxygen after modified RCA-cleaning treatment [16] and hot-H_2O_2 chemical oxide formation [17], which results in no roughening of SiO_2/Si interface. The Ta sputtering deposition on gate oxide was carried out by using the dual-rf excitation plasma processing equipment which makes it possible to individually control the key parameters in the sputtering film deposition process, i.e., the film growth rate, the ion bombardment energy, the ion flux density, and the substrate temperature [18]. The ion bombardment energy, defined as the kinetic energy of individual bombarding ions incident on the substrate surface, was determined by the potential difference between the time-averaged plasma potential and the substrate potential. The time-averaged plasma potential was accurately measured by the advanced rf plasma probing method [19]. The ion flux density provided to the wafer was determined from the measurements of the saturation ion current on a negatively biased substrate. This plasma processing equipment was constructed based on the philosophy of ultraclean technology [10], [11], i.e., the oil-free ultra-high vacuum exhaust system and the ultraclean gas delivery system were employed. So, this has enabled us to form Ta films in an ambient with minimal disturbances of impurities. In this study, to clarify the effects of inert-gas ion species on gate oxide reliability in the sputtering deposition process, Ta films were deposited under the identical key parameters. The gate material for control samples was *in-situ* P-doped poly-Si which was deposited by LPCVD. The single source/drain junctions with low reverse-bias current was formed by using low-temperature post-implantation annealing technology [20], resulting in no thermal reaction between Ta-gate electrode and gate oxide [8], [9]. The sheet resistance and the junction depth of the source/drain region was 156 Ω/sq. and 60 nm, respectively. The samples were finally annealed in a hydrogen atmosphere at 400 °C for 30 min. The important point to note is that all etching process for pattern definition was performed by wet-chemical etching. Consequently, there was no cause of plasma-induced damage in samples other than Ta sputtering deposition process.

III. Results and Discussion

A. Effect of Physical Ion-Bombardment on Gate Oxide Reliability

Fig. 1 compares the breakdown field ($E_{\rm BD}$) histograms of MOS capacitors with Ar plasma sputtering-deposited Ta-gate electrode, Xe plasma sputtering-deposited Ta-gate electrode, and LPCVD P-doped poly-Si gate electrode. Ta was deposited under the identical key parameters as the ion bombardment energy of 20 eV, the normalized ion flux (= ion flux/Ta flux) of 13, the film growth rate of 20 nm/min and at room temperature. Fig. 1(a) shows that the breakdown events of Xe plasma sputtering-deposited Ta-gate MOS capacitors concentrate at the breakdown field of 12 MV/cm, which is 1.5 times higher than those of Ar plasma sputtering-deposited Ta-gate MOS capacitors. In terms of the breakdown field, the use of Xe plasma instead of Ar plasma in Ta-gate film sputtering deposition process can be attained to such gate oxide integrity as conventional P-doped poly-Si gate MOS structure, as shown in Fig. 1.

Fig. 2 shows the comparison of the time-dependent dielectric breakdown (TDDB) characteristics for 10.2-nm-thick gate oxide MOS capacitors. TDDB behavior was investigated under the constant current of 0.1 A/cm^2 by applying positive voltages to the gate electrode, where an accumulation layer was formed at the silicon surface. The result of our experiment clearly shows that Ta-gate MOS capacitors for Xe plasma sputtering deposition exhibit five times higher 50% cumulative failures charge-to-breakdown ($Q_{\rm BD}$) than those for Ar plasma sputtering deposition. Moreover, Xe plasma sputtering deposition can suppress the initial random failure.

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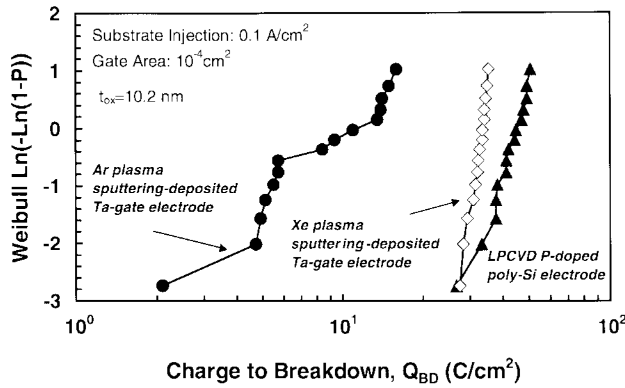

Fig. 2. Comparison of TDDB characteristics of MOS capacitors with Xe plasma sputtering-deposited Ta-gate electrode, Ar plasma sputtering-deposited Ta-gate electrode, and LPCVD P-doped poly-Si gate electrode. The gate oxide thickness is 10.2 nm.

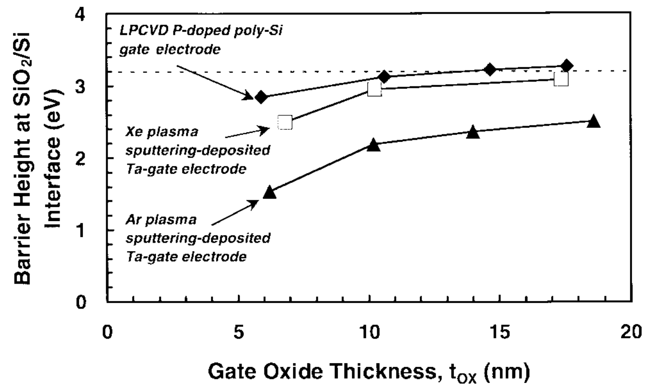

Fig. 4. Barrier height at SiO_2/Si interface as a function of gate oxide thickness. The barrier height was determined from Fowler–Nordheim current region of J-V characteristics.

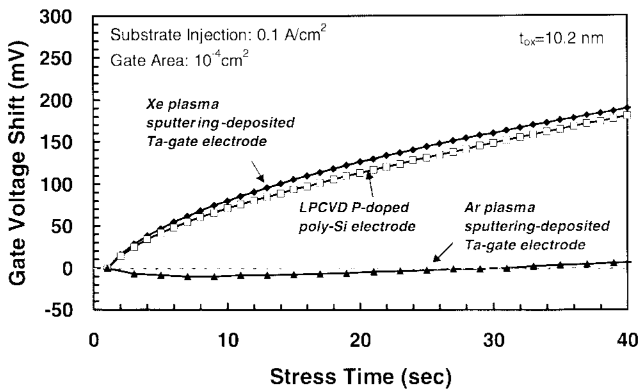

Fig. 3. Gate voltage shift of MOS capacitors with 10.2-nm-thick gate oxide as a function of stress time under the constant substrate-injected current of 0.1 A/cm^2.

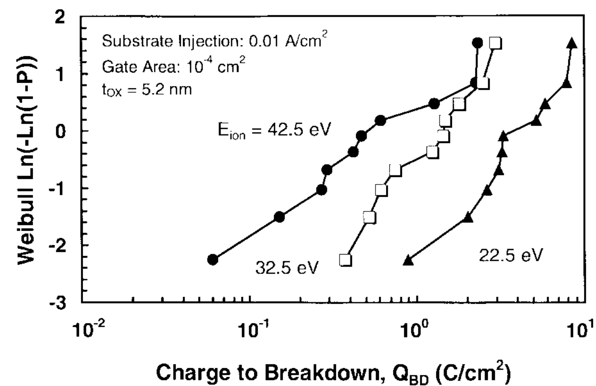

Fig. 5. Comparison of TDDB characteristics of Ta-gate MOS capacitors for various ion bombardment energy in Xe plasma sputtering deposition process. The normalized ion flux and the film growth rate are 14 and 20 nm/min, respectively. The gate oxide thickness is 5.2 nm.

The TDDB characteristics for Xe plasma sputtering-deposited Ta-gate is similar to those for LPCVD P-doped poly-Si gate. Fig. 3 shows the gate voltage shift of MOS capacitors with 10.2-nm-thick gate oxide as a function of stress time under the constant substrate-injected current of 0.1 A/cm^2. There is a slight negative gate voltage shift for Ar plasma sputtering deposition, whereas there are positive gate voltage shifts for both Xe plasma sputtering deposition and LPCVD. Since the flat-band voltage ($V_{\rm FB}$) for Ar plasma sputtering-deposited Ta-gate MOS capacitors before the stress is the same as that for Xe plasma sputtering-deposited Ta-gate MOS capacitors, there is no difference of the initial fixed charge density ($N_{\rm fc}$) of the gate oxide between both MOS capacitors [21]. Therefore, it is obvious that Ar plasma sputtering-deposited Ta-gate MOS capacitors have more hole trap sites in gate oxide than the others under process-finished condition. During TDDB stressing, the generated holes are trapped within the hole trap sites of gate oxide. More trapped holes increase the cathode field, which in turn causes a slight negative gate voltage shift phenomenon under the constant current stressing.

Fig. 4 shows the barrier height at SiO_2/Si interface as a function of gate oxide thickness. The barrier height is determined from the Fowler–Nordheim (FN) current region of gate current density-gate voltage (J-V) characteristics. The J-V characteristics was investigated by applying positive voltages to the gate electrode in which an accumulation layer was formed at the silicon surface. It can be seen from this data that the barrier height at SiO_2/Si interface slightly decreases as gate oxide thickness decreases. Our interpretation is that this degradation is mainly due to a distortion of the electric field in gate oxide with increased proportion of SiO_2/Si-interface-microroughness to gate oxide thickness. This data also demonstrate that Ar plasma sputtering-deposited Ta-gate MOS capacitors show much lower barrier height than the others. This fact indicates that Ar plasma sputtering-deposited Ta-gate MOS capacitors have more hole trap sites in gate oxide than the others. Since holes trapped in hole trap sites during J-V measurement enhance the internal electric field in gate oxide, the injected electrons have high probability of tunneling completely through the gate oxide. Therefore, it can be concluded that the more hole trap sites in gate oxide cause the lower effective barrier height for electron tunneling, the lower breakdown field, as shown in Figs. 4 and 1, respectively.

To clarify the influence of the physical bombardment of energetic inert-gas ion on gate oxide characteristics, TDDB characteristics was measured on Ta-gate MOS capacitors for various ion bombardment energy in Xe plasma sputtering-deposition process, as shown in Fig. 5. The normalized ion flux and the film growth rate are 14 and 20 nm/min, respectively. It can be seen that the higher energy ion bombardment in gate-

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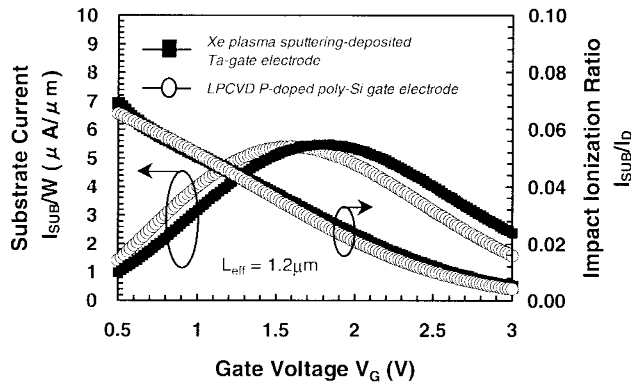

Fig. 6. Substrate current $(I_{\rm SUB})$ and impact ionization ratio $(I_{\rm SUB}/I_D)$ as a function of gate bias at the drain voltage of 5.0 V for n-channel MOSFET with Xe plasma sputtering-deposited Ta-gate electrode or LPCVD P-doped poly-Si gate electrode. The effective channel length and the gate oxide thickness is 1.2 μm and 5.4 nm, respectively.

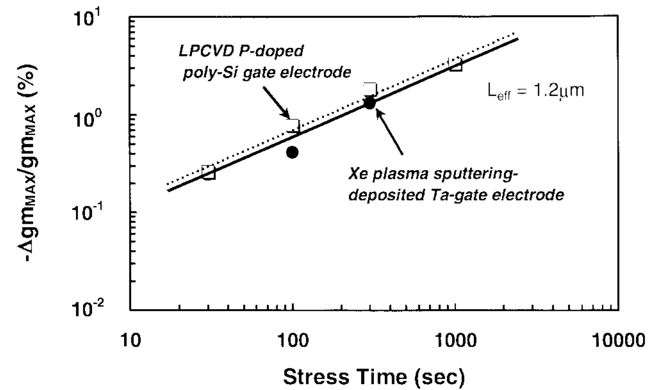

Fig. 7. Stress time dependence of maximum transconductance $(g_{m\rm MAX})$ degradation for n-channel MOSFET with Xe plasma sputtering-deposited Ta-gate electrode or LPCVD P-doped poly-Si gate electrode. Both devices were stressed at the drain voltage of 5.0 V and gate bias adjusted to generate peak substrate current. The gate oxide thickness is 5.4 nm.

metal sputtering deposition process causes the lower charge-to-breakdown characteristics. This fact clearly demonstrates that the plasma-induced gate oxide damage in the gate-metal sputtering deposition process is mainly due to the physical bombardment of energetic ion.

B. Hot Carrier Reliability

In this section the validity of Xe plasma sputtering process described in the previous section is examined experimentally from the standpoint of hot carrier reliability. The substrate current $(I_{\rm SUB})$ and the impact ionization ratio $(I_{\rm SUB}/I_D)$ as a function of the gate bias (V_G) at the drain voltage of 5 V for n-channel MOSFET with LPCVD P-doped poly-Si gate electrode and Xe plasma sputtering deposited Ta-gate electrode are shown in Fig. 6. The gate oxide thickness is 5.4 nm. The substrate current $(I_{\rm SUB})$ and the drain current (I_D) were measured on the MOSFET's with relatively long effective channel of 1.2 μm in order to eliminate parasitic effects as short channel behavior. The maximum value of substrate current $(I_{\rm SUB})$ for Xe plasma sputtering deposited Ta-gate MOSFET's is almost the same as that for conventional P-doped poly-Si gate MOSFET's. Moreover, both devices show the same impact ionization value under the $I_{\rm SUB}$ maximum conditions. The stress time dependence of the maximum transconductance (g_m) degradation for n-channel MOSFET with Xe plasma sputtering-deposited Ta-gate electrode or LPCVD P-doped poly-Si gate electrode is shown in Fig. 7. Hot-carrier stressing tests were performed on n-channel MOSFET's with 1.2 μm effective channel length. To compare Xe plasma sputtering-deposited Ta-gate MOSFET's with conventional P-doped poly-Si gate MOSFET's in terms of hot-carrier durability, both devices were stressed at the drain voltage of 5 V and the gate voltage adjusted to generate the maximum substrate current. The maximum transconductance (g_m) is measured at the drain voltage of 1 V. Both devices show the same immunity to hot-carrier-induced degradation under the same supply voltage. Fig. 8 compares the device lifetime as a function of the substrate current for n-channel MOSFET's with Xe plasma sputtering-deposited Ta-gate electrode or LPCVD P-doped poly-Si gate electrode. The device lifetime was defined as a static stressing time during which 10% maximum transconductance (g_m) degradation occurs. It is clearly seen that the both device lifetime for Xe plasma sputtering-deposited Ta-gate electrode and LPCVD P-doped poly-Si gate electrode is uniquely plotted on the line with the slope of -2.06. This suggests that the threshold energy for generating the interface state for Xe plasma sputtering-deposited Ta-gate MOSFET's is the same as that for conventional LPCVD P-doped poly-Si gate MOSFET's. Moreover, it is expected that both devices have 10 years lifetime under practical operational condition, i.e., $I_{\rm SUB} = 10^{-7}$ A/μm.

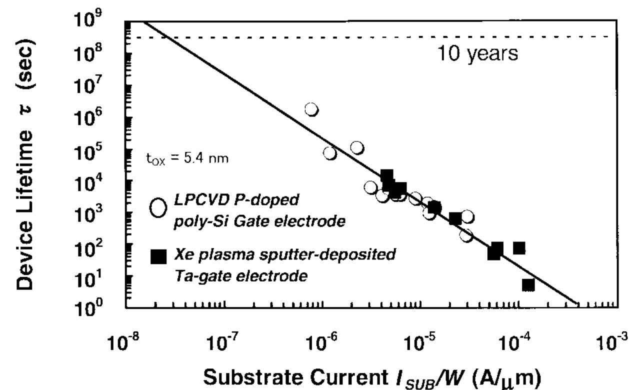

Fig. 8. Hot carrier lifetime plot for n-channel MOSFET with Xe plasma sputtering-deposited Ta-gate electrode or LPCVD P-doped poly-Si gate electrode. The gate oxide thickness is 5.4 nm. The device lifetime was defined as a static stressing time during which 10% maximum transconductance (g_m) degradation occurs.

C. Physical Plasma-Damage Model

The effects of the inert-gas ion species in gate-metal sputtering deposition process on gate oxide reliability can be interpreted as simple center-of-mass elastic collision of two isolated particles. According to the conservation of energy and momentum, the energy transfer efficiency η from impinging particle (Ar or Xe) to static atom (Si or O) can be written as

$$\eta = \frac{4\mu}{(\mu+1)^2}.$$

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Here, μ is the mass ratio of impinging particle to static atom. It is reasonable to suppose that the energetic bombardment of sputtered Ta particles can be neglected from this model, because the energy of the impinging Ta particles on gate oxide is negligible small. The impinging Ta particles on gate oxide is nearly neutrals, so that they cannot accelerate toward gate oxide in plasma sheath region. Moreover, the mean free path of the sputtered Ta particles under the operating gas pressure is much smaller than the substrate-target distance of this process chamber, so that there is little impingement of energetic Ta particle upon gate oxide. The mass ratio of Ar/Si is only $1.4\ (=39.9/28.1)$, but that of Xe/Si is $4.7\ (=131.3/28.1)$ [22]. While 97% of the bombarding energy is transferred from the Ar ion to the Si atom in a single collision, only 58% of the bombarding energy is transferred from Xe to Si. This suggests that Xe ion irradiation makes less oxide imperfection related to the loosely combined and/or broken Si–O bonds compared with Ar ion irradiation, resulting in less hole trap sites in gate oxide.

Although it is essential to reduce the ion bombardment energy on sputtering film deposition process in terms of reduction of the physical plasma damage to gate oxide, as indicated by Fig. 5, it has difficulty in making the ion bombardment energy reductive below the level of several electronvolts. On RF discharges, in most instances the electron temperature of plasma and the cyclic change of plasma potential set an inferior limit of the ion bombardment energy of approximately 20 eV. Therefore, it is proper to employ large-mass inert-gas in order to extend the acceptable region of the ion bombardment energy in gate-material sputtering deposition process.

IV. Conclusion

We have described that Xe plasma sputtering-deposited Ta-gate MOS capacitors show 1.5 times higher breakdown field and 5 times higher 50%-$Q_{\rm BD}$ compared with Ar plasma sputtering deposition. Moreover, the same immunity to hot-carrier-induced degradation as conventional LPCVD P-doped poly-Si gate MOSFET's can be completely realized at Xe plasma sputtering-deposited Ta-gate MOSFET's. In the gate-metal sputtering deposition process, the physical bombardment of energetic inert-gas ion causes to generate hole trap sites in gate oxide, resulting in the lower gate oxide reliability. We have also proposed the simplified model providing a better understanding of the empirical relation between the gate oxide reliability and the inert-gas ion bombardment energy in gate-metal sputtering deposition process. The sputtering deposition process using low-energy large-mass ion bombardment suites for low-temperature gate material formation in future high speed giga-scale-integration.

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Takeo Ushiki (S'96) was born in Niigata, Japan, on June 3, 1970. He received the B.S. and M.S. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1994 and 1996, respectively. He is currently pursuing the Ph.D. degree in electronic engineering at Tohoku University. His research focus is on high-performance SOI/CMOS device technology.

Mr. Ushiki is a member of the Institute of Electronics, Information, and Communication Engineers of Japan and a Research Fellow of the Japan Society for the Promotion of Science.

Kunihiro Kawai received the B.S. degree in electronic engineering from Tohoku University, Sendai, Japan, in 1997. He is currently pursuing the M.S. degree in electronic engineering at Tohoku University.

His current research interests are in SOI MOSFET's.

Mo-Chiun Yu was born in Hsinchu, Taiwan, R.O.C., on October 1, 1968. He received the B.S. degree in electrical engineering from National Tsing-Hua University, Hsinchu, in 1991, and the M.S. degree in electrical engineering from Tohoku University, Sendai, Japan, in 1997.

In 1997, he joined Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, where he has been engaged in research and development of semiconductor devices. His current research interests are in SOI device.

Toshikuni Shinohara was born in Kagoshima, Japan, on October 15, 1973. He received the B.S. and M.S. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1996 and 1998, respectively. He is currently pursuing the Ph.D. degree in electronic engineering at Tohoku University, where he is researching high-performance ULSI devices technologies.

Mr. Shinohara is a Research Fellow of the Japan Society for the Promotion of Science.

Kazuhide Ino (S'97–M'98) was born in Saitama, Japan, on March 31, 1970. He received the B.S., M.S., and Ph.D. degrees, in electronic engineering, from Tohoku University, Sendai, Japan, in 1992, 1995, and 1998, respectively. His doctoral thesis work involved the development of low-energy large-mass ion bombardment process for low-resistivity damage-free bcc-tantalum film growth, and the development of the source/drain junction formation technology with tantalum-silicide by low-temperature annealing below 550 °C, and their application to the fabrication of tantalum-gate SOI MOSFET's.

Currently, he is a Postdoctoral Fellow of the Japan Society for the Promotion of Science, Tohoku University.

Mizuho Morita (M'93) received the B.S. degree in electronic engineering from Hiroshima University, Hiroshima, Japan, in 1976, and the M.S. and Ph.D. degrees in electrical and communication engineering from Tohoku University, Sendai, Japan, in 1978 and 1981, respectively.

He then worked as a Postdoctoral Fellow at the Japan Society for the Promotion of Science. He was a Research Associate at Hiroshima University from 1982 to 1985. He was a Research Associate at Tohoku University from 1985 to 1991, and an Associate Professor from 1991 to 1997. He is presently a Professor in the Department of Precision Science and Technology, Graduate School of Engineering, Osaka University. His research is in the field of electron devices and microfabrication systems.

Dr. Morita is a member of the Japan Society of Applied Physics, the Institute of Electrical Engineers of Japan, the Institute of Electronics, Information and Communication Engineers, and the Japan Society for Precision Engineering.

Tadahiro Ohmi (M'81) was born in Tokyo, Japan, on January 10, 1939. He received the B.S., the M.S., and Ph.D. degrees in electrical engineering from Tokyo Institute of Technology, in 1961, 1963, and 1966, respectively.

Prior to 1972, he served as a Research Associate in the Department of Electronics of Tokyo Institute of Technology, where he worked on Gunn diodes such as velocity overshoot phenomena, multi-valley diffusion and frequency limitation of negative differential mobility due to an electron transfer in the multi-valleys, high-field transport in semiconductor such as unified theory of space-charge dynamics in negative differential mobility materials, Bloch-oscillation-induced, negative mobility and Bloch oscillators, and dynamics in injection layers. In 1972, he moved to Tohoku University and is presently a Professor at the New Industry Creation Hatchery Center (NICHe). He is currently engaged in researches on high-performance ULSI such as ultra-high-speed ULSI: current overshoot transistor LSI, HBT LSI, and SOI on metal substrate, base store image sensor (BASIS) and high-speed flat-panel display, and advanced semiconductor process technologies, i.e., ultra-clean technologies such as high-quality oxidation, high-quality metallization due to low kinetic energy particle bombardment, very-low-temperature Si epitaxy particle bombardment, crystallinity control film growth technologies from single-crystal, gain-size-controlled polysilicon and amorphous due to low kinetic energy particle bombardment, highly selective CDV, highly selective RIE, high-quality ion implantation with low-temperature annealing capability etc., based on the new concept supported by newly developed ultra-clean gas supply system, ultra-high vacuum-compatible reaction chamber with self-cleaning function, ultra-clean wafer surface cleaning technology, etc. He has published 700 original papers and has 600 patent applications.

Dr. Ohmi received the Ichimura Award in 1979, the Teshima Award in 1987, the Inoue Harushige Award in 1989, the Ichimura Prizes in Industry-Meritorious Achievement Prize in 1990, the Okouchi Memorial Technology Prize in 1991, the Minister of state for Science and Technology Award for the promotion of invention 1993, the Invention Prize and 4th International Conference on Soft Computing (IIZKA 96') Best Paper Award in 1996, and the IEICE Achievement Award in 1997. He serves as the President of the Institute of Basic Semiconductor Technology-Development (Ultra Clean Society). He is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Institute of Electronics of Japan, the Japan Society of Applied physics, and the ECS.

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