A Low-noise Bi-CMOS Linear Image Sensor with Auto-Focusing Function

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A Low-Noise Bi-CMOS Linear Image Sensor with Auto-Focusing Function

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Abstract—**A bipolar imaging device consisting of a capacitor loaded emitter follower circuit for a phototransistor has been implemented into a linear image sensor having two lines of 48-bit array for an auto-focus camera system, which has capabilities of self-noise reduction and charge amplification. The linear image sensor has been demonstrated experimentally to exhibit excellent performance such as a responsivity of 24 V/x · s, a wide dynamic range of 85.3 dB at a storage time of 10 ms, and an ambient temperature of 25°C, a high S/N ratio of 27.6 dB at a faceplate light intensity of 1×10^{-3} lx, a storage time of 200 ms, and an ambient temperature of 25°C and wide applicable light intensity illumination from 1×10^{-3} to 1×10^{4} lx.**

I. Introduction

RECENTLY, CCD linear image sensors have been remarkably improved, where sensors having thousands of bits have been realized. In the applications to facsimile or copy machines, the sensors play an important role as key devices. Also, the sensors have been applied to instruments such as position detectors and distance-measuring devices. The most popular application of the sensors to a distance-measuring system is in auto-focus single-lens-reflex cameras, where the CCD linear image sensor has made a great contribution. The distance-measuring accuracy in an auto-focus camera mainly depends on the performance of the linear image sensor. For example, to establish accurate focusing of a photographic object illuminated by a low light level, the linear image sensor is required to have a very small random noise level, that is, the S/N ratio for very a low light level must be very high. The authors have developed a novel bipolar image sensor called a Base-Stored Image Sensor (BASIS) having high responsivity, low random noise, and wide dynamic range characteristics [1].

BASIS is characterized by the capacitor loaded emitter follower circuitry using a phototransistor. Such a circuit configuration has enabled the establishment of a wide dynamic range of linearity for input light signal and a low output impedance due to its amplification capability. BASIS exhibits a remarkable feature of self-noise reduction capability, which realizes a high S/N ratio at a very low light level. This self-noise reduction capability is realized by introducing a hybrid reset operation [1], [2]. BASIS has been implemented into a linear image sensor having two lines of 48-bit array for an auto-focus camera, which is characterized by a very wide dynamic range of linearity, a very high S/N ratio at a low light level, high responsivity, low power dissipation, and auto-focusing functions such as a real time peak light intensity monitoring.

This paper reports representative characteristics for this BASIS linear image sensor. The circuit operation and structure of the BASIS linear image sensor are described in Section II. Section III describes typical characteristics. Random noise and fixed pattern noise are discussed in Section IV. The performance of the BASIS linear image sensor is summarized in Section V. The conclusion is given in Section VI.

II. Circuit Operation and Structure of BASIS Linear Image Sensor

The linear image sensor developed for an auto-focus camera consists of two lines of a 48-bit array and one optical black cell (OB) having a bit pitch of 30 μm whose circuit configuration is illustrated in Fig. 1(a). The image of an ideal light source focused on the sensor surface by the auto-focus optics system of the camera is a spot 60 μm in diameter, which is determined by the resolution of the optics. In order to detect the center of the image precisely, the bit pitch needs to be made smaller than at least half of the image spot size, i.e., 30 μm. The 48-bit array configuration is required to realize auto-focusing for various lens systems, such as wide-angle lenses, telephoto lenses, etc. For a telephoto lens having a long focal length of 300 mm, for instance, it is possible to measure the distance of an object and calculate the amount of defocusing precisely and quickly even if the object is located in an infinite distance and the lens is focused on the closest position. The two-line configuration is essential to calculate the amount of defocusing from the separation of images on these two-array lines.

The circuit configuration and a cross-sectional view of the unit cell of this linear sensor are shown in Fig. 1(b) and (c), respectively. This unit cell consists of a phototransistor, a pMOS Q_P connected to the base, two nMOS's Q_{N1}, Q_{N3} connected to the emitter, a switching transistor Q_{N2}, and two capacitors C_T and C_{E1}. Here, C_{E1} is the

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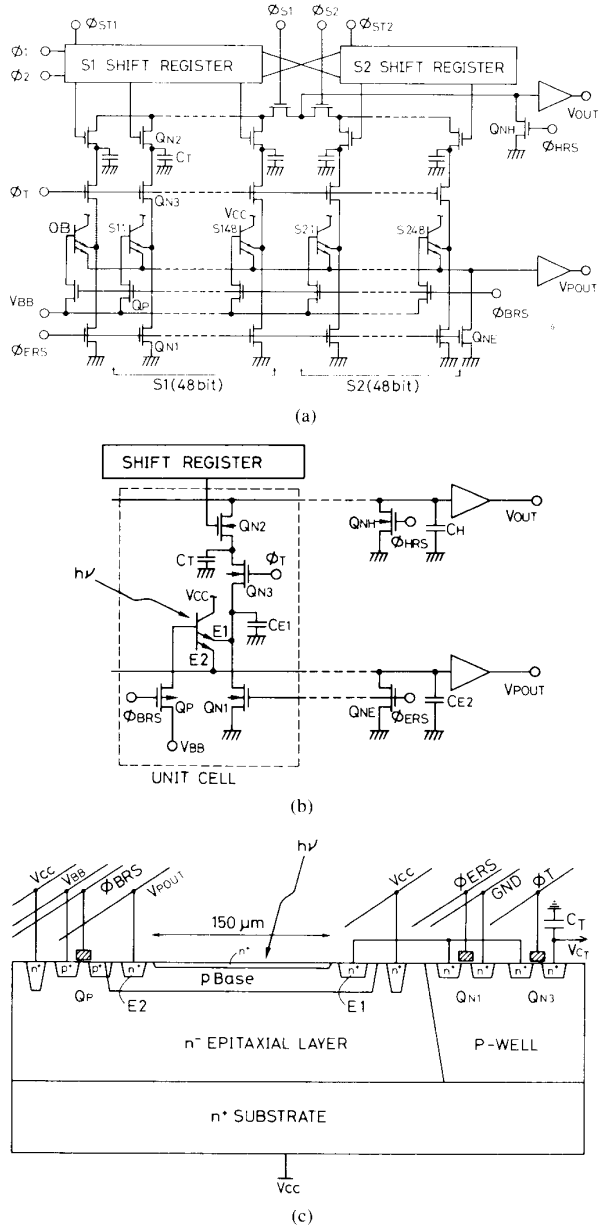

Fig. 1. (a) Circuit configuration of BASIS linear image sensor having two lines of 48-bit array. (b) The unit cell of BASIS linear image sensor. (c) Schematic cross-sectional view of the unit cell of BASIS linear image sensor.

stray capacitance of the emitter. Note that in Fig. 1(b), one nMOS Q_{N3} and one capacitor C_{E1} are additionally introduced to improve the performance of practical line sensors compared to the basic unit cell operating in forward-biased storage discussed in [1]. The phototransistor having two emitters is in a capacitor loaded emitter follower circuit configuration. One of these two emitters ($E1$) is used for the signal outputs of individual cells, while the other emitter ($E2$) is connected to a common sensing node for real-time peak intensity monitoring of the light signal to adjust the storage time of the line sensor having a most accurate distance measurement. This real-time peak light intensity monitoring can be achieved by the nondestructive read-out characteristic of BASIS [1], [2]. BASIS requires one bipolar phototransistor, one pMOS, and three nMOS transistors for the unit cell of the line sensor to improve performance with the introduction of a hybrid reset operation [1]. Thus, this linear image sensor has a structure suitable to be fabricated by conventional Bi-CMOS technologies. The Bi-CMOS structure enables the BASIS linear sensor to have intelligent functions in the future.

A typical timing chart of this linear image sensor is shown in Fig. 2, where the operational sequence is also illustrated including clamp reset, transient reset, storage, and read-out operations [1], [2]. The base voltage of the phototransistor is clamped to V_{BB} through the pMOS Q_P in the clamp reset operation (ϕ_{BRS}) while the emitter is kept at a floating potential state. Emitters $E1$ and $E2$ are grounded through the nMOS Q_{N1} and Q_{NE} in the transient reset operation (ϕ_{ERS}), and, at the same time, the temporary storage capacitor C_T is completely discharged through the nMOS $Q_{N3}(\phi_T)$. The light signal storage starts just after the transient reset operation. During the storage operation, both emitters $E1$ and $E2$ are floating so that the emitter voltages V_{E1} and V_{E2} increase linearly following the base voltage V_B. Since emitter $E2$ is wired to a common sensing node and to an output amplifier directly, the monitor output V_{POUT} of the base voltage in the phototransistor irradiated by the highest light intensity is obtained in real time. The emitter voltage V_{E2} is approximately expressed as the following equation:

$$C_{E2} \cdot \frac{dV_{E2}}{dt} = nI_0 \cdot \exp \frac{q}{KT}\left\{\frac{i_p}{C_{\text{sum}}} t - V_{E2}\right\} \quad (1)$$

where C_{E2} is the stray capacitance of a common line, n is the number of phototransistors receiving highest light irradiation, I_0 is the saturation current, C_{sum} is total base capacitance, and i_p is the photo-generated current. The solution of (1) is given by

$$V_{E2} = \frac{i_p \cdot t}{C_{\text{sum}}} + \frac{KT}{q} \ln\left\{\frac{nI_0}{i_p} \cdot \frac{C_{\text{sum}}}{C_{E2}}\right\}. \quad (2)$$

It is clearly seen from (2) that the peak signal output is proportional to $i_p \cdot t$.

The peak light intensity monitoring output V_{POUT} from 96 bits is shown as a function of the time for various light intensities in Fig. 3. The value of V_{POUT} is obtained through the source follower amplifier having a gain of 0.9.

The storage operation is finished when the peak light intensity monitoring output V_{POUT} reaches a predetermined critical value V_{CR}, which results in starting the read-out operation as shown in Fig. 2. The light signals of all phototransistors are simultaneously transferred to the temporary storage capacitors C_T through the nMOS Q_{N3} by applying ϕ_T. Each light signal stored in C_T is read out to the output line through the nMOS Q_{N2} following the scanning pulse from the shift register. The light signal is

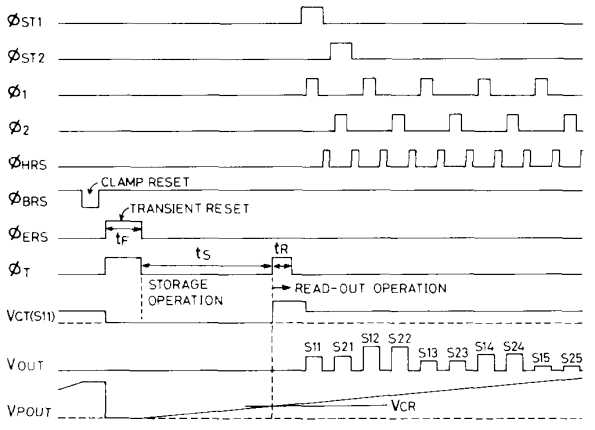

Fig. 2. Typical operational timing chart of BASIS linear image sensor. The operational sequence is also illustrated.

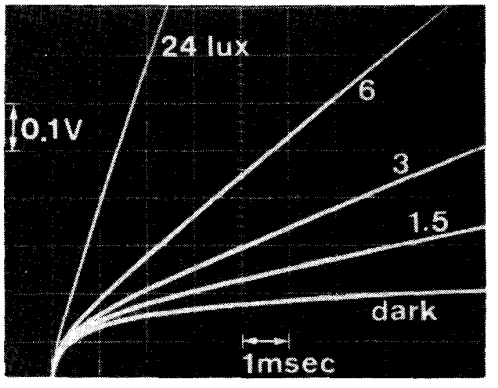

Fig. 3. Waveforms of peak light intensity monitoring output for various light intensities.

read out alternately from two lines S_1 and S_2, where the clock rates of ϕ_1 and ϕ_2 are 10 kHz for an auto-focusing function, respectively. The schematic light signal waveform $V_{CT}(S_{11})$ stored in C_T is illustrated in Fig. 2, where there is a signal decrease due to the division of the capacitance ratio $(C_H/(C_H + C_T))$ after the read-out operation. Here, C_H is the stray capacitance of the output line as shown in Fig. 1(b).

Typical device parameters are summarized in Table I. Fig. 4 shows photograph of this linear image sensor mounted in a mold package. This is the first case to mount a line sensor in a mold package for practical use.

III. Characteristics of the Linear Image Sensor

A. Photo-electric Conversion Characteristics

The characteristics of photo electric conversion, that is, the output voltage versus the light intensity on the faceplate of the sensor, are shown in Fig. 5 for various storage times, where these data are obtained under the conditions of $V_{cc} = 5$ V, the transient reset time $t_F = 20$ μs, the light source has a color temperature of 2854 K, and the IR cut filter has a cutoff wavelength of 740 nm. The linearity has been obtained in the range of the output voltage from

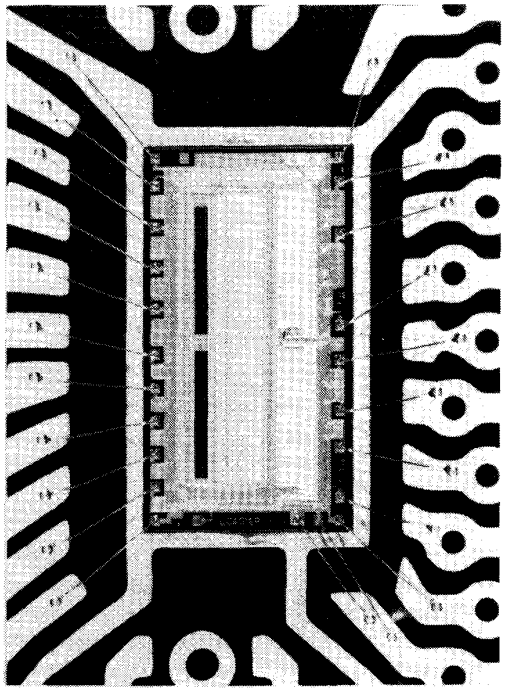

Fig. 4. The photograph of the BASIS linear image sensor mounted in a mold package.

TABLE I
Typical Device Parameters of BASIS Linear Image Sensor

n^--layer	Thickness	5 μm
	Impurity Concentration	2×10^{14} cm^{-3}
Aperture Size of a Cell		30×150 μm^2
Pitch		30 μm
Number of Cells		48 bit x 2 line
Chip Size		2.5×4.6 mm^2
Package		22 pin dual in line mold Package

about 1 mV to 2.2 V for the fixed storage time. Moreover, the linearity is maintained for light intensities ranging from 1×10^{-3} to 1×10^{4} lx by adjusting the storage time. It is seen from Fig. 5 that the light intensity required to produce a given signal output voltage increases inversely proportional to the storage time from 100 ms down to 100 μs. When the storage time is reduced from 100 to 10 μs, however, an increase in the light intensity required to yield the same signal output voltage becomes less than a factor of 10. This is the reason why the effective storage time becomes longer than the given storage time t_s; the light signal storage is carried out in a part of the transient reset time t_F (20 μs) and in a whole period of t_R (2 μs) at

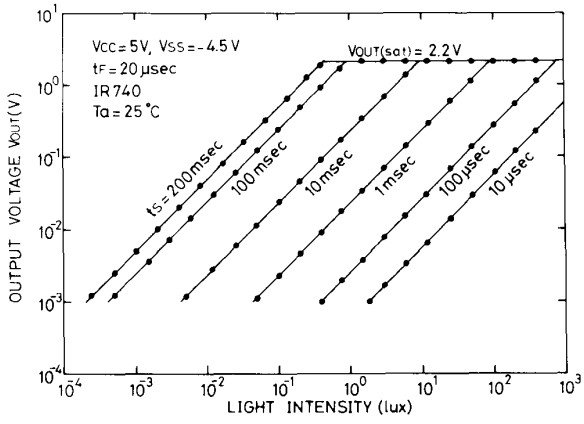

Fig. 5. Photo-electric conversion characteristics. Output voltage is plotted as a function of the faceplate light intensity on the faceplate of the sensor for various storage times t_s.

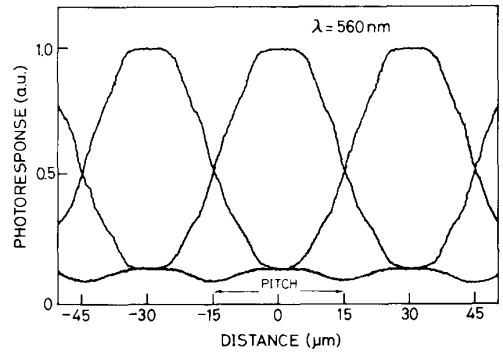

Fig. 6. Aperture response. Aperture response is illustrated over three unit cells at a wavelength of 560 nm.

the read-out operation. The value of t_s is defined by the period from the trailing edge of ϕ_{ERS} in the transient reset to the leading edge of ϕ_T in the read-out operation as shown in Fig. 2. Thus, the effective storage in the transient reset and the read-out operation cannot be neglected when the storage time t_s decreases down to 10 μs.

A responsivity of 24 V/lx · s and an output saturation voltage of 2.2 V are observed from Fig. 5. The emitter saturation voltage V_E(sat) for the phototransistor itself is V_{cc}, while the output saturation voltage V_{out}(sat) is given by the next expression.

$$V_{\text{out}}(\text{sat}) = (V_{GH} - V_{th}) \cdot \frac{C_T}{C_T + C_H} \cdot G_{SF} \qquad (3)$$

where V_{GH} is the high level of pulse ϕ_T applied to Q_{N3}, V_{th} is the threshold voltage of Q_{N3}, C_H is the stray capacitance of the output signal line, and G_{SF} is the gain of the output source follower amplifier. Using the real values of V_{GH} = 5 V, V_{th} = 1.0 V, C_T = 5.6 pF, C_H = 3.3 pF, and G_{SF} = 0.9, an output saturation voltage V_{out}(sat) of about 2.26 V is obtained, which coincides well with the measured value.

B. Aperture Response

The aperture response of BASIS can be controlled by the structure of the isolation region between the adjacent unit cells. The isolation has been constituted with the n^+ region having a width of 4 μm and a depth of 1.2 μm. These dimensions have been adopted so as to exhibit half of a maximum response for each cell at the center of the isolation region in order to keep the photoresponse in the adjacent cell. The photoresponse in the adjacent cell is designed to decrease linearly toward the center of that cell. This enables the spatial resolution to be improved up to 1/10 of the bit pitch (for example, 30 μm) by correlating output signals from two lines S_1 and S_2. The aperture response is illustrated over three unit cells at a wavelength of 560 nm in Fig. 6. The small level photoresponse appears in whole remaining cells due to the coupling between the base and the common emitter line for the peak light intensity monitoring through the base-to-emitter capacitance C_{be}. This small-level photoresponse also appears in the optical black cell, so that this influence is cancelled by subtraction between the photo-cell and the optical black cell.

C. Spectral Photoresponse

The characteristic of spectral photoresponse is shown in Fig. 7, where the peak responsivity has appeared at around a wavelength of 750 nm. The ripple observed in Fig. 7 is caused by the multi-interference in the dielectric layers on the silicon surface, which depends upon the dielectric layer materials and thicknesses.

D. Photoresponse Nonuniformity

Fixed pattern noise (*FPN*) originates from two factors. One is generated even in a dark state. Another is generated by light illumination. The latter is defined as a photoresponse nonuniformity (PRNU). Fig. 8 shows the characteristic of FPN_{pp} (the peak-to-peak voltage of *FPN*) versus the light intensity for a storage time of 100 ms, where the signal output voltage is also plotted as a function of light intensity. *FPN* increases linearly proportional to the light intensity, except for a very small light intensity region where dark level *FPN* remains.

PRNU is caused by the dimensional fluctuation resulting from process variations. To put it more concretely, the fluctuation of the total base capacitance C_{sum} and the aperture size A_P of the individual cells are the main origins of PRNU. PRNU is derived from the expression giving the base voltage ($V_B \propto A_P/C_{\text{sum}}$) such as

$$\frac{\Delta V_B}{V_B} = \frac{\Delta A_P}{A_P} - \frac{\Delta C_{\text{sum}}}{C_{\text{sum}}}. \qquad (4)$$

It is seen from Fig. 8 that a PRNU of less than 2 percent has been realized in this linear image sensor. PRNU is easily cancelled in various application systems because of its proportionality to light intensity.

The dark-level *FPN* will be discussed in detail in the next section.

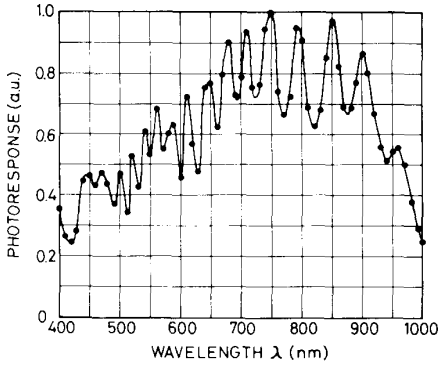

Fig. 7. Characteristic of spectral photoresponse.

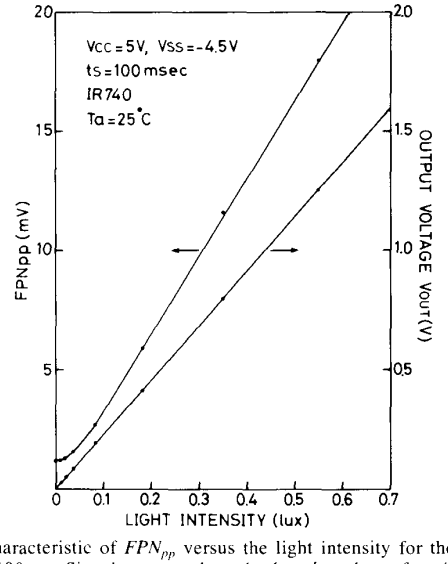

Fig. 8. Characteristic of FPN_{pp} versus the light intensity for the storage time of 100 ms. Signal output voltage is also plotted as a function of the light intensity.

IV. Random Noise and Fixed Pattern Noise

A. Random Noise

The fundamental characteristics of random noises (*RN*) and fixed pattern noises (*FPN*) have already been described in a previous paper [1]. Self-noise reduction capability essentially comes from the characteristics of the base-to-emitter p-n junction itself, where high base voltage due to fluctuations induces large emitter current resulting in the rapid decrease of the base voltage to catch up low base voltage due to the fluctuations. This self-noise reduction mechanism becomes remarkable within a short transient reset time at a deep forward-bias reset operation.

The *RN*rms random noise voltage in root mean square is plotted as a function of the storage time t_S without the light illumination for two ambient temperatures in Fig. 9, where the transient reset time t_F is set at 20 μs. The transient reset time t_F is designed to be less than several tenths of a microsecond in practical application systems. It is seen from Fig. 9 that the *RN*rms scarcely increases with an increase in storage time t_S up to 10 ms from 105 to 120

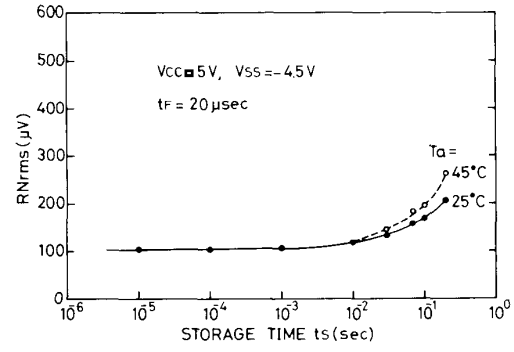

Fig. 9. Characteristics of the random noise *RN*rms versus the storage time t_S for ambient temperatures of 25 and 45°C.

μV and starts to increase for an increase of t_S greater than 10 ms up to 205 μV (at T_a = 25°C) and 260 μV (at T_a = 45°C) at t_S of 200 ms mainly due to the dark current.

BASIS has a charge amplification function with a factor of C_T/C_{sum}, even though the output voltage is equal to the signal base voltage. Thus, authors usually discuss noise voltage at the load capacitor. It is easy to transform discussions from noise voltage to electron numbers.

A detailed discussion about the random noise caused by the dark current will be described in another paper.

B. Fixed Pattern Noise

The origins of *FPN* are classified into five categories: 1) *FPN* occurs at the instance of turn-off pMOS Q_P at the final stage of the clamp reset operation, which is caused by the fluctuations of the gate-to-drain capacitances of pMOS Q_P. But, this *FPN* is able to be reduced drastically in the succeeding transient reset operation, as well as random noise reduction. 2) A little bit of *FPN* appears at the instant when turning off nMOS Q_{N1} at the final stage of the transient reset operation, which is caused by the fluctuation in the base-to-emitter capacitances of the phototransistors. 3) *FPN* appears in the storage time region in less than 30 ms, where the main origins are the fluctuations of C_{sum} and the current gain h_{fe} of the phototransistors in a wide range of the current densities. 4) *FPN* is caused by the dark currents in the storage time region over 30 ms. 5) *FPN* comes from the read-out circuitry.

Fig. 10 shows the characteristic of the transient reset time dependency of FPN_{pp} in the dark state, where an FPN_{pp} of a few millivolts is observed at an initial stage in the transient reset operation. FPN_{pp} is reducing with the lapse of t_F and converging approximately to 0.5 mV at a transient reset time of 10 ms, which is given by the sum of the noises of origins 2), 3), and 5).

FPN_{pp} is plotted as a function of the storage time t_S for two ambient temperatures T_a such as 25 and 45°C in Fig. 11, where the transient reset time t_F is set at 20 μs. It is clearly seen from Fig. 11 that FPN_{pp} almost does not depend on the ambient temperature variation in the range of storage time t_S up to 30 ms while FPN_{pp} exhibits a rapid increase with an increase of t_S greater than 30 ms for higher temperature operation. The rapid increase in FPN_{pp}

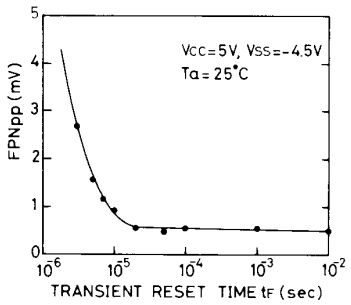

Fig. 10. Characteristics of the fixed pattern noise FPN_{pp} versus the transient reset time t_F.

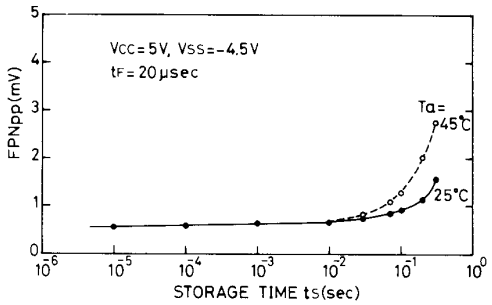

Fig. 11. Characteristics of the fixed pattern noise FPN_{pp} versus the storage time t_s for ambient temperatures of 25 and 45°C.

at storage times longer than 30 ms is mainly caused by an influence of the increase of the dark currents. The dark current density of this BASIS linear image sensor is 0.2 nA/cm^2 at V_{cc} of 5 V and T_a of 25°C.

FPN_{pp} exhibits a slight increase from 0.56 to 0.77 mV for an increase in storage time from 10 μs to 30 ms, which comes from noise origin 3). The base voltage fluctuation in the storage operation is given by

$$\Delta V_B = \frac{i_E \cdot t_S}{C_{\text{sum}} \cdot (h_{fe} + 1)} \cdot \left(\frac{\Delta C_{\text{sum}}}{C_{\text{sum}}} + \frac{\Delta h_{fe}}{h_{fe} + 1} \right) \quad (5)$$

where i_E is the emitter current expressed as

$$i_E = C_{E1} \cdot \frac{dV_{E1}}{dt}. \quad (6)$$

Here, C_{E1} is a stray capacitance of emitter $E1$. The emitter current i_E induces the hole recombination current in the base region given by $i_E/(h_{fe} + 1)$, resulting in a decrease of the base voltage. The fluctuations of h_{fe} and C_{sum} in the phototransistors introduce the nonuniform decreases of base voltage V_B given by (5). Equation (5) indicates that FPN_{pp} slightly increases proportional to the storage time as shown in Fig. 11.

V. Performance of BASIS Linear Image Sensor

The performance of a BASIS linear image sensor having two lines of 48-bit array is summarized in Table II. Dynamic ranges are obtained under the typical operational conditions of t_S = 10 ms and T_a = 25°C, where the values of RNrms and FPN_{pp} are 0.12 and 0.65 mV from Figs. 9 and 11, respectively. The high sensitivity of the sensor is greatly needed, particularly at low light intensity illuminations in an auto-focus camera system, so that the S/N ratio is defined under conditions of a faceplate light intensity of 1 × 10^{-3} lx, a storage time of 200 ms, and an ambient temperature of 25°C. Under these conditions, the signal output voltage V_{out} is 4.8 mV from Fig. 5, RNrms is 0.20 mV from Fig. 9, and FPN_{pp} is 1.1 mV from Fig. 11, resulting in an S/N ratio such as V_{out}/RNrms = 27.6 dB and V_{out}/FPN_{pp} = 12.8 dB. These data are sufficient for practical use. However, Table II indicates that the FPN must be decreased by a factor of one order for future improvements of the BASIS linear image sensor where FPN is less than RN.

TABLE II
Performance of BASIS Linear Image Sensor Having Two Lines of 48-Bit Array

Scanning rate		20	kHz
Driving Voltage	V_{cc}	5	V
	V_{ss}	-5	V
Power Dissipation		10	mW
Saturation Output Voltage $V_{out(sat)}$		2.2	V
Responsivity		24	V/lux·sec
Dynamic Range (t_s=10msec, T_a=25°C)	$\frac{V_{out(sat)}}{RN_{rms}}$	85.3	dB
	$\frac{V_{out(sat)}}{FPN_{pp}}$	70.6	dB
S/N Ratio (light intensity 1x10^{-3}lux, t_s=200msec, T_a=25°C)	$\frac{V_{out}}{RN_{rms}}$	27.6	dB
	$\frac{V_{out}}{FPN_{pp}}$	12.8	dB
Applicable Light Intensity Range		1x10^{-3}~1x10^{4}lux	
Photoresponse Non-Uniformity PRNU		< 2.0	%
Image Lag		< 0.3	%

VI. Conclusion

A novel image sensor, BASIS, having capabilities of amplification and self-noise reduction has been implemented into a linear image sensor having two lines of 48-bit array where the real-time peak light intensity monitoring is introduced as an auto-focusing function. The BASIS linear image sensor has been demonstrated experimentally to exhibit excellent performance such as a responsivity of 24 V/lx · s, a wide dynamic range of 85.3 dB for random noise and 70.6 dB for fixed pattern noise at a condition of storage time t_S = 10 ms and an ambient temperature T_a = 25°C, and wide applicable light intensity illumination from 1 × 10^{-3} to 1 × 10^4 lx by

adjusting the storage time following the real-time peak light intensity monitoring signals.

In the linear image sensors developed so far, the dynamic range is restricted by large fixed pattern noise due to process variations. Thus, an improvement in the fabrication process has the possibility of increasing the dynamic range by a factor of 10.

Detailed discussions on the noise characteristics of BASIS will be described in a following paper.

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REFERENCES

[1] N. Tanaka, T. Ohmi, and Y. Nakamura, "A novel bipolar imaging device with self-noise reduction capability," *IEEE Trans. Electron Devices*, this issue, pp. 31-38.

[2] T. Ohmi and N. Tanaka, "Photoelectric converter," U.S. Patent 4 686 554.

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Tadahiro Ohmi (M'81) was born in Tokyo, Japan, in January 10, 1939. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Tokyo Institute of Technology, Tokyo, in 1961, 1963 and 1966, respectively.

Prior to 1972, he served as a Research Associate in the Department of Electronics of the Tokyo Institute of Technology, where he worked on Gunn diodes such as velocity overshoot phenomena, multivalley diffusion and frequency limitation of negative differential mobility due to an electron transfer in the multivalleys, high-field transport in semiconductors such as unified theory of space-charge dynamics in negative differential mobility materials, bloch oscillation-induced negative mobility and bloch oscillators, and dynamics in injection lasers. He is presently a Professor in the Department of Electronics, Faculty of Engineering, Tohoku University. He is currently engaged in research on high-performance ULSI such as ultra-high-speed ULSI: the Current Overshoot Transistor LSI, HBT SLI, and SOI on metal substrate, Base Store Image Sensor (BASIS) and advanced semiconductor process technologies, i.e., ultra-clean technologies such as high-quality oxidation, high-quality metallization due to low kinetic energy particle bombardment, very low temperature Si epitaxy having simultaneous doping capability due to low kinetic energy particle bombardment, crystallinity control film growth technologies due to low kinetic energy particle bombardment, *in situ* wafer surface cleaning technologies due to low kinetic energy particle bombardment, highly selective CVD, highly selective RIE, high-quality ion implantations having low-temperature annealing capability, etc., based on the new concept supported by a newly developed ultra-clean gas supply system, ultra-high-vacuum compatible reaction chamber having a self-cleaning function, ultra-clean wafer surface cleaning technology, etc.

He serves as a general chairman of the International Symposium on Power Semiconductor Devices and the International Symposium on ULSI Ultra Clean Technologies.

Dr. Ohmi is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Institute of Electrical Engineers of Japan, the Japan Society of Applied Physics, and the Electrochemical Society. He serves as a general chairman of the International Symposium on Power Semiconductor Devices and the International Symposium on ULSI Ultra Clean Technologies.

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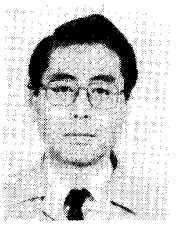

Yoshio Nakamura (M'85) was born in Niigata Prefecture, Japan, in 1948. He received the B.S. degree from the University of Electro-communications in 1971 and the M.S. degree in electronics engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1973.

He joined Oki Electric Industry Co., Ltd., Tokyo, Japan, in 1979, where he worked on bipolar LSI design. In 1979, he joined the Toyota Central Research and Development Laboratories, Inc., Nagoya, Japan, where he was engaged in LSI design and the development of power devices. In 1985, he joined the Semiconductor Development Division at Canon Inc., Kanagawa Prefecture, Japan, where he is now Manager of the Design Department.

Mr. Nakamura is a member of the Institute of Electronics, Information and Communication Engineers of Japan. He received the outstanding paper award of the IEEE International Conference of Computer Design 1984.

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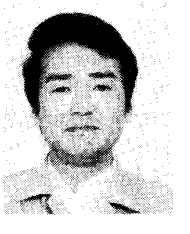

Shigeyuki Matsumoto was born in Tokyo, Japan, in 1950. He received the Bachelor's and Master's degrees in physics from Waseda University, Tokyo, Japan, in 1975 and 1977, respectively.

In 1977, he joined the Canon Research Laboratory, where he was involved in inkjet process technology. Since 1980, he has developed I L, CMOS, and advanced bipolar processing in the Component Development Center. At present, he is developing sensor device and semiconductor process technology, and is Manager of the semiconductor process group.

Mr. Matsumoto is the member of the Japan Society of Applied Physics and the Society of Polymer Science of Japan.