# Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing


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# Improvement of Aluminum–Si Contact Performance in Native-Oxide-Free Processing

M. MIYAWAKI, S. YOSHITAKE, AND TADAHIRO OHMI, MEMBER, IEEE

*Abstract*—**The improvement of Al-to-Si contact performance, such as a low contact resistance of 0.4 $\mu\Omega \cdot cm^2$ and a Schottky junction having an $n$ factor of 1.02 without any thermal treatment, has been achieved by the newly developed native-oxide-free processing, which consists of processes such as $N_2$ gas sealed wet cleaning using pure water with low dissolved oxygen (20 ppb), wafer transport and loading in an $N_2$ environment, and Al deposition by low-energy ion bombardment.**

## I. Introduction

As DEVICE geometry has been scaled down to submicrometer areas, the parasitic resistance in an interconnection structure is going to increase in significance because the contact resistance increases at contact holes. Therefore, a low and stable contact resistance to shallow $n^+$ and $p^+$ layers is required in order to realize highly reliable submicrometer ULSI's.

However, native silicon oxide layers are easily formed on Si surfaces in an environment of coexistence of oxygen and water (moisture) [1], [2], and consequently give rise to an increase of the contact resistance with accompanying increases of their nonuniformity and fluctuation. In order to solve these problems, it is essential to develop native-oxide-free processing. Particularly, the highly doped $n^+$ region is immediately oxidized even in a rinsing process in ultrapure water having a high dissolved oxygen concentration (600 ppb), which mainly comes from the diffusion of oxygen in air to the ultrapure water. Therefore, we have developed net wet cleaning equipment where ultrapure water and a diluted HF vessel are sealed by $N_2$ gas. By using this equipment, the Si substrate surface is chemically etched with diluted HF acid dip, rinsed in water with low dissolved oxygen (20 ppb), and dried with $N_2$ gas blowing in an $N_2$ environment (hereafter called as the N-process).

This paper describes improvements of Al/$n^+$-Si contact resistance down to 0.4 $\mu\Omega \cdot cm^2$ and the performance of a Schottky junction of Al/n-Si without any thermal treatment. These high performances are achieved by an introduction of an $N_2$ gas sealed cleaning and drying process, wafer transport in the $N_2$ environment, and Al film deposition by low-energy ion-bombardment bias sputtering [3]. In addition, the fluctuation of the contact resistance has been demonstrated to be drastically improved compared to that in a conventional process.

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The authors are with the Department of Electronics, Tohoku University, Sendai 980, Japan.

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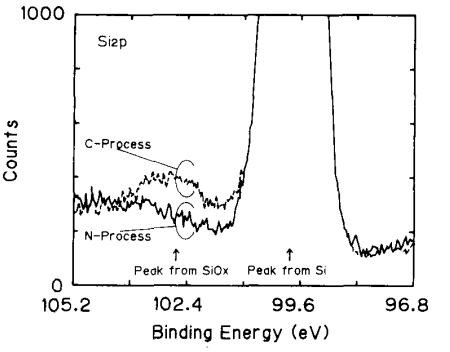


Fig. 1. XPS $Si_{2p}$ spectra of $n^+$-Si surface in the N-process (solid) and C-process (dashed).

## II. Experiments and Results

In order to confirm the effect of the $N_2$ gas sealed rinsing and drying process on the suppression of native oxide growth, the existence of native oxide layers on the $n^+$-Si surface has been evaluated by X-ray photoelectron spectroscopy (XPS). Fig. 1 shows the XPS $Si_{2p}$ spectra from silicon oxide on the $n^+$-Si surface obtained in the N-process and in the conventional one (C-process). In the air, the C-process is to perform succeeding processes such as HF dipping, rinsing in pure water with a dissolved oxygen concentration (600 ppb), and drying with $N_2$ gas blowing. It is seen from Fig. 1 that the height at which $Si_{2p}$ peaks from $SiO_x$ ($0 \le x \le 2$) in the N-process is significantly lower than that in the C-process. The N-process, therefore, has been confirmed to be very effective in preventing the native oxide layers from growing on the $n^+$-Si surface.

Contact resistance is measured by the four-point probe Kelvin method [4]. The $n^+$ regions are formed by implanting $1 \times 10^{16}$ $cm^{-2}$ of arsenic at 70 keV and annealing at a temperature of 1000°C for 10 min in an $N_2$ gas ambient. As a result, the sheet resistance and the surface carrier concentration are 30 $\Omega/\square$ and $0.8 \times 10^{20}$ $cm^{-3}$, respectively. In the Al sputtering chamber, the *in-situ* substrate surface cleaning [5] is carried out in order to remove the adsorbed impurity molecules by Ar ion bombardment having an energy of 2 ~ 3 eV at a working gas pressure of $8 \times 10^{-3}$ torr.

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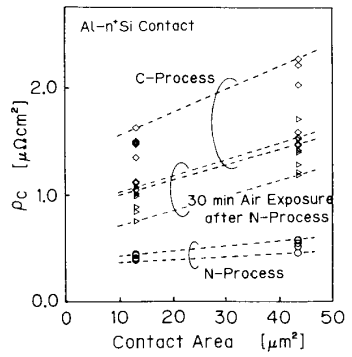


Fig. 2. Contact resistances of Al/n$^+$-Si (100) as a function of contact hole size.

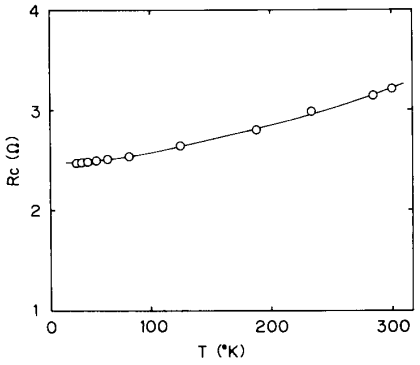


Fig. 3. Contact resistance of Al/n$^+$-Si (100) as a function of temperature.

Then Al films are deposited on the substrate under the optimum condition Ar ion bombardment energy of 50 eV at a working pressure of $3 \times 10^{-3}$ torr at room temperature, using the ultrahigh-purity Ar gas supplied through the ultra-clean gas delivery system [6]. The main component of impurities in Ar gas is $H_2O$, which has been reduced to about $2 \sim 3$ ppb or below at the inlet to the chamber. The base pressure of the main chamber is about $1 \times 10^{-9}$ torr. The measured contact resistance of samples in the N-process becomes as small as 0.4 $\mu\Omega \cdot cm^2$ without any thermal treatment, as illustrated in Fig. 2. This value is nearly equal to the conventional one obtained after 450–500°C annealing [7], [8]. Furthermore, it is seen from Fig. 2 that the fluctuations of the contact resistances in the N-process are decreased by a factor of 3 compared to those in the C-process. Temperature dependence of the contact resistance has been evaluated in the range from 27 to 300 K. It is clearly seen in Fig. 3 that the contact resistance slightly decreases with a decrease of ambient temperature. This tendency is similar to the theoretical calculation [9] in the range of surface impurity concentration beyond $3 \times 10^{19}$ $cm^{-3}$.

These three processes for metallization, i.e., the $N_2$ gas sealed cleaning and drying process, wafer transport in an $N_2$ environment, and Al deposition by low-energy ion bombardment bias sputtering, are essentially required for the improvement of the electrical characteristics of the metal-to-Si interface. Ignoring any one of these processes leads to the degradation of these characteristics. As for wafer transport,

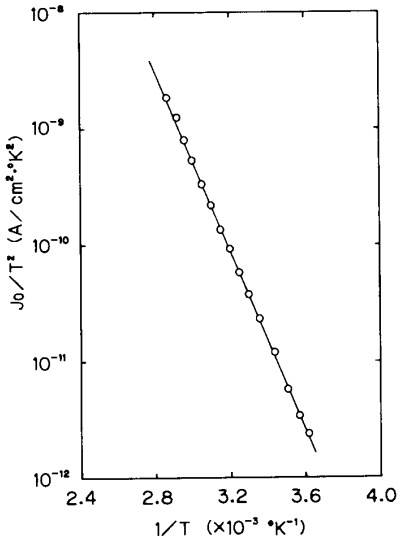


Fig. 4. Arrhenius plot of $J_0/T^2$ for the N-process sample.

the contact resistance degrades to a few $\mu\Omega \cdot cm^2$ where the wafer surface is exposed to the clean room atmosphere having a temperature of 23°C and relative humidity of 40% for 30 min after $N_2$ gas sealed cleaning and drying, as shown in Fig. 2. As for the conditions of Al deposition, we have evaluated the $n$ factor of a Schottky diode on n-type (100) Si wafers with an impurity concentration $2 \times 10^{14}$ $cm^{-3}$. The $n$ factor is 1.02 for the sample fabricated under the optimum ion-bombardment condition of $2 \sim 3$ eV for *in-situ* cleaning and 50 eV for Al deposition, thus showing the formation of an ideal Schottky diode. The Schottky barrier height is 0.77 eV, which is determined from the plot of $\ln(J_0/T^2)$ against reciprocal temperature $(1/T)$ as shown in Fig. 4, where $J_0$ is the saturation current at a reverse-bias voltage of 0.1 V. On the other hand, the $n$ factors for the samples in the N-process with and without *in-situ* cleaning under a higher Ar ion bombardment energy of 50 eV degrade to 1.1 and 1.25, respectively. It is found that *in-situ* cleaning under the optimum ion energy is required to remove contaminant species, such as moisture molecules adsorbed on the substrate surface during transporting and loading to the chamber, even in the N-process.

## III. Conclusion

Native-oxide-free processing has been demonstrated to improve Al-to-Si contact performance such as low contact resistance, the stability of its contact resistance, and an ideal Schottky diode without any thermal treatment.

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## References

[1] M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, and K. Suma,

"Control factor of native oxide growth on silicon in air or in ultrapure water," *Appl. Phys. Lett.*, vol. 55, no. 6, pp. 562–564, Aug. 1988.

[2] M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, and M. Ohwada, "Growth of native oxide on a silicon surface," to be published in *J. Appl. Phys.*, July 15, 1990.

[3] T. Ohmi, H. Kuwabara, S. Saitoh, and T. Shibata, "Formation of high-quality pure aluminum films by low-kinetic-energy particle bombardment," *J. Electrochem. Soc.*, vol. 137, no. 3, pp. 1008–1016, 1990.

[4] S. J. Proctor, L. W. Linholm, and J. A. Mazer, "Direct measurements of interfacial contact resistance, and interfacial contact layer uniformity," *IEEE Trans. Electron Devices*, vol. ED-30, no. 11, pp. 1535–1542, Nov. 1983.

[5] T. Ohmi, T. Ichikawa, T. Shibata, K. Matudo, and H. Iwabuchi, "In situ substrate-surface cleaning for very low temperature silicon epitaxy by low-kinetic-energy particle bombardment," *Appl. Phys. Lett.*, vol. 53, no. 1, pp. 45–47, July 1988.

[6] T. Ohmi *et al.*, "Ultra clean gas supplying system for ULSI fabrication and its evaluation," in *Proc. Ist Int. Symp. Ultra Large Scale Integration Science and Technology, ECS Spring Meeting* (Philadelphia, PA), May 1987, Extended Abstr. 216.

[7] T. J. Faith, R. S. Irven, S. K. Plante, and J. J. O'Neill, Jr., "Contact resistance: Al and Al-Si to diffused $N^+$ and $P^+$ silicon," *J. Vac. Sci. Technol.*, vol. A1, no. 2, pp. 443–448, Apr.–June 1983.

[8] H. H. Berger, "Contact resistance and contact resistivity," *J. Electrochem. Soc.*, vol. 119, no. 4, pp. 507–514, Apr. 1972.

[9] C. Y. Chang, Y. K. Fang, and S. M. Sze, "Specific contact resistance of metal–semiconductor barriers," *Solid-State Electron.*, vol. 14, pp. 541–550, 1971.