Atomically Flat Silicon Surface and Silicon/Insulator Interface Formation Technologies for (100) Surface Orientation Large-Diameter Wafers Introducing High Performance and Low-Noise Metal-Insulator-Silicon FETs

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Atomically Flat Silicon Surface and Silicon/Insulator Interface Formation Technologies for (100) Surface Orientation Large-Diameter Wafers Introducing High Performance and Low-Noise Metal–Insulator–Silicon FETs

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***Abstract*—Technology to atomically flatten the silicon surface on (100) orientation large-diameter wafer and the formation technology of an atomically flat insulator film/silicon interface are developed in this paper. Atomically flat silicon surfaces composed of atomic terraces and steps are obtained on (100) orientation 200-mm-diameter wafers by annealing in pure argon ambience at 1200 °C for 30 min. Atomically flat surfaces with various terrace widths and step structures are observed by atomic force microscopy. It is found that the atomic terrace width changes widely with an off angle of the wafer surface from the (100) lattice plane. It is also found that the direction of the off angle significantly affects the atomically flat surface morphology, i.e., when the directions of the off angles are parallel to the ⟨110⟩ directions, the step structure is composed of alternating pairs of straight and triangular steps. When the directions of the off angles are parallel to the ⟨100⟩ directions, the step structure is composed of only straight steps. By precise control of the off angle and the direction toward the ⟨100⟩ directions for a 200-mm-diameter silicon wafer, we have succeeded in fabricating an atomically flat surface with straight atomic steps and a very uniform terrace width of 140–150 nm on the entire surface of a large-diameter silicon wafer. Furthermore, it is found that only radical-reaction-based insulator film formation technology, such as oxidation utilizing oxygen radicals carried out at a low temperature (400 °C), preserves the atomic flatness of the insulator film/silicon interface. Finally, when MOSFETs are fabricated with an atomically flat interface, they exhibit near ideal subthreshold swing factors, with much smaller fluctuation, extremely lower $1/f$ noise, and higher MOS dielectric breakdown field intensity compared with MOSFETs fabricated with conventional technologies.**

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***Index Terms*—Atomic force microscopy (AFM), CMOSFETs, semiconductor device noise, semiconductor–insulator interfaces, silicon, surface treatment.**

I. Introduction

As THE SCALING down of silicon MOSFETs continues, the flatness and uniformity of the gate insulator film/silicon interface will, if not already, significantly impact the device performance. It is a well-known fact that carrier scattering caused by roughness at the gate insulator film/silicon interface degrades the MOS inversion layer mobility [1], [2]. Moreover, papers have been published about the effect of interface flatness on $1/f$ noise characteristics [3], [4]. A recent article has proposed that the MOS inversion layer mobility and current drivability of MOSFETs can be improved up to a very high speed performance by the introduction of an atomically flat gate insulator film/silicon interface [5]. Furthermore, fluctuations in the electrical characteristics of MOSFETs, as well as $1/f$ noise, increase due to the progression of device miniaturization. This has become one of the most crucial issues in analog and even digital applications of modern scaled-down LSIs [6]–[8]. The fabrication and the control of an atomically flat silicon surface and interface on large-diameter wafers, such as 200 or 300 mm, have drawn much interest from LSI developers, as well as in academic circles.

In the next section, 1200 °C pure argon ambience annealing was applied to 200-mm-diameter (100) orientation silicon wafers, and the atomic flatness of the surface was observed after annealing by atomic force microscopy (AFM). The correlation between the off angles of the wafer surface from the (100) lattice plane and the width of the atomic terrace is discussed, as well as the correlation between the directions of the off angles of the surface and the shape of the atomic terrace and step structure.

In Section III, various oxidation processes were applied to form insulator films on an atomically flat silicon surface. The flatness of the fabricated insulator film/silicon interfaces was analyzed to evaluate the effect of the various oxidation processes.

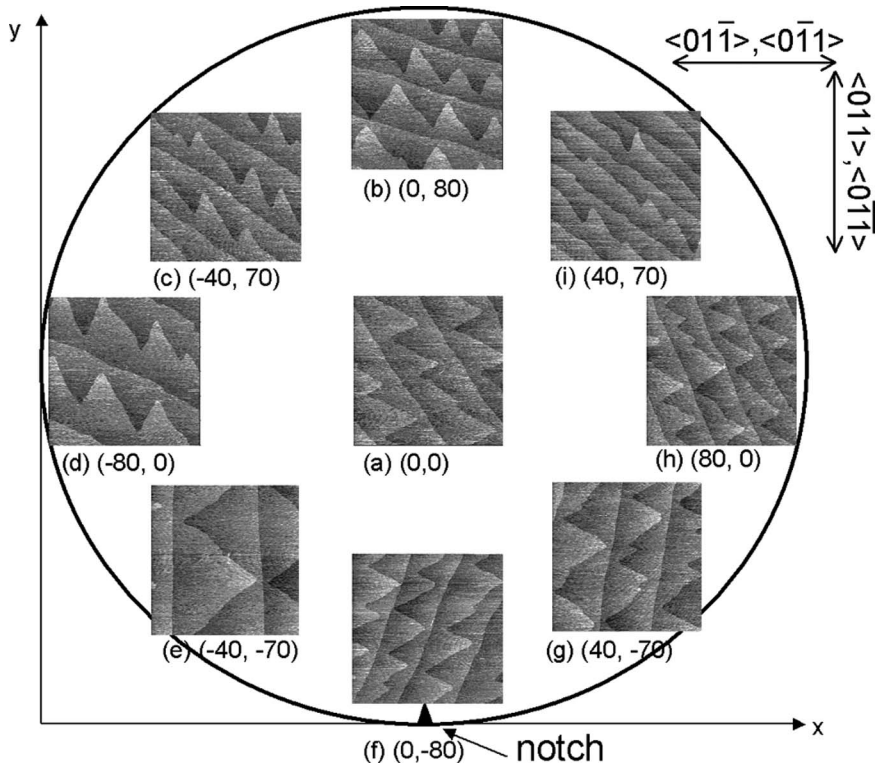

Fig. 1. AFM images, at 3×3 μm, of various positions on the surface of the 200-mm wafer, Wafer 1. The numbers for (a)–(i) correspond to the positions of the measurement point on the wafer in millimeters.

In Section IV, an oxidation process that utilizes the radical-reaction-based insulator film formation technology is introduced into a process flow to fabricate MOSFETs with an atomically flat gate insulator film/silicon interface [8], [20], [22], [23]. Data on the impact of this technology on electrical characteristics of fabricated MOS devices are also provided.

II. Technology to Atomically Flatten (100) Orientation Silicon Large-Diameter Wafer Surface

The silicon wafers used in these experiments were manufactured by slicing 200-mm-diameter Czochralski (Cz) grown boron- or phosphorous-doped silicon ingots with (100) growth direction. The resistivities and corresponding impurity concentrations of the p- and the n-type wafers were $8-12\ \Omega \cdot \mathrm{cm}$ $(1-2 \times 10^{15}\mathrm{cm}^{-3})$ and $0.8-1.2\ \Omega \cdot \mathrm{cm}$ $(3-6 \times 10^{15}\ \mathrm{cm}^{-3})$, respectively. The off angles of both types of wafers were measured by X-ray diffraction (X'pert Pro, PANalitycal) and were therefore guaranteed to be smaller than 0.10° which is a limit of current X-ray diffration monitor. These wafers were treated with a diluted HF (0.5%) solution and an ultrapure water to remove native oxides on the silicon surface and then annealed at 1200 °C in a pure argon ambience under atmospheric pressure for 30 min [11]. The surface morphologies of the various positions of the annealed wafers were observed by using AFM, SPI400 SII, which utilizes a carbon-nanotube probe (Daiken Chemical) by using a tapping scan mode.

A high-temperature annealing, such as 1200 °C, is employed in order to allow surface silicon atoms to migrate and reconstruct themselves into a more stable energy state. Subsequently, this will form an atomically flat surface. It is a well-known fact that at an elevated temperature, a nonreactive ambience with a relatively low oxygen and H_2O concentration, such as 100 ppb, will etch the silicon surface and cause it to become very rough [9]. Therefore, precisely controlling the very low oxygen and H_2O concentrations in nonreactive ambience is critical in this experiment. We have succeeded in developing an ultraclean annealing furnace and ultraclean argon gas supply system that contains an extremely low oxygen and H_2O concentration of less than 0.2 ppb [10].

Figs. 1 and 2 show the 3×3-μm AFM images of the silicon surface at various positions within the p- (wafer 1) and the n-type (wafer 2) wafers respectively. It can be clearly seen in both wafers that the entire surface of the 200-mm-diameter wafer is composed of atomic terraces and steps. As is shown in Fig. 1, the terrace width varies based on different positions within the wafer. Moreover, the shapes of the step structures are composed of alternating pairs of straight and triangular steps for almost all positions, with the exception of Fig. 1(i). However, in Fig. 2, the terrace widths are uniformly maintained at around 140–150 nm across a wide range of positions for the entire 200-mm wafer surface. Furthermore, the shapes of the step structures are composed of only the straight step. Fig. 3(a) and (b) shows the AFM images and the cross-sectional profile of the surface. It has been confirmed that the step heights of both wafers are the height of one atomic layer of (100) orientation silicon, i.e., 0.135 nm. This indicates that an atomically flat surface composed of atomic terraces and steps can be successfully fabricated on the entire surface of the 200-mm-diameter wafers.

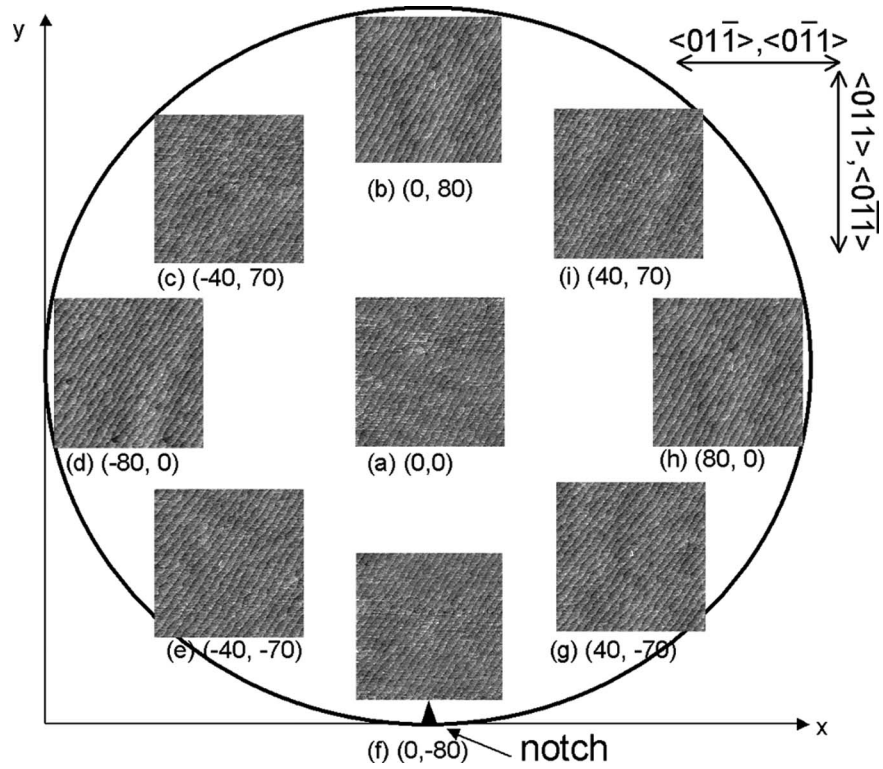

Fig. 2. AFM images, at 3 × 3 μm, of various positions on the surface of the 200-mm wafer, Wafer 2.

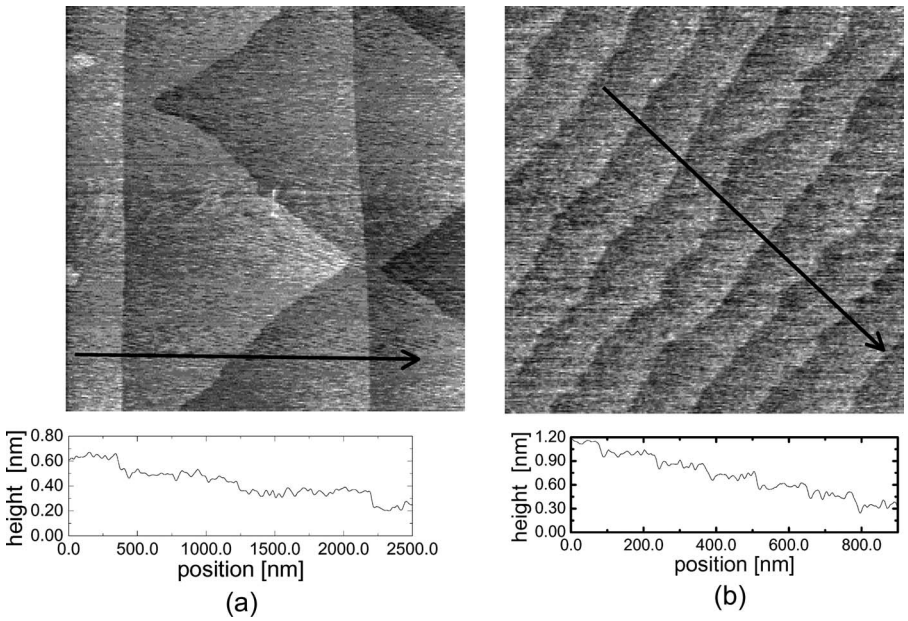

Fig. 3. AFM images of (a) Wafer 1 (3 × 3 μm) and (b) Wafer 2 (1 × 1 μm) surfaces and their cross-sectional profiles under the arrows. Each arrow also indicates the direction of the off angle for the surface. Average step heights for both surfaces are the height of one atomic step of silicon (100), i.e., 0.135 nm.

The silicon surface is set at an off angle from the (100) orientation plane, which can be calculated by measuring the observed atomic terrace width based on the following:

$$\theta \approx \tan^{-1}(0.135/W) \tag{1}$$

where θ is the off angle and W is the atomic terrace width, in nanometers, parallel to the direction of the off angle. The calculated off angle and direction of the off angle of the observed surface are summarized in Table I. Moreover, the shapes of the atomic step and terrace structures of the annealed wafers can be classified based on the directions of the off angles. When the direction of the off angle is parallel to the $\langle 110 \rangle$ directions, the surface is composed of alternating pairs of the straight and the triangular steps. This kind of surface structure has already been reported in other works [11], [12]. However, when

TABLE I
EXTRACTED OFF ANGLES FROM (100) LATTICE PLANE AND DIRECTIONS OF THE OFF ANGLES FROM $\langle 0\bar{1}1\rangle$ AZIMUTH OF THE SURFACES SHOWN IN FIGS. 1 AND 2

	Wafer 1		Wafer 2	
	off angle [deg]	off direction [deg]	off angle [deg]	off direction [deg]
(a)	0.012	32	0.054	326
(b)	0.016	73	0.054	329
(c)	0.015	57	0.051	326
(d)	0.010	65	0.054	326
(e)	0.008	359	0.051	325
(f)	0.015	340	0.054	325
(g)	0.013	350	0.055	323
(h)	0.018	23	0.054	328
(i)	0.017	53	0.055	328

the direction of the off angle is parallel to the $\langle 100\rangle$ directions, the surface is composed of only the straight steps, as shown in Fig. 2. It has been suggested that there are various types of atomic step structures on the (100) orientation silicon surface. They can be characterized by dimer structures of the silicon surface [13]. Our experimental results introduce an additional importance in relation to discussions on the effects of the off angle and its direction on the step structures.

Consequently, due to precisely controlling the very low oxygen and H_2O concentration gas ambience for a high-temperature annealing system, as well as wafer surface off angle and direction, we can fabricate atomically flat silicon surfaces suitable for high-performance semiconductor devices.

The atomic flatness of a silicon surface fabricated by the annealing must be protected so as to present the flat wafers to the next step in the process, such as insulator formation. In particular, native oxide is known to grow on the silicon surface and cause it to roughen [14]–[16]. We evaluated the growth speed of the native oxide on the surface of annealed wafers. Fig. 4(a) and (b) shows the Fourier transform infrared attenuated total reflectance (FTIR-ATR) spectra of (a) a hydrogen-terminated silicon surface after diluted HF treatment for reference and (b) an atomically flat silicon surface after the pure argon ambience annealing. The wafers were exposed to clean room air, and the observation time was, at most, 24 h. In the measurement range of 1000–1300 cm^{-1}, the largest absorption peak was at around 1120 cm^{-1} for the hydrogen-terminated silicon surface and around 1200 cm^{-1} for the atomically flat silicon surface. Although the positions of the peaks for both surfaces are different, the peaks are considered to correspond to the absorption of longitudinal optic vibration due to Si–O–Si asymmetric stretching (LO), where the shift of the peak position of LO, in accordance with a magnitude of oxidation on a hydrogen-terminated silicon surface, has been reported [17]. Furthermore, the peaks that appear around 1060 and 1250 cm^{-1} are considered to be the absorption of transverse optic vibration due to Si–O–Si asymmetric stretching and vibration due to $Si–CH_3$ stretching, respectively [17], [18]. It can be clearly seen from these results that the speed of the native oxide growth on the atomically flat silicon surface is considerably higher than that of the hydrogen-terminated silicon surface. This indicates that the atomically flat silicon surfaces are more easily oxidized in clean room air compared with the hydrogen-terminated silicon surfaces. Therefore, atomically flat silicon surfaces must not be exposed to clean room air but, rather, must be handled in ultraclean N_2/Ar ambience to protect the surface from native oxide growth. Such a "closed-manufacturing system" is ideal for manufacturing atomically flat silicon surfaces [19].

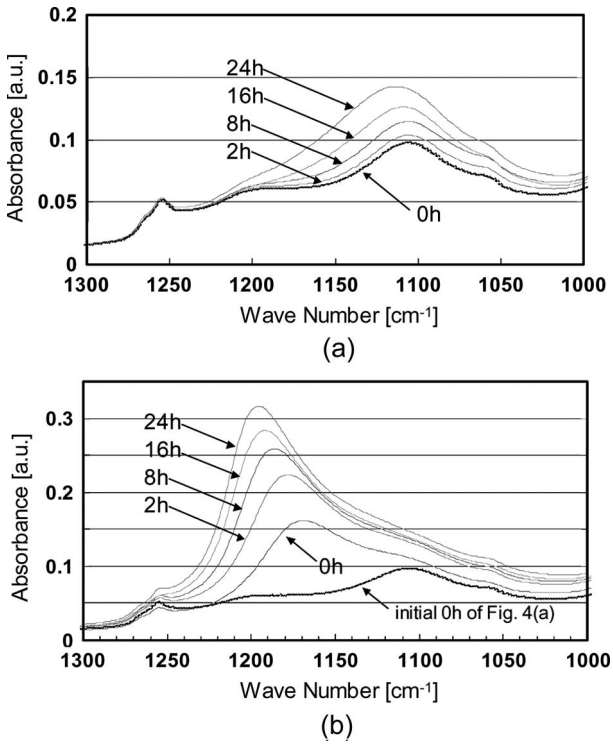

Fig. 4. FTIR-ATR spectra of (a) hydrogen-terminated silicon surface and (b) atomically flat silicon surface after 1200 °C annealing in pure argon ambience. The observation time is, at most, 24 h in clean room air.

III. FORMATION TECHNOLOGY OF AN ATOMICALLY FLAT GATE INSULATOR FILM/SILICON INTERFACE

In this section, we evaluate the flatness of SiO_2 film/silicon interfaces fabricated by various oxidation technologies on atomically flat silicon surfaces. SiO_2 films were formed on the atomically flat silicon surface of boron-doped Cz wafer (Cz-p wafer) by using microwave-excited Kr/O_2 mixture gas plasma oxygen radical oxidation at 400 °C [8], [20], [22], [23] and also by the conventional thermal dry oxidation in oxygen ambience at 900 °C and 1000 °C. The flatness of SiO_2 film/silicon interfaces were measured by AFM after the SiO_2 films were etched with HCl (37%)/HF (50%) mixture and a ratio of 19 : 1 as a very strong acid solution with very low OH^- ion concentration. Subsequently, the silicon surface is not roughened during the etching process of SiO_2 film [21]. Fig. 5(a)–(d) shows the measured results of (a) the initial atomically flat silicon surface and also the silicon surface after HCl/HF treatment to remove the SiO_2 films formed by (b) radical oxidation, (c) thermal dry oxidation at 900 °C, and (d) thermal dry oxidation at 1000 °C. The thickness of the oxide films was 6 nm [Fig. 5(b)], 6 nm [Fig. 5(c)], and 17 nm [Fig. 5(d)] each. It can be clearly seen that the interface formed by the radical oxidation maintains an atomic flatness very similar to the initial surface. On the contrary, for the case of the thermal oxidation at 900 °C and

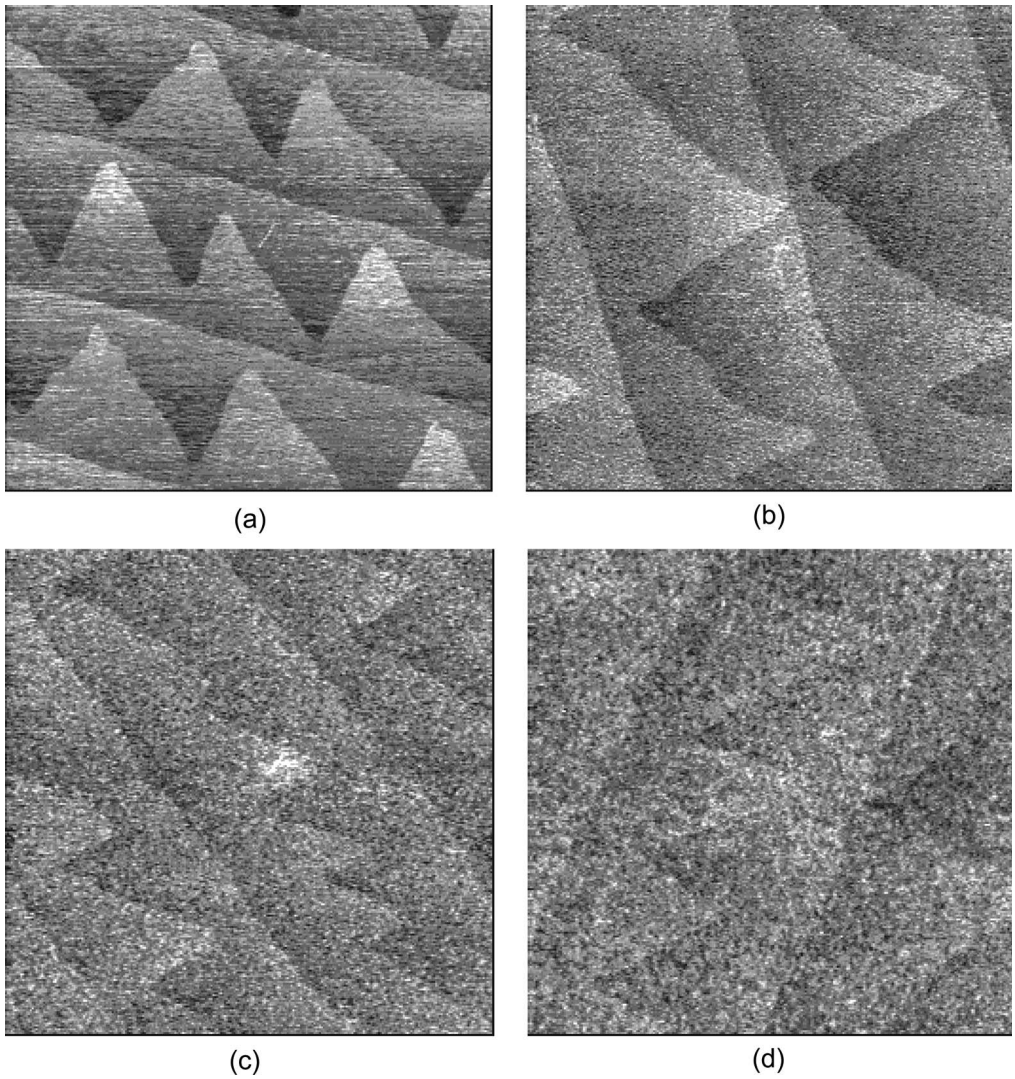

Fig. 5. AFM images, at 3×3 μm, of (a) atomically flat silicon surface after the annealing and (b)–(d) silicon surface after oxide films were etched with HCl/HF solution. Oxide films were formed by (b) radical oxidation for 6 nm, (c) thermal dry oxidation at 900 °C for 6 nm, and (d) thermal dry oxidation at 1000 °C for 17 nm, all on the atomically flat surfaces.

1000 °C, interfaces are obviously roughened by the thermal oxidations.

The reason that the radical oxidation can preserve the atomic flatness of the insulator/silicon interface is considered as follows. It has been reported that radical oxidation using microwave-excited Kr/O_2 mixed gases plasma carried out at 400 °C experimentally shows almost no dependence of the oxidation rate on the crystal orientation [22], [23]. This indicates that the radical oxidation is an isotropic oxidation process. This isotropic oxidation characteristic can also be seen in wet oxidation carried out at very high temperature, such as those higher than 1100 °C. However, a dry oxidation process carried out at 900 °C or 1000 °C exhibits a completely anisotropic oxidation behavior, which is easily understood by the different oxidation rates on various orientation silicon surfaces [22]. In addition, the radical oxidation exhibits a layer-by-layer oxidation process, which is clearly confirmed in the case of (111) orientation silicon surfaces [24]. Thus, due to the nature of the isotropic and layer-by-layer oxidation processes, radical oxidation using microwave-excited Kr/O_2 gases plasma can form an atomically flat insulator/silicon interface when the oxidation is carried out on an atomically flat surface.

Consequently, CMOSFET with an atomically flat interface between a high integrity and ultrathin gate insulator film and silicon surface can be fabricated by the introduction of a radical-reaction-based insulator film formation technology to an atomically flat silicon surface.

Before starting oxidation, atomically flat silicon surface must be cleaned-up by wet chemical cleanings. Conventional ultra-pure water rinse process can not be applied to maintain the atomically flat silicon surface. It must be replaced by 30% IPA (Isopropyl alcohol) added ultra-pure water rinse for the atomically flat silicon surface resulting in a realization of three-step total room temperature wet chemical cleaning before the radical oxidation and the radical nitridation [25]. Absorbed IPA molecules on bare silicon surface are completely eliminated by Kr^+ ion or Xe^+ ion bombardment before starting the radical oxidation/nitridation. The ion bombardment is also necessary to eliminate the surface terminated hydrogen in order to obtain very high integrity SiO_2 and Si_3N_4 films [8].

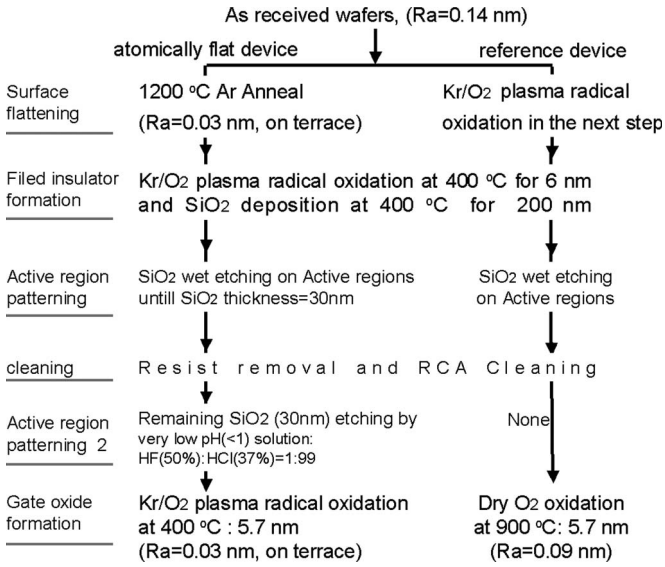

Fig. 6. Process flows up to the gate insulator film formation to fabricate MOS devices with atomically flat interface and the reference.

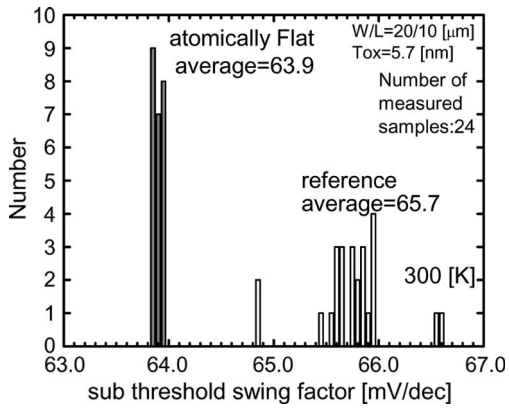

Fig. 7. Distribution of the measured S-factors of the fabricated devices with atomically flat gate insulator film/silicon interface and the reference.

IV. MOS Devices With Atomically Flat Gate Insulator Film/Silicon Interface

P-channel MOSFETs (pMOS) and MOS capacitor with atomically flat gate insulator film/silicon interface were fabricated on an atomically flat Cz-n wafer surface. The radical oxidation technology was utilized for both device-isolation and the gate insulator film formation processes. The detailed process flow is shown in Fig. 6. For reference, MOS devices were fabricated without using the atomic flattening process. Instead, RCA cleaning was used for pre-gate insulator film formation cleaning, and the thermal dry oxidation was used for gate insulator film formation. The thickness of the gate insulator SiO_2 film for both devices was 5.7 nm. Fig. 7 shows the distribution of the measured subthreshold swing factors (S-factor) of the fabricated pMOS devices. The devices with atomically flat gate insulator film/silicon interface exhibit near ideal S-factors with an average value of 63.9 mV/dec. This is smaller than the average value of the S-factors of reference devices, i.e., 65.7 mV/dec. Moreover, the fluctuation of the S-factors in the devices with atomically flat gate insulator film/silicon interfaces is much smaller than that of the reference devices. Fig. 8 shows the $1/f$ noise characteristics of the fabricated pMOS. The noise level is suppressed for about two orders of magnitude due to the atomic flattening of the gate insulator film/silicon interface. This result highlights the correlation between the $1/f$ noise characteristics and the flatness of the gate insulator film/silicon interface and will progress the development of ultralow noise devices [3], [4]. Fig. 9(a) and (b) shows the measured gate current characteristics of the fabricated MOS capacitors and Weibull plots on the dielectric breakdown field intensities $(E_{\rm bd})$, respectively. $E_{\rm bd}$ is increased

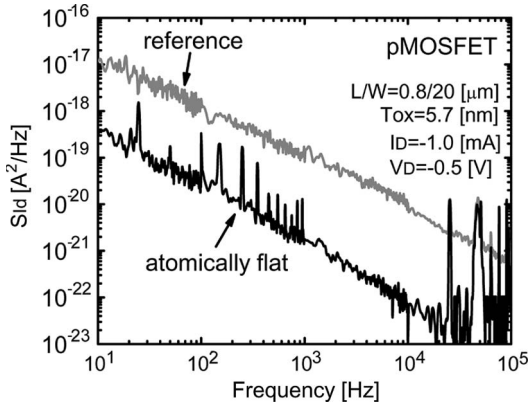

Fig. 8. pMOS $1/f$ noise characteristics, with atomically flat interface and reference. pMOS with atomically flat gate insulator film/silicon interface exhibits very low $1/f$ noise level, about two orders of magnitude lower than that of the reference.

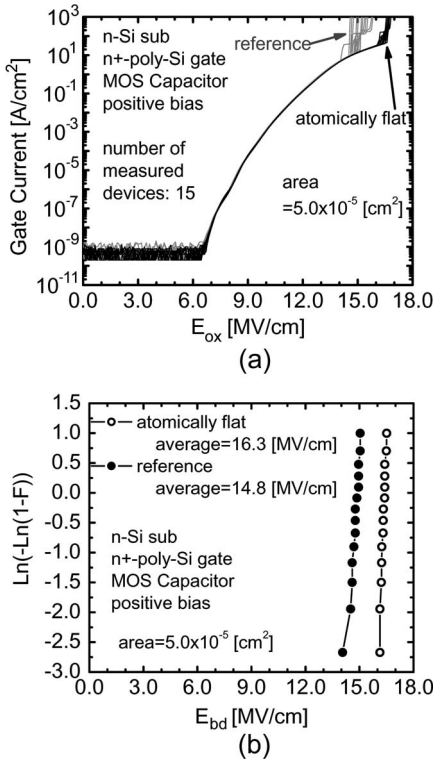

Fig. 9. (a) $J_G - E_{\rm ox}$ and (b) Weibull plot on breakdown $E_{\rm ox}$ intensity $(E_{\rm bd})$ of MOS capacitor with atomically flat interface and the reference. FN-tunneling current characteristic for over 10 dec and a very sharp distribution at high $E_{\rm bd}$ of over 16 MV/cm are obtained due to the atomic flatness at the interface.

up to over 16 MV/cm from 14.8 MV/cm, and a very sharp distribution is obtained for the device with an atomically flat interface.

V. Conclusion

We have developed the technology to fabricate an atomically flat (100) orientation silicon surface on large-diameter wafers. It has been found that the atomic terrace width changes with the off angle of the wafer surface and that the relationship between an atomic terrace width and off angles has been clarified. Moreover, it has been found that the direction of the off angles significantly affects the morphology of an atomically flat surface. When the direction of the off angles is parallel to the $\langle 110 \rangle$ directions, the step structure is composed of straight and triangular steps alternatively. When the direction of the off angles is parallel to the $\langle 100 \rangle$ directions, the step structure is only composed of the straight steps. These findings provide us with very important information regarding the preparation of wafer surfaces, for MOS devices of high performance, and very small electrical characteristic fluctuations. We have successfully fabricated atomically flat silicon surfaces with straight atomic steps and a very uniform terrace width of 140–150 nm on an entire 200-mm-diameter wafer surface with an off angle of $0.051-0.057^\circ$ parallel to the $\langle 100 \rangle$ direction.

The atomically flat gate insulator film/silicon interface can be formed only by the radical-reaction-based insulator film formation technology due to the nature of its completely isotropic and layer-by-layer oxidation/nitridation processes [26]. CMOSFETs, with atomically flat gate insulator film/silicon interfaces, can be fabricated by the combination of this newly developed technology, to atomically flatten a silicon surface using a high-temperature pure argon ambience annealing, and of the radical oxidation/nitridation technology. In comparison with MOS devices of conventional flatness, MOS devices that have been fabricated with an atomically flat gate insulator film/silicon interface exhibit superior characteristics, such as two orders of magnitude suppressed $1/f$ noise characteristic and a very high dielectric breakdown field intensity higher than 16 MV/cm with minor small fluctuations. Consequently, this newly developed technology to atomically flatten the silicon surface and the formation technology of the gate insulator film/silicon interface are both necessary for the fabrication of CMOSFETs of high performance, ultralow noise, and high reliability.

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