Ultra-Low-Temperature Growth of High-Integrity Gate Oxide Films by Low-Energy Ion-Assisted Oxidation

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Ultra-low-temperature growth of high-integrity gate oxide films by low-energy ion-assisted oxidation

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The gate oxide films have been grown at a temperature as low as 450 °C by direct oxidation of silicon. Such a low-temperature oxidation has been realized by employing a precision controlled ion bombardment in an Ar/O_2 mixed plasma for the surface activation. Perfectly controlled Ar ions give the bombardment energy for the oxide film growth. Dielectric breakdown fields of 10 MV/cm are achieved. Integration in a total low-temperature device process has been demonstrated by fabricating self-aligned Al-gate metal-oxide-silicon field effect transistor (MOSFET) formed without any heat processing over 450 °C. The precise control of the ion bombardment is quite essential for the low-temperature process.

As semiconductor devices are scaled down to smaller dimensions, conventional device process temperatures such as 900 °C will tend to become incompatible with the desired device designs. For example, high-temperature oxidation changes the impurity profiles previously formed in the substrate. Moreover, high stress in oxide films caused by the difference in the thermal expansion of Si and other films causes wafer bending, film cracking, and defect formation in the underlying Si. Thus low-temperature semiconductor device fabrication techniques are needed to prevent these problems.[1]

We have already reported silicon epitaxy at 250 °C[2] and a high integrity ion implanted region by 450 °C furnace annealing.[3] In order to realize a low-temperature Si epitaxial growth, Ar ion bombardment of a growing silicon film surface in a very-low-energy regime is utilized to activate the surface layer. 450 °C furnace annealing is realized by metallic contamination free implantation obtained by Si capping of the inner surface of the implanter. These technologies are the key to establish a total low-temperature ultra-large-scale integration (ULSI) manufacturing. But only the low-temperature gate oxidation has not yet been realized.

Recently, the low-temperature formation of silicon gate oxide films has been extensively studied using various methods such as sputter deposition,[4,5] silicon oxidation in an oxygen plasma,[6] thermal oxidation,[7] chemical vapor deposition[8] and liquid phase deposition.[9] We have investigated the formation of a high-quality gate oxide film by employing a high-precision-controlled ion assisted process similar to the low-temperature silicon epitaxy process. In this letter, we discuss a low-temperature gate oxidation process at a temperature as low as 450 °C by direct oxidation of silicon.

The apparatus used for the low-energy ion-assisted process is a dual-frequency-excitation plasma process system[10] which is shown in Fig. 1. This system is characterized by a precise and independent control of the ion energies and the ion flux bombarding the wafer surface. This is achieved by adjusting the rf power inputs from the upper and the substrate electrodes. The upper rf power supply is employed to generate a high density plasma using a magnetron discharge to control the ion flux density. The substrate rf power supply is employed to generate a self-bias onto the wafer surface to control the assisting ion energy. In this experiment, the wafer surface is oxidized in an Ar/O_2 mixed plasma at the temperature of 450 °C. The Ar and O_2 flow rates are 300 and 8 sccm, respectively. The upper electrode has an input of 100 MHz rf (100 W) for controlling the Ar plasma density. The wafer electrode has an input of 41 MHz rf (2 W) for controlling the bombarding Ar ion energy onto the wafer surface. Under these conditions, the flux density of the Ar ion and the ion energy at the wafer surface are 9.7×10^{15} atoms/cm^2 s and 15 eV, respectively. The Ar ion bombardment condition assists the oxidation of silicon (low-energy ion-assisted oxidation). The system has an oil-free magnetic suspension type turbomolecular pump (TMP) for the vacuum system, and the inner surface of this chamber and gas delivery system are electropolished and oxide passivated in order to minimize the outgassing. As a result, a background pressure of 10^{-10} Torr is achieved.

Figure 2 shows the time dependence of the oxide thick-

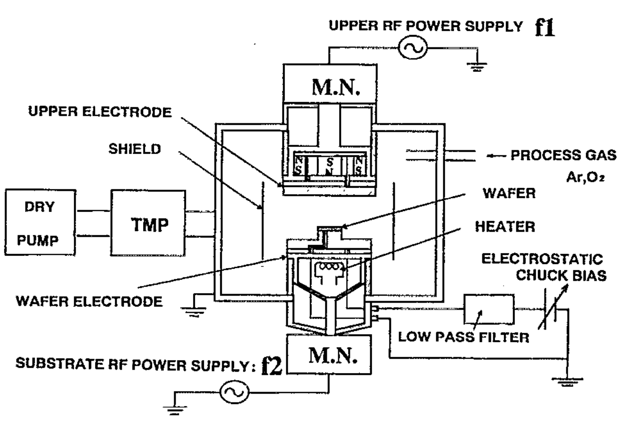

FIG. 1. Schematic of the dual-frequency excitation plasma process equipment.

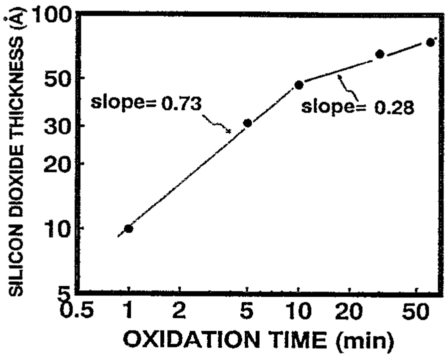

FIG. 2. Oxide thickness as a function of oxidation time at 450 °C.

ness during low-energy ion-assisted oxidation for n-Si (100) at 450 °C, where the oxide thickness is determined by XPS. The growth rate slope is given by 0.73 at the initial growth up to 50 Å. It indicates that the growth of the oxide film is both Si-SiO_2 interface reaction controlled and diffusion controlled in the SiO_2 film. The growth rate slope is 0.28 for an oxide thickness greater than 50 Å. The growth of this oxide film is considered to be according to the Cabrera–Mott model.

The plot of the oxide thickness against the reciprocal temperature ($1/T$) is given in Fig. 3. The thermal activation energy of the low-energy ion assisted oxidation is 0.025 eV calculated from this plot. The value is lower than the activation energy of thermal oxidation (about 1.5 eV). This indicates that this oxidation is dominantly activated by the ion bombardment.

Figure 4 shows the dielectric breakdown histograms of MOS [Al/SiO_2/n-Si(100)] diodes for a low-energy ion assisted oxide [Fig. 4(a)] and a dry oxide at 1000 °C [Fig. 4(b)]. A dielectric breakdown field of 10 MV/cm is achieved for the 450 °C oxidation. Furthermore, the breakdown-field distribution of the low-energy ion-assisted oxidation is similar to that of the thermal oxidation.

Figure 5 shows the energy barrier height at the oxide/silicon interface for electron emission from the silicon to the oxide, which is derived from the Fowler–Nordheim tunnel-

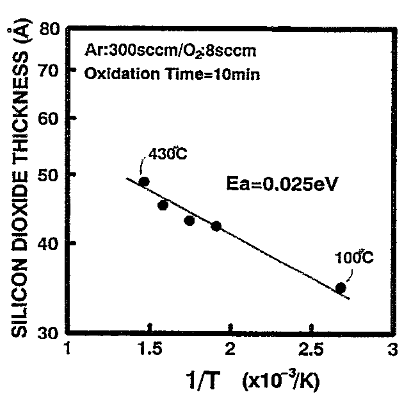

FIG. 3. Arrhenius plot of oxide thickness at the temperature from 100 to 430 °C. Oxidation time is 10 min.

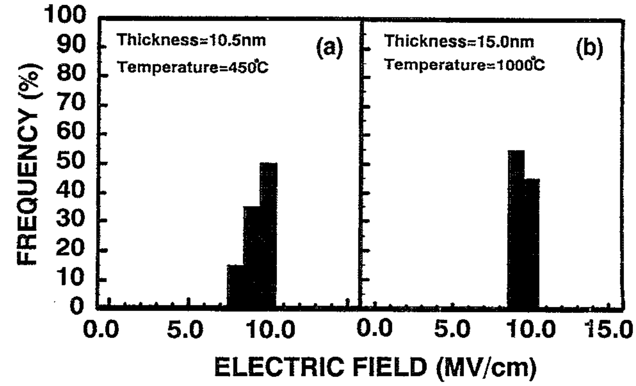

FIG. 4. Dielectric breakdown characteristics of low-energy ion assisted oxide film (a) and thermal oxide film (b). Low-energy ion assisted oxide film is 10.5 nm thick. The thermal oxide film having a 15 nm thickness is formed by dry oxidation at 1000 °C. The judgment current is 1.0×10^{-4} A and the area of the electrode is 1.69×10^{-4} cm^2.

ing current in the current density-average electric field characteristics of MOS [Al/SiO_2/n-Si(100)] diodes under the positively biased metal electrodes. The barrier height of the thermal oxide film formed at 1000 °C is 3.2 eV, while that of the low-energy ion assisted oxide film is 3.16 eV. This value indicates that the quality of the low-energy ion assisted oxide is close to that of the thermal oxide.

Figure 6 shows the drain current-drain voltage characteristics of a self-aligned Al-gate MOSFET formed without any heat processing over 450 °C by the low-energy ion assisted oxidation and the 450 °C ion implanted region annealing. The thickness of this gate oxide is 8.5 nm, where the channel length and the channel width are 10 and 50 μm, respectively. The fluctuation of the threshold voltage is limited to within 20 mV. But it is confirmed that this Al-gate MOSFET can be operated even at a gate voltage as high as 5 V.

It is concluded that the precise control of the ion energy and the ion flux density is quite essential for the low-temperature gate oxidation by low-energy ion bombardment plasma process. Though the oxide film quality is poor com-

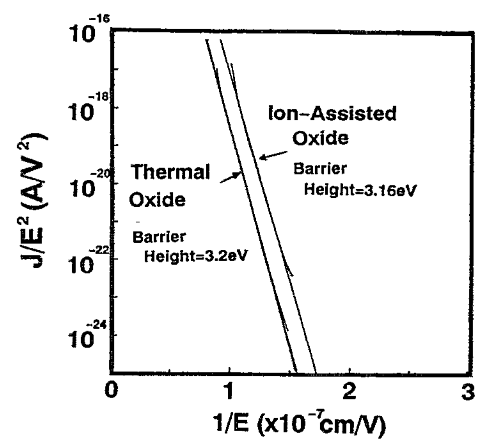

FIG. 5. The Fowler–Nordheim plots of the current through the oxide formed by a low-energy ion assisted and a thermal (1000 °C dry oxidation) process.

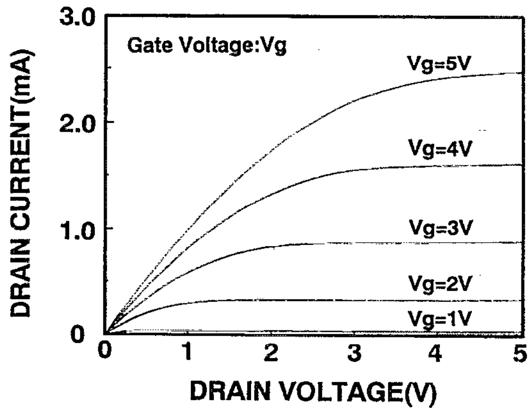

FIG. 6. Drain current–drain voltage characteristics of Al-gate MOSFET formed without any heating process over 450 °C by low-energy ion assisted oxidation. The gate oxide thickness is 8.5 nm and the channel length 10 μm, and the channel width 50 μm.

pared to that of the thermal oxide film, it is speculated that the bombarding ion energy down to several electron volts with an accompanying increase of the bombarding ion flux density will improve the film quality further.

This study was carried out at the Mini Super Clean Room of the Faculty of Engineering, and the Super Clean Room of the Laboratory for Microelectronics, Research Institute of Electrical Communication, Tohoku University.

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