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Very thin oxide film on a silicon surface by ultraclean oxidation

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Very thin oxide films with a high electrical insulating performance have been grown by controlling preoxide growth using the ultraclean oxidation method. The current level through the ultraclean oxide is lower than that through the conventional dry oxide including thicker preoxide. The barrier height at the silicon-oxide interface for electrons emission from silicon to oxide for the ultraclean oxide is little decreased as the thickness is thinner, while the barrier height for conventional dry oxide is drastically decreased. The growth rate of ultraclean oxide at 900 °C is governed by a simple parabolic law even in the range of 5–20 nm.

The electrical insulating performance of very thin gate oxide films is one of the crucial factors that dominate the rate and the limitation of shrinking ultralarge scale integrated (ULSI) devices. As the gate oxide gets thinner, the current through the oxide increases and the scaling down of metal-oxide-semiconductor (MOS) ULSI devices will be limited. It is important to clarify factors dominating the current level through very thin oxide films in order to extend the limitation of gate oxide films.

The presence of native oxide (preoxide) in very thin gate oxide films may induce the degradation of the electrical insulating performance. We have investigated the control factors of native oxide growth on the cleaned silicon surface, and have found that the coexistence of oxygen and water (or moisture) is required to grow native oxide on silicon both in air and in ultrapure water at room temperature.[1–4] We have also demonstrated that the average thickness of native oxide (preoxide) formed during the wafer heating up to thermal oxidation temperature can be controlled within a monolayer oxide thickness by extreme lowering of the moisture concentration in argon gas.[5] In this letter, we describe the very thin thermal oxides with high electrical insulating performance by controlling oxide layer growth during the wafer heating-up period right before thermal oxidation.

Very thin oxide films were formed using ultraclean oxidation characterized by extremely low moisture and extremely low metal impurity concentrations in the oxidation environment.[6–9] In this ultraclean oxidation system, the thickness of the preoxide can be controlled, because the wafer can be heated up to thermal oxidation temperature in one atmospheric argon gas with extremely low moisture concentration. The desorption of hydrogen from the HF cleaned silicon surface is demonstrated to start at about 300 °C and the silicon surface consequently reacts with impurities (oxygen or moisture) at temperatures higher than 500 °C.[10] In this experiment, the HF cleaned wafers were heated up to 300 °C in argon gas at the rate of 50 deg/min, and then were intentionally oxidized at 300 °C in an ultraclean oxygen gas for 30 min to form one oxide molecular layer as a passivation layer.[11] The wafers were again heated up to the thermal oxidation temperature of 900 °C in the ultraclean argon gas to prevent preoxide growth and an increase of surface microroughness. Figure 1 shows Si_{2p} x-ray photoelectron spectroscopy (XPS) spectra of oxide grown during heating the wafer up to 900 °C. The oxide thickness (0.4 nm) of the ultraclean is the same as that intentionally formed at 300 °C as a passivation layer, because oxide growth hardly progresses during the heating-up from 300 to 900 °C in the ultraclean argon gas. The thickness of oxide grown during the wafer loading into a conventional furnace is 1.4 nm. This result proves that the preoxide growth can be precisely controlled by the ultraclean oxidation method.

Figure 2 shows the time dependence of oxide thickness at 900 °C by ultraclean oxidation, where the oxide thicknesses were determined by XPS calibrated with ellipsometry for oxides with thicknesses thinner than 14 nm or by ellipsometry for the others.[3] The oxide growth obeys a simple parabolic law. The kinetics of ultraclean oxidation can be explained by the Deal–Grove model even for oxide thicknesses thinner than 30 nm,[12–14] where the parabolic rate constant B (diffusion controlled) determined from plot of Fig. 2 is $2.3\times10^{-4}\ \mu m^2/h$. This result suggests that the preoxide is located on the outer surface of thermal oxide.

Figure 3 shows the current density-average electric field characteristics of metal-oxide-semiconductor (MOS) diodes with n^+-polycrystalline silicon/oxide/p-silicon(100) structure under the negatively biased metal electrodes for 5.5 nm thick oxide films. The current level through the ultraclean oxide is lower than that through the conventional dry oxide over the range. The current of the ultraclean oxide over the range and of the conventional dry oxide at the average electric field higher than 8.8 MV/cm is considered to be dominated by the Fowler–Nordheim tunneling of electrons from n^+-polycrystalline silicon to oxide, because the barrier height for electrons tunneling at n^+-polycrystalline silicon/oxide interface is lower than that for holes tunneling at oxide/p-silicon. This result exhibits that the barrier height of electrons tunneling at n^+-polycrystalline silicon /oxide interface for the ultraclean oxide is higher than that for conventional dry oxide. At the average electric field lower than 8.8 MV/cm, the leakage current is easy to be observed in the conventional dry oxide. The current through conventional dry oxide is in-

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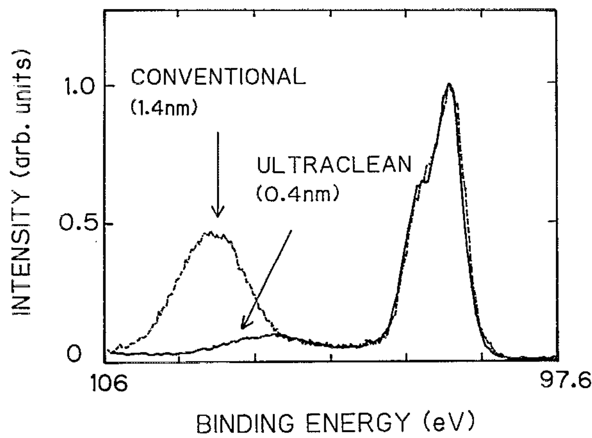

FIG. 1. Si_{2p} XPS spectra of oxides grown during the wafer heating up period right before thermal oxidation.

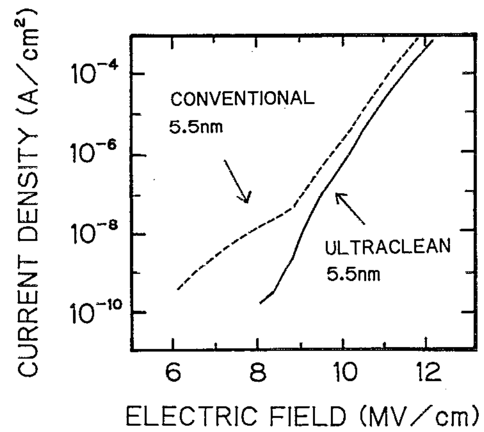

FIG. 3. Current density-average oxide field characteristics of n^+-polycrystalline silicon/oxide/p-silicon(100) diodes with 5.5 nm thick oxide under negatively biased metal electrodes.

creased at the low-field region as the thickness is thinner. The current level through ultraclean oxide is not significantly increased even for 5.5 nm thick oxide. In fact, the current density-average electric field characteristics for 5.5 nm is nearly overlapped on that for 9.0 nm only in ultraclean oxide. The leakage current is also speculated to result in electron conduction from the barrier height for electron at n^+-polycrystalline silicon/oxide interface being low compared with that for hole at oxide/p-silicon. Therefore, these current level differences can be concluded to be caused by the presence of preoxide located at the outer surface of thermal oxide.

Figure 4 shows the energy barrier height at oxide/silicon interface for electrons emission from silicon to oxide as a function of oxide thickness, which is derived from the current dominated by Fowler–Nordheim tunneling in the current density-average electric field characteristics of aluminum/oxide/n-silicon(100) MOS diodes under the positively biased metal electrodes. Although the barrier height for conventional dry oxide is drastically decreased as the thickness is thinner, the barrier height for ultraclean oxide is little decreased and is higher than 2.9 eV for 5.1 nm oxide. The current level through the ultraclean oxide with the thickness of 5.1 nm is actually lower than that through conventional dry oxide. This result probably implies that the barrier height for the conventional dry oxide is apparently low because the current is due to Frenkel–Poole emission along with Fowler–Nordheim tunneling, or that the oxidation mechanism is influenced by the presence of the preoxide located at the outer surface of thermal oxide which consequently gives a different oxide structure near the oxide/silicon interface from that of the ultraclean oxide. Further investigation is, however, necessary to clarify the factor dominating the barrier height.

The threshold voltage shift of metal-oxide-semiconductor field-effect transistor (MOSFET) by the injection of hot electrons from substrate silicon into the oxide was also evaluated,[15,16] where the channel length is 48.4 μm and the channel width 100 μm. The threshold voltage shifts of ultraclean and conventional dry oxides with the thickness of 5.6–5.7 nm are 0.4 mV for the number of injected electrons of 1.3×10^{17} cm^{-2}. For 9.0 nm, the shifts of ultraclean (9.7 nm) and conventional dry (9.3 nm) oxides are 3 and 16 mV for the injected electrons of 1.3×10^{17} cm^{-2}, respectively. The ultraclean oxide has higher reliability compared with the conventional dry oxide. This result also manifests that the reliability of oxides is enhanced as the thickness gets thinner.

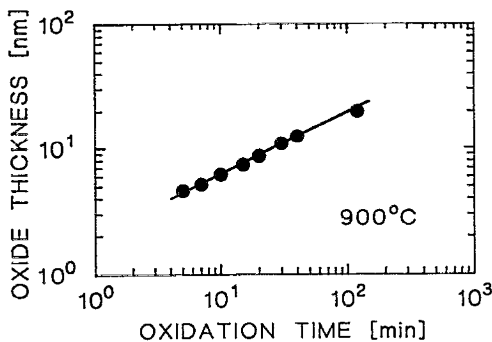

FIG. 2. Oxide thickness as a function of thermal oxidation time at 900 °C.

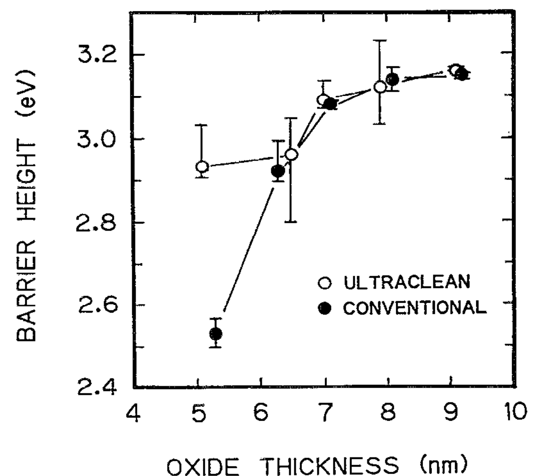

FIG. 4. Energy barrier height at silicon-oxide interface for electrons emission from silicon to oxide as a function of oxide thickness.

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In conclusion, we have demonstrated that the very thin ultraclean oxide formed by controlling the preoxide growth during the wafer heating up before thermal oxidation has high electrical insulating performance and high reliability. The preoxide layer grown by the heating up causes to decrease the energy barrier height for electrons emission at metal-oxide and oxide-semiconductor interfaces. This work also suggests that further investigation of thinner gate oxide with high electrical insulating performance is essential to realize the further ULSI devices, because the reliability of thinner oxides is guaranteed to be high.

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