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Low-temperature silicon epitaxy by low-energy bias sputtering

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Bias sputtering at low energies, i.e., comparable to typical crystal interatomic binding energies, has been utilized to control the kinetics of thin-film growth. It was found that the crystallographic structures of sputter-deposited silicon films are drastically changed by the energy of ions incident at the substrate. As a result, formation of high quality epitaxial silicon films on (100) silicon substrates has been realized at such low temperatures as 320–350 °C. At the same time, low-temperature impurity doping of the epitaxial layer has been also demonstrated. Furthermore, the low-energy bias sputtering process has made it possible to perform very effective substrate surface cleaning at extremely low temperatures without introducing any damage to the substrate.

The most essential requirement for future ultralarge scale integration (ULSI) fabrication with lower submicron design rules is the high precision control of processes as well as the realization of low-temperature processing. The growth of silicon epitaxial films at low temperatures is of particular importance for fabricating ULSI devices because of the necessity for precise impurity profile control.

Epitaxial growth of silicon is usually performed using chemical vapor deposition (CVD) technologies. However, they require high-temperature heat cycles typically over 1000 °C for film deposition and also for substrate surface cleaning. Recently, high quality epitaxial silicon was grown at 600 °C with a large deposition rate by surface reaction film formation technology utilizing free-jet molecular flow.[1,2] Low-temperature silicon epitaxy below 400 or 730 °C has also been reported using ion beam technologies, such as partially ionized vapor deposition[3] or ionized cluster beam deposition,[4] respectively. However, in these processes the energies of ions or ionized clusters are in the range of keV's, which is much higher than the typical crystal interatomic binding energies. This means that these processes can cause damage in the underlying substrates or devices. Furthermore, since the effective interaction of ions with constituent atoms at the surface layer of thin films is expected to occur with much lower energies, it is more desirable to use ion beams in which all accelerated particles have a well-defined kinetic energy comparable to crystal interatomic binding energies. The purpose of this letter is to present new results on the formation of high quality epitaxial silicon films at low temperatures below 350 °C by a newly developed low-energy bias sputtering process.

The deposition of silicon films was carried out using an rf-dc coupled mode bias sputtering system[5] illustrated in Fig. 1. A 100 MHz rf power supply was employed to generate a high density Ar plasma at low pressures ($\sim 10^{-3}$ Torr), and two dc power supplies are provided to control the target and the substrate bias voltages independently. Therefore, the ion energies incident on the target and the substrate are determined by the two dc bias voltages, while the ion flux is adjusted by changing the rf power input. As a result, the experimental technique has enabled the independent and precise control of various important process parameters, such as energy and flux of ions incident on growing film surfaces and film growth rates. Such a versatile feature in the thin-film growth process has been successfully applied to the formation of high quality aluminum films[5] and copper films.[6]

The entire system was constructed based on the philosophy of ultraclean technology,[7] i.e., oil-free ultrahigh vacuum exhaust system and ultraclean gas delivery system[8] were employed. As a result, the impurity levels in Ar gas as low as several ppb or below (mainly H_2O) and a base pressure for the main vacuum chamber of 2×10^{-10} Torr were achieved.

n-type (100) silicon wafers of 5–8 Ω cm resistivity were used as substrates. The wafers were precleaned by conventional wet-chemical processes: boiling in H_2SO_4/H_2O_2 solution, rinsing in ultrapure water, diluted HF etch, and drying in isopropyl alcohol vapor. After being dried, a wafer was immediately set in the loading chamber, which was evacuated to 10^{-7} Torr by a turbomolecular pump, and then transported to the sputtering chamber via load lock. After raising the wafer temperature to 350 °C, the surface of the wafer was bombarded with low-energy Ar ions for substrate surface cleaning. *In situ* surface cleaning by preheating at higher

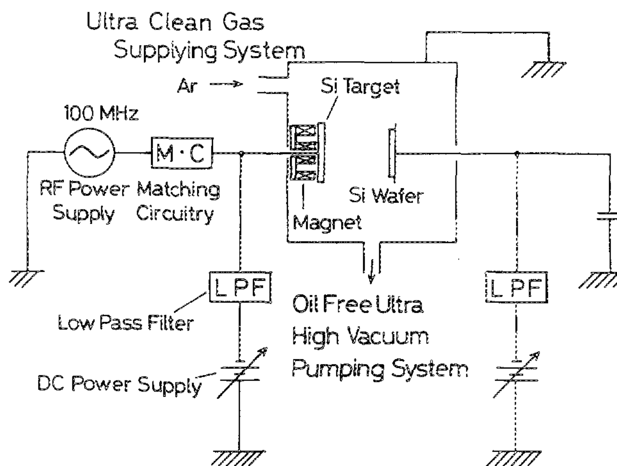

FIG. 1. Schematic of the rf-dc coupled mode bias sputtering system used for Si film deposition by low-energy bias sputtering process.

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temperatures was not employed. About 0.5-μm-thick films were deposited on the substrate, using a floating-zone (FZ) silicon block phosphorus doped to 3×10^{18} cm^{-3} as a target. The typical film formation conditions were as follows: the Ar gas pressure of 8×10^{-3} Torr; the rf power of 40 W; the target bias voltage varied from -100 to -400 V; and the substrate bias voltage varied from $+15$ to -15 V. The typical deposition rate at a target bias voltage of -300 V is about 2 Å/s, which is substantially constant for substrate bias voltages in the range of $+15$ to -15 V.

Figure 2 shows the reflection electron diffraction patterns obtained from silicon films deposited on (100)Si with a target bias of -300 V for varying substrate bias voltages. The dramatic effect of kinetic energies of ions impinging on the growing silicon films is clearly demonstrated in the figure. At a substrate voltage of $+10$ V, the deposited film is polycrystalline with a preferred orientation [Fig. 2(a)]. However, at substrate voltages between 0 and -5 V, epitaxial growth of (100) single-crystal films was observed as seen in Fig. 2(b). The homoepitaxial growth was also verified by the lattice image observation using high-resolution cross-sectional transmission electron microscopy. An increase in the ion energy by increasing the negative substrate bias to -10 V altered the film structure to highly oriented polycrystalline silicon as shown in Fig. 2(c). Further increase in the bias to -15 V resulted in fine-grain polycrystalline silicon without any preferred orientation [Fig. 2(d)]. The series of diffraction pattern observations described above clearly demonstrates that various crystalline structures of the deposited silicon film can be obtained by controlling the energy of ions incident on the growing film surface.

The dependence of crystal structure on the combination of a target bias (V_t) and a substrate bias (V_s) is summarized in Fig. 3. Various regions representing the occurrence of different crystal structural conditions, such as polycrystalline silicon, single-crystal silicon, and amorphous silicon, are indicated in the figure. The current-voltage characteristics of the target and the substrate electrodes under varying bias conditions were measured, which made it possible to estimate the plasma potential variation as a function of V_s and V_t. Three solid lines in the figure were generated from these measurements showing the combination of V_s and V_t which gives an identical potential difference between the plasma and the wafer, viz., an identical ion energy for bombarding wafer surfaces. The energy values given in the figure are only the estimated values, since the absolute value of plasma potential is not exactly known. The excellent coincidence of these lines to the regions representing specific structural conditions shows that the crystalline form is primarily determined by the ion bombardment energy. At lower ion energies, insufficient energy is transferred to the deposited Si atoms, thus resulting in polycrystalline silicon films. With an optimum ion energy transfer, it appears possible to grow single-crystal Si films. When the energy is increased above the optimum value, the damage effect of ion bombardment predominates and the film structure changes sequentially to highly oriented polycrystalline silicon, fine-grain polycrystalline silicon, and amorphous silicon. The total number of ions bombarding the film surface would also influence the crystalline form developed. The study on the effect of ion flux on the crystal structure is under way and will be presented elsewhere.

The reflection electron diffraction pattern showing single-crystal silicon in Fig. 2(b) is not as good as that obtained from the substrate silicon, implying defect formation in the film. Wright etch observation of the sample as well as the

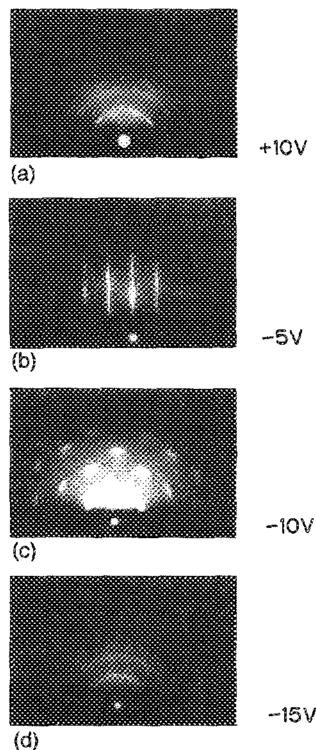

FIG. 2. Reflection electron diffraction patterns from Si films deposited on (100)Si for varying substrate bias voltages as indicated in the figure. The target bias is -300 V for all samples.

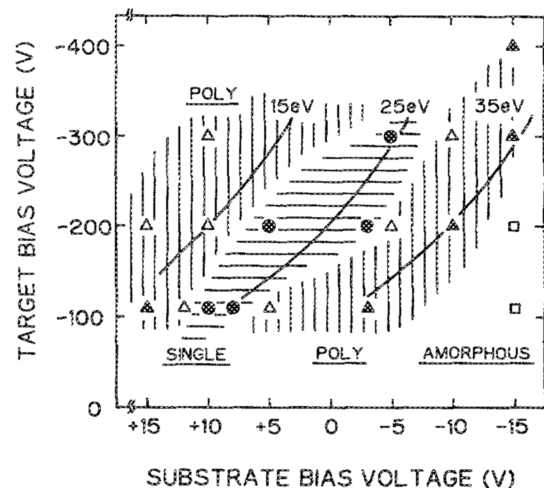

FIG. 3. Dependence of silicon film structure on target bias (V_t) and a substrate bias (V_s). The solid lines represent combinations of V_t and V_s giving constant ion-bombardment energy. (⊗) single crystal, (△) polycrystal (preferred orientation), (▲) polycrystal (random orientation), (□) amorphous.

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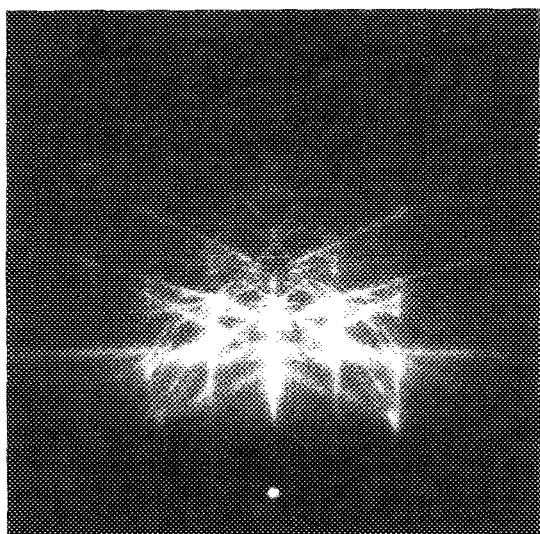

FIG. 4. Reflection electron diffraction pattern obtained from a Si film deposited with an optimized substrate surface cleaning condition. The silicon surface was subjected to Ar ion bombardment for 5 min with $V_t = -25$ V, $V_s = +7$ V and rf power of 5 W before the silicon deposition.

cross-sectional transmission electron microscope (TEM) observation revealed that a high density of defects existed in the film, which has been attributed to improper surface cleaning performed prior to the film growth.

Figure 4 shows the reflection electron diffraction pattern obtained from a deposited silicon film for which we employed an optimized surface cleaning condition as described in the figure caption. A diffraction pattern with strong Kikuchi lines clearly shows the crystal perfection of the film. We failed to find any defects by scanning electron microscope (SEM) observation of the sample surface after Wright etching. The result strongly suggests that a very thin layer of native oxide or adsorbed molecular layers of moisture or other gas molecules in the air have been very effectively removed at low temperatures by the low-energy ion bombardment. Further discussion on the optimization of the surface cleaning process will be presented in a separate article.[9]

The electrical resistivity of the single-crystal layer obtained with the optimum condition was measured to be 0.023 Ω cm, while that of the target silicon block is 0.013 Ω cm. The data suggest that approximately 20–30% activation of impurities was achieved at a low substrate temperature of 320–350°C. However, it is not clear at present whether the reduced concentration of activated impurities is due to the deactivation of incorporated phosphorus atoms, or the reevaporation of impurity atoms during the film growth process.

In conclusion, very low temperature silicon epitaxy with simultaneous impurity doping as well as damage-free, low-temperature substrate surface cleaning has been established by a low-energy bias sputtering process. It is concluded that this process will definitely play essential roles in the fabrication of ULSI devices requiring high precision control of processes at low temperatures.

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