Switching delay of a nonlatching Josephson gate evaluated from ring oscillator operation

doi: 10.1109/77.740684

Switching Delay of a Nonlatching Josephson Gate Evaluated from Ring Oscillator Operation

Yoshinao Mizugaki, Koji Nakajima, and Akira Shoji

***Abstract*— The authors present the experimental results for the switching delay of a dc-biased nonlatching Josephson gate (a coupled-superconducting quantum interference device gate). The measurement is executed by the use of a ring oscillator (RO) method. A frequency-to-voltage converter is used to evaluate the oscillation frequency of the RO. The circuit is designed and fabricated using a 2.5-kA/cm^2 Nb/AlO$_x$/Nb Josephson junction technology. The results show the minimum switching delay of 18 ps.**

***Index Terms*—Circuit testing, dc-biasing, Josephson logic, nonlatching Josephson gate, ring oscillator, superconducting circuits, switching delay.**

I. Introduction

RECENTLY, several dc-biased nonlatching Josephson digital circuits have been developed to prevent the problems in ac-biased latching Josephson circuits [1], [2]. A coupled-superconducting quantum interference device (C-SQUID) gate is one of such dc-biased Josephson devices [3]. We have reported low-speed testing of the C-SQUID applications to a 3-bit neuron-based A/D converter [4] and a flip-flop [5] fabricated on Nb/AlO$_x$/Nb integrated circuits. We have also investigated the high-speed performance numerically, of which the results indicate that the single C-SQUID gate can operate with the high-speed clock up to several tens of GHz [5]–[7]. Evaluation of the C-SQUID performance should be followed by high-speed testing.

In this paper, we experimentally evaluate the switching delay of the C-SQUID gates by the use of a ring oscillator (RO) method. The oscillation frequency is converted to a dc voltage by a frequency-to-voltage converter (FVC), in which single-flux-quantum (SFQ) transitions and the Josephson voltage-frequency ($\langle V\rangle$-f) relations are employed. Though it is not direct measurement of the oscillation, this method gives us accurate information on the oscillation frequency, as the dc-voltage evaluation used in the SFQ circuitry [8].

II. Design and Simulation

Fig. 1 shows the schematic diagram of the circuit. The circuit is composed of a five-stage RO, a Buffer, and an FVC.

Manuscript received April 28, 1998; revised August 3, 1998. This work was performed through Special Coordination Funds for promoting Science and Technology of the Science and Technology Agency of the Japanese Government.

Y. Mizugaki and K. Nakajima are with the Laboratory for Electronic Intelligent Systems, Research Institute of Electrical Communication, Tohoku University, Sendai 980-8577, Japan.

A. Shoji is with the Electrotechnical Laboratory, Tsukuba 305-8568, Japan.

Publisher Item Identifier S 1051-8223(98)09477-9.

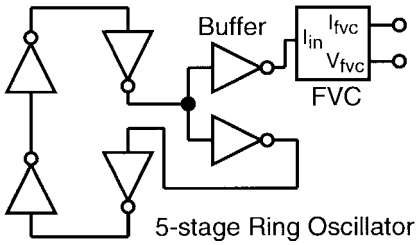


Fig. 1. Schematic diagram of the circuit.

The RO and the Buffer comprise the C-SQUID inverter gates. Details of the C-SQUID gate are described in our previous papers [3], [5]. Only shunt resistance is changed according to the specific capacitance of 5.5 fF/cm^2 [9]. The load resistor value of each C-SQUID gate is 0.39 Ω.

The oscillated output current of the RO drives the FVC through the Buffer gate. The equivalent circuit of the FVC is shown in Fig. 2(a). It has the qualitatively same structure as the dc-to-SFQ converter used in the RSFQ circuits [10]. Each junction of the FVC is resistively shunted to obtain a McCumber parameter as small as 0.5 to avoid undesirable resonance.

Fig. 2(b) shows the calculated threshold characteristics of the FVC. If the bias current ($I_{\rm fvc}$) is in the range of about 0.1–0.2 mA, an SFQ enters the superconducting loop through the grounded junction when the input current ($I_{\rm in}$) is on. The loop cannot store the SFQ without $I_{\rm in}$, and hence, the trapped SFQ exits the loop through the other junction when $I_{\rm in}$ is off. That is, a sequence of the injection and extraction of an SFQ occurs at one oscillation period. The frequency of this SFQ injection/extraction sequence can be measured as a dc average voltage of the junction ($\langle V_{\rm fvc}\rangle$). According to the Josephson $\langle V\rangle$-f relation, $\langle V\rangle = \Phi_0 f$, we can obtain the oscillation frequency from $\langle V_{\rm fvc}\rangle$. ($\Phi_0$ is the flux quantum.)

Fig. 3(a) shows the numerical circuit operation simulated by the use of JSIM [11]. At the rising edge of $I_{\rm in}$, an SFQ voltage pulse is generated at the $V_{\rm fvc}$ terminal. Fig. 3(b) shows the simulated dc current-voltage ($I_{\rm fvc}$-$\langle V_{\rm fvc}\rangle$) characteristics. A voltage step is observed in the $I_{\rm fvc}$-$\langle V_{\rm fvc}\rangle$ characteristics when the RO is on. The voltage step corresponds to the averaged SFQ voltage pulses. The average switching delay (τ_d) of the single C-SQUID gate can be calculated from the step voltage ($V_{\rm step}$). The RO has five C-SQUID inverters, that is, ten switching stages for one oscillation period. Then the average switching delay is expressed as $\tau_d = \Phi_0/(10 \times V_{\rm step})$. In this case, $V_{\rm step}$ and τ_d are 8.3 μV and 25 ps, respectively. The

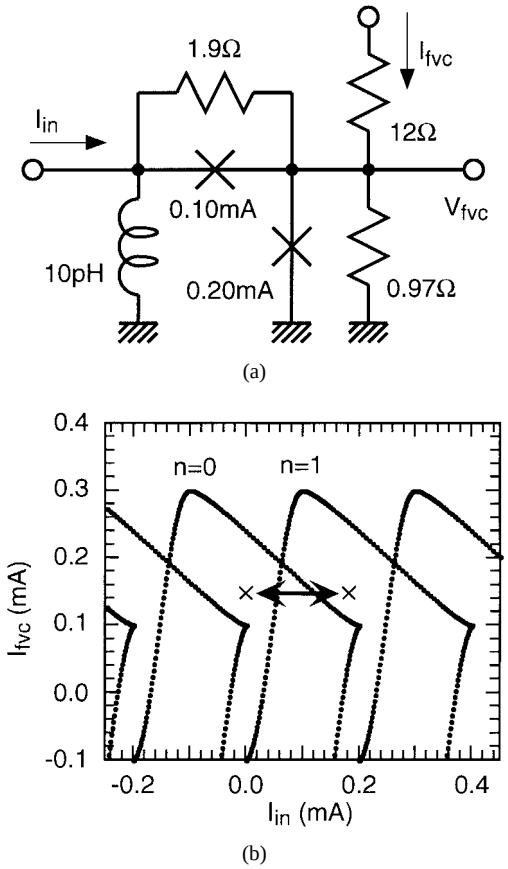


Fig. 2. FVC. (a) Equivalent circuit. (b) Calculated threshold characteristics.

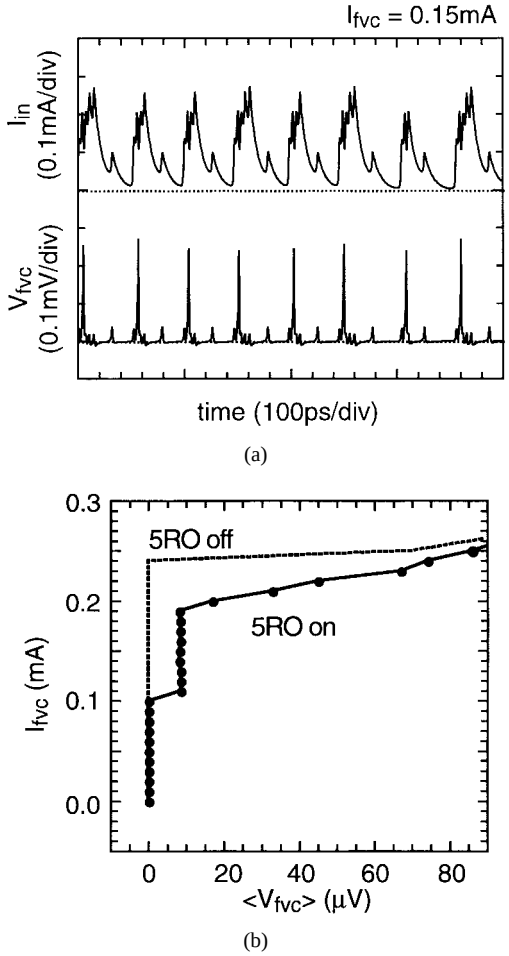


Fig. 3. Simulated results of the circuit operation. (a) Transitional wave forms. The RO and the Buffer are biased up to 90% of their critical current. The load inductance and resistance are 2.0 pH and 0.39 Ω, respectively. (b) $I_{\rm fvc}$-$\langle V_{\rm fvc}\rangle$ characteristics of the FVC.

voltage step appears in the $I_{\rm fvc}$ range of 0.11–0.19 mA. That is, the margin of $I_{\rm fvc}$ is as wide as ±27%.

III. Experiment

Fig. 4 shows a microphotograph of the circuit, which was fabricated at NEC Corporation using their standard 2.5-kA/cm^2 Nb/AlO$_x$/Nb process [12]. The experiment was performed at 4.2 K in a helium-dewar inserted with double μ-metal shields.

Fig. 5 shows the measured threshold characteristics of the test elements for the FVC and the C-SQUID gate. From Fig. 5(a), the fabricated inductance value is estimated as 5.8 pH, which is about 60% of the designed value. The parameters of the C-SQUID gate are also estimated as $\beta_1 = 0.3$ and $\beta_2 = 0.5$, which are larger than the designed values [3], [5].

Fig. 6 shows the $I_{\rm fvc}$-$\langle V_{\rm fvc}\rangle$ characteristics of the FVC with and without the RO operation. A voltage step is observed in the $I_{\rm fvc}$-$\langle V_{\rm fvc}\rangle$ characteristics when the RO is on, as the numerical study suggested.

The step voltage $V_{\rm step}$ depends on the bias current to the C-SQUID gates. Fig. 7 shows the bias current dependence of $V_{\rm step}$. Measurement was executed for two chips. In Fig. 7, the horizontal axis is the total bias current for the RO and the Buffer gate. The simulated and experimental results show the same dependence on the bias current. In the experiment, $V_{\rm step}$ increases with the increasing bias current in the range of 12.5–12.8 mA. This means that the oscillation frequency

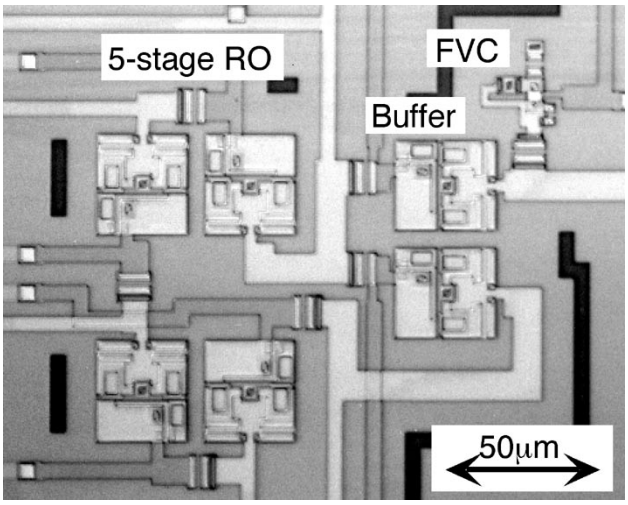
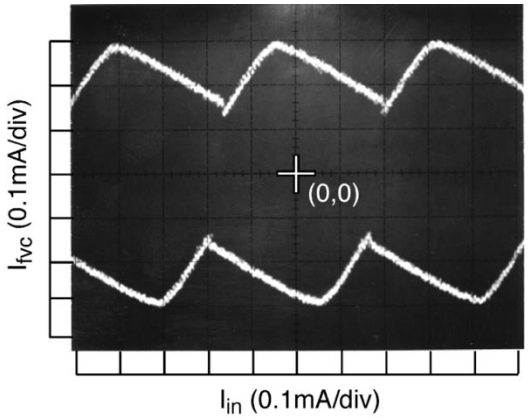
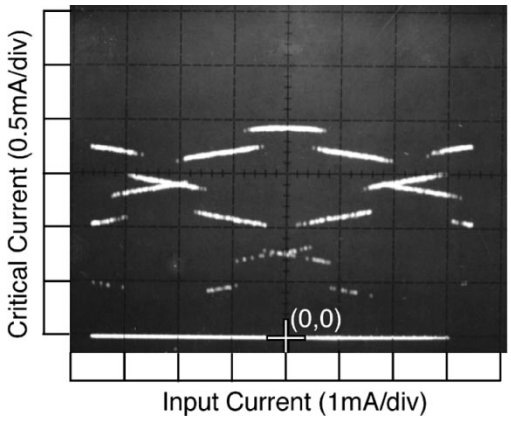


Fig. 4. Microphotograph of the fabricated circuit.

of the RO increases with the bias current. On the other hand, $V_{\rm step}$ decreases with the increasing bias current in the range of 12.8–13.3 mA. Simulations show that the RO does not operate correctly in the bias current region where $V_{\rm step}$ has negative



(a)



(b)

Fig. 5. Threshold characteristics of the fabricated circuit. (a) FVC. (b) C-SQUID gate.

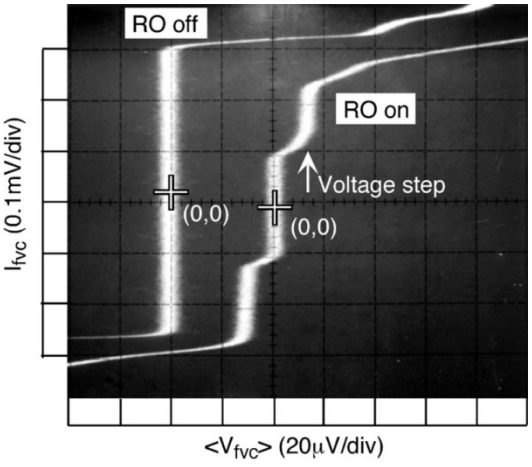


Fig. 6. $I_{\rm fvc}$-$\langle V_{\rm fvc}\rangle$ characteristics of the FVC (chip 2) with and without the RO operation.

dependence on the bias current. The bias margin of the measured circuits is 12.5–12.8 mA. This narrow bias margin is mainly due to the incomplete layout of the inductances in the FVC and the C-SQUID gates, as mentioned above. We have simulated the circuit operation assuming the fabricated parameters and confirmed that the bias margin is reduced from 10.2 to 12.3 mA to 11.4–12.3 mA.

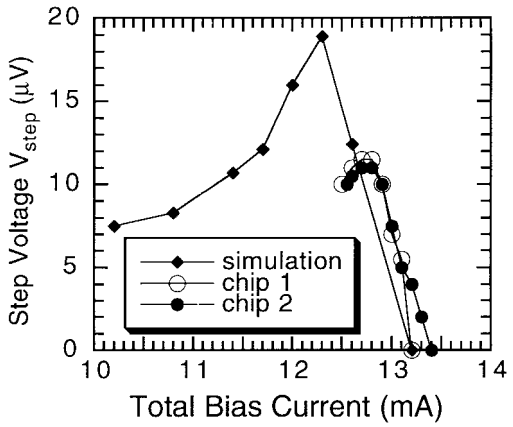


Fig. 7. Step voltage $V_{\rm step}$ as a function of the total bias current for the RO and the Buffer gate.

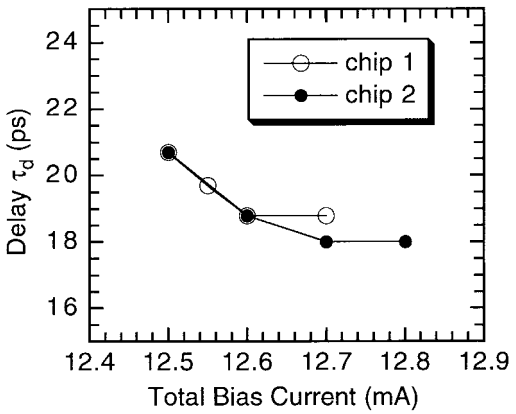


Fig. 8. Bias current dependence of the switching delay τ_d.

Fig. 8 shows the bias dependence of the C-SQUID switching delay in the bias current range of 12.5–12.8 mA. The minimum switching delay is 18 ps. This value is in the same range with the numerical results [5]. As shown in Fig. 4, one of the C-SQUID gates has a long output wiring. Its time constant is estimated in the order of 40 ps, about 20% of the oscillation period. Hence, by redesigning the circuit layout, the averaged switching delay would be improved at about 20%.

The junctions in the C-SQUID gate are shunted by the small resistance, which limits the switching speed. Employing the junctions having higher critical current density is effective to increase the speed performance [5], [6].

IV. Conclusion

We present the experimental results for the switching delay of the C-SQUID gate. The switching delay was calculated from the step voltage of the FVC by the use of the Josephson $\langle V\rangle$-f relation. The minimum delay was 18 ps/gate. This evaluation method restricts high-speed signal propagation within the Josephson integrated circuit in a dewar. Hence, it is a simple, accurate, and effective method for the evaluation of RO operation composed of nonlatching Josephson gates.

ACKNOWLEDGMENT

The authors would like to thank T. Onomi, H. Satoh, H. Hayakawa, A. Fujimaki, and F. Furuta for fruitful discussions. Part of this work was carried out at the Laboratory for Electronic Intelligent Systems, Research Institute of Electrical Communication, Tohoku University.

REFERENCES

[1] S. M. Schwarzbek, R. A. Davidheiser, G. R. Fischer, J. A. Luine, and N. J. Schneier, "Digital logic with $YBa_2Cu_3O_{7-x}$ dc SQUID's," *Appl. Phys. Lett.*, vol. 59, pp. 866–868, Aug. 1991.

[2] F. Furuta, S. Matsumoto, H. Akaike, A. Fujimaki, and H. Hayakawa, "New SQUID gate and its implementation into logic circuits," *IEEE Trans. Appl. Superconduct.*, vol. 7, pp. 3311–3314, June 1997.

[3] Y. Mizugaki, K. Nakajima, Y. Sawada, and T. Yamashita, "Implementation of new superconducting neural circuits using coupled SQUID's," *IEEE Trans. Appl. Superconduct.*, vol. 4, pp. 1–8, Mar. 1994.

[4] ———, "Superconducting neural circuits using SQUID's," *IEEE Trans. Appl. Superconduct.*, vol. 5, pp. 3168–3171, June 1995.

[5] Y. Mizugaki, T. Onomi, K. Nakajima, and T. Yamashita, "Experimental operation of an RS flip-flop composed of nonlatching Josephson gates," *IEEE Trans. Appl. Superconduct.*, vol. 6, pp. 90–93, June 1996.

[6] Y. Mizugaki, K. Nakajima, and T. Yamashita, "Neuro-base Josephson flip-flop," *IEICE Trans. Electron.*, vol. E78-C, pp. 531–534, May 1995.

[7] Y. Mizugaki and K. Nakajima, "Numerical simulation for digital applications of a coupled-SQUID gate with DC-biasing," in *Ext. Abst. 6th Int. Supserconductive Electronics Conf.*, Berlin, Germany, 1997, vol. 2, pp. 272–274.

[8] S. V. Polonsky, V. K. Semenov, P. I. Bunyk, A. F. Kirichenko, A. Yu. Kidiyarova-Shevchenko, O. A. Mukhanov, P. N. Shevchenko, D. F. Schneider, D. Yu. Zinoviev, and K. K. Likharev, "New RSFQ circuits," *IEEE Trans. Appl. Superconduct.*, vol. 3, pp. 2566–2577, Mar. 1993.

[9] M. Maezawa, M. Aoyagi, H. Nakagawa, I. Kurosawa, and S. Takada, "Specific capacitance of $Nb/AlO_x/Nb$ Josephson junctions with critical current densities in the range of 0.1–18 kA/cm^2," *Appl. Phys. Lett.*, vol. 66, pp. 2134–2136, Apr. 1995.

[10] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," *IEEE Trans. Appl. Superconduct.*, vol. 1, pp. 3–28, Mar. 1991.

[11] E. S. Fang and T. Van Duzer, "A Josephson integrated circuit simulator (JSIM) for superconductive electronics application," in *Ext. Abstr. Int. Superconductivity Electronics Conf.*, Tokyo, Japan, 1989, pp. 407–410.

[12] S. Nagasawa, Y. Hashimoto, H. Numata, and S. Tahara, "380 ps, 9.5 mW Josephson 4-Kbit RAM operated at a high bit yield," *IEEE Trans. Appl. Superconduct.*, vol. 5, pp. 2447–2452, June 1995.

Yoshinao Mizugaki received the B.E., M.E., and Ph.D. degrees from Tohoku University, Sendai, Japan, in 1990, 1992, and 1995, respectively.

In 1995, he was a Research Fellow of JSPS at Nagoya University for six months. Since 1995, he has been a Research Associate at the Research Institute of Electrical Communication, Tohoku University. His research interests include neural networks, advanced integration systems, and Josephson computing devices.

From 1992 to 1995, Dr. Mizugaki was awarded a Research Fellowship of the Japan Society for the Promotion of Science (JSPS) for Young Scientists. He is a member of the Japan Society of Applied Physics and the Institute of Electronics, Information and Communication Engineers of Japan.

Koji Nakajima received B.E., M.E., and Dr. Eng. degrees from Tohoku University, Sendai, Japan, in 1972, 1975, and 1978, respectively.

Since 1978, he has been working on Josephson junctions and soliton physics at the Research Institute of Electrical Communication, Tohoku University, except for a period in 1983, when he worked as a Visiting Assistant Research Engineer at the University of California, Berkeley. He is currently engaged in the study of VLSI implementation of neural networks, intelligent integrated systems, and Josephson junction devices for digital applications as a Professor at the Research Institute of Electrical Communication, Tohoku University.

Dr. Nakajima is a member of the Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers of Japan, the Institute of Electrical Engineers of Japan, and the Japanese Neural Network Society.

Akira Shoji was born in Yamagata Prefecture, Japan, on November 30, 1948. He received the B.S., M.A., and Ph.D. degrees in electrical engineering from Tohoku University, in 1972, 1974, and 1987, respectively.

He joined the Electrotechnical Laboratory of MITI in Japan in 1974. His research interests include applications of superconductivity, especially ultrahigh-speed digital circuits, submillimeter-wave oscillators, and voltage standards.