Superconducting neural circuits using fluxon pulses

doi: 10.1063/1.108571

Superconducting neural circuits using fluxon pulses

Yoshinao Mizugaki, Koji Nakajima, Yasuji Sawada, and Tsutomu Yamashita
Research Institute of Electrical Communication, Tohoku University, Sendai, Japan

(Received 14 April 1992; accepted for publication 8 December 1992)

A superconducting neural circuit is fabricated for the first time by use of a niobium integrated-circuit technology. Fluxon pulses on Josephson transmission lines (JTLs) are used as neural impulses. In this circuit a threshold element (a neuron) is composed of two JTL elements connected through a resistor. The conductance value of the resistor represent a synaptic strength. The fan-in and the fan-out are accomplished by the biased JTL branches. The operation of 2-bit neural based A/D converter is successfully observed. These circuits do not require any hysteretic Josephson junctions, and hence, have a potential to be fabricated with the high-T_c superconductors.

Recently, artificial neural networks are receiving extensive attention as new approaches to information processing. Several groups have reported the implementation of neural networks using semiconductor integrated circuits.[1,2] However, power dissipation will be a serious problem when large scale networks are attempted, because neural networks require a huge number of interconnections.

In this letter, we report superconducting integrated circuits for neural networks. Superconducting Josephson circuits have ultra-high-speed operation with very low power dissipation, and hence, they are suitable for large scale neural networks. This is the first report of fabricating superconducting neural integrated circuits and verifying the operation. Although there are a few proposals to implement neural networks using superconductors,[3,4] there has been no report of real implementation to the authors' best knowledge.

An artificial neural network consists of neuron devices which are connected to one another via synapse elements. In a network of n neurons, the activity of the ith neuron is described as

$$X_i=f(v_i), \quad \tau dv_i/dt=\sum_j^n T_{ij}X_j+h_i-v_i, \tag{1}$$

where τ, X_i, v_i, h_i, and T_{ij} are a time constant, the output, the potential level, the threshold value, and the synaptic strength of the ith neuron bringing input from the jth one, respectively. $f(v_i)$ is a sigmoid-shape function.

A basic superconducting circuit for a neuron, a threshold element, with constant synaptic strength is shown in Fig. 1(a). It is composed of two Josephson transmission lines (JTLs) and a resistor which connects the two JTLs. Fluxon pulses ($\sim$10 ps in width) on JTLs work as neural impulses with soliton characteristics in this circuit. When a fluxon propagating on the input JTL reaches the LR_{ij} loop containing the neuron junction which is the first junction of the output JTL, it is trapped there because of the loss of the resistor and the threshold characteristics of the neuron junction. The circulating current to hold the fluxon, which corresponds to neural potential level, decreases with the time constant L/R_{ij}. The fan-in (spatial summation) is accomplished by connecting plural input JTLs to the neuron junction through resistors.[5] When the temporal and spatial summation of the current flowing into the neuron junction exceeds the critical current, one fluxon comes out to the output JTL. The frequency of fluxon pulses on the JTLs is measured as the voltage across the junctions due to the ac Josephson effect. If the time constants of all inputs are the same, the current flowing through the ith neuron junction is described as

$$\tau du_i/dt=\sum_j^n (1/R_{ij})V_j-\sum_j^n (1/R_{ij})V_i^*+I_i-u_i, \tag{2}$$

where τ, V_i, V_i^*, u_i, I_i, R_{ij} are the time constant ($=L/R_{ij}$), the output voltage, the voltage of the neuron junction, the summation of the loop current, the external bias current for the ith neuron junction, and the resistor value which connects the jth output to the ith input, as shown in Fig. 1(a), respectively. Equation (2) has the same form as Eq. (1) except for the second term in the right-hand side. The existence of the second term means that this neuron circuit cannot avoid having self-connection because of the incomplete input–output isolation. One can break the lin-

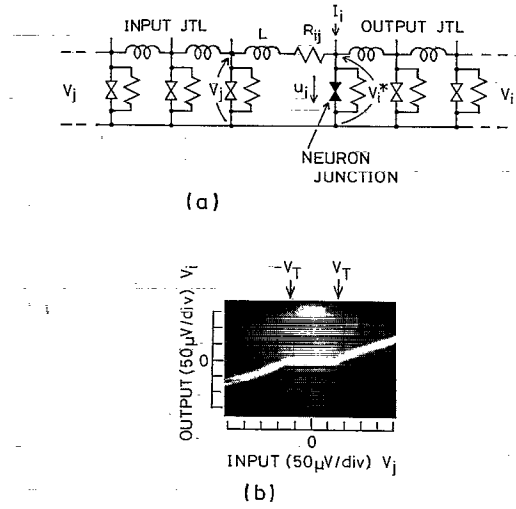

FIG. 1. (a) Equivalent circuit for a superconducting neuron with constant synaptic strength. (b) Input–output characteristics of a superconducting neuron circuit with constant synaptic strength. The inductance and the resistance inserted to the JTL are 4.1 pH and 0.023 Ω, respectively.

 0003-6951/93/070762-03$06.00

ear relation between V_i and V_i^* by inserting a junction ("break junction") into part of the inductance of the output JTL. Because the break junction switches to the voltage state with increasing V_i^*, the nonlinear relation can be used instead of the desired saturation characteristics of a neuron output.

The Josephson circuits are composed of a Nb ground plane, $Nb/AlO_x/Nb$ junctions, Au–In resistors, and Pb–In wiring. Each layer is isolated by SiO or Nb_2O_5. Sputtered Nb layers were patterned by anodization and wet etching. Nb_2O_5 was also used as an etching stopper.[6] $Nb/AlO_x/Nb$ junctions were defined by use of the SNAP (selective niobium anodization process) technology.[7] The JTLs are discrete type with overlap structure and are composed of 18 junctions of 5×5 μm^2 with shunt resistance. The critical current of each junction is designed to be 0.5 mA. The spacing between junctions is 60 μm. The loop inductance of each section of the discrete JTL is 1.31 pH. The capacitance of the junctions is 0.06 pF/μm^2.[8] Therefore the penetration depth λ_J is 84.6 μm. The shunt resistance for each junction is 0.66 Ω.

Figure 1(b) shows the experimental result for the relation between input and output voltage of the 1-input neuron circuit where $L=4.1$ pH and $R_{ij}=0.023$ Ω. No output voltage is observed until the input voltage is over the threshold value V_T. The experimental and numerical results shows that V_T is proportional to the resistance value R_{ij} independent of the loop inductance L, and also shows that the coefficient I_c^0 corresponds to the sum of the critical current of the output JTL with a length of about 2.5 λ_J. This means that V_T might be written as

$$V_T=\Phi/\tau=L\times I_c^0/(L/R_{ij})=I_c^0\times R_{ij}, \tag{3}$$

where Φ is flux in the LR_{ij} loop. The slope of the output characteristics beyond the threshold is $r/(R_{ij}+r)$, where r is the resistance of the output JTL beyond its critical current. The experimental output characteristics include some undulation which seem to be caused by the critical current modulation from the self-field.

A neuron with variable synapse is accomplished by connecting a dc-SQUID parallel to the neuron junction. The control current changes the critical current of the dc-SQUID. Then the critical current I_c^0 and the threshold voltage V_T suffer change. We observed the periodic modulation of the threshold voltage at the neuron circuit with variable synapse. The attached dc-SQUID is composed of two 10×10 μm^2 junctions and 0.38 pH loop inductance. The threshold voltage was reduced to 50% of the maximum. It would be possible to control the critical current of a dc-SQUID by fluxons trapped in the rf-SQUID loop which has large inductance and is magnetically coupled to the dc-SQUID. In the same way as the superconducting storage loop in a single-chip SQUID[9], this rf-SQUID would work as one kind of the analog memories. The number of fluxons in the rf-SQUID might be changed by external or internal learning system. The size of the rf-SQUID loop would limit the integration of synapses. Assuming that the critical current density, the critical current, the linewidth, and the inductance of the rf-SQUID

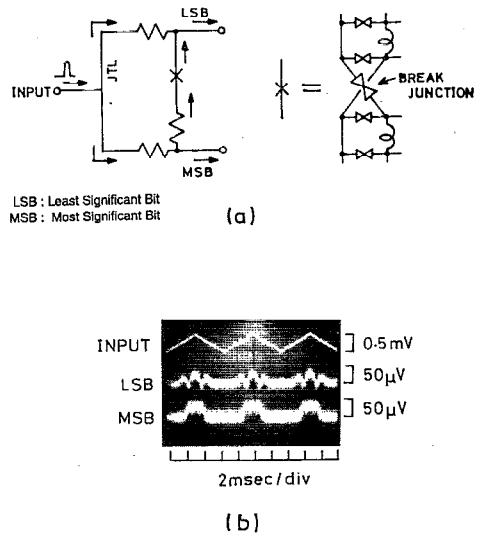

FIG. 2. Schematic configuration (a) and experimental result (b) of 2-bit A/D converter of the superconducting neural network.

are 7 kA/cm^2, 2 mA, 1 μm, and 10 pH, the size of junction and the length of the loop are 5.3×5.3 μm^2 and 20 μm, respectively. Then the size of one synapse is estimated to be 20×20 μm^2 and it is possible to integrate 2.5×10^5 synapses per 1 cm^2. At present, 500 ps has been achieved as the minimum access time of Josephson random access memories.[10] So the expected learning speed is 2 gigainterconnections per s at the lowest.

In order to demonstrate the operation of the superconducting neural circuit, we designed a 2-bit A/D converter of Hopfield type[11] which is one of the circuits solving optimization problems. The A/D converter is composed of three resistors, an input JTL, two output JTLs including two neuron junctions, and the fourth JTL which makes a synaptic connection between the two neuron junctions, as shown in Fig. 2(a). In order to make a inhibitory connection, the fourth JTL is twisted. The twist is accomplished by inserting a "break junction" which has 56 times larger critical current than that of the normal junctions of JTLs. The bias current is supplied to the twisted JTL to flow fluxons in one direction. The other JTLs are also biased to obtain proper thresholds. Fluxon pulses from the input diverge at the phase conserving branch[5] and propagate to each neuron junction through each resistor. When the frequency of input fluxons is low, no fluxon appears on either output JTL. This is "00" state. If the input voltage exceeds the threshold V_{TL} of the LSB (least significant bit) neuron, the LSB neuron switches to voltage state and "01" state is achieved. When the input exceeds the threshold V_{TM} of the MSB (most significant bit) neuron, where $V_{TM} > V_{TL}$, the MSB output suppresses the LSB activity; that is "10" state. The increase of the suppressive signal lets the "break junction" transit to voltage state. It suppresses the increasing rate of the suppressive signal and then "11" state appears. Figure 2(b) shows the experimental results for the operation of the 2-bit A/D converter. The power

dissipation in the 2-bit A/D converter was 2.5 μW/junction and 11 nW/junction including and excluding the biasing, respectively. By cutting down the biasing resistance to ten times as large as the shunt resistance of the junction, the power dissipation will be reduced to 100 nW/junction including the biasing.

In summary, we propose superconducting neural circuits using fluxon pulses and implement them with Nb/AlO_x/Nb integrated circuits. We demonstrate the operation of a 2-bit neural-based A/D converter. This is the first report of experimental measurement of superconducting neural integrated circuits. In order to avoid the power distribution and dissipation problem, we can use JTLs only in the part of neurons and use superconducting strip line for interconnections. These circuits are based on the phase mode logic circuits and do not require any hysteretic junctions. Hence, they have the potential to be fabricated with high-T_c superconductors.

[1] A. F. Murray and A. V. W. Smith, IEEE J. Solid-State Circ. **23**, 688 (1988).
[2] Z. Tang, O. Ishizuka, and H. Matsumoto, The Transaction of the Institute of Electronics, Information and Communication Engineers **E74**, 1329 (1991).
[3] Y. Harada and E. Goto, IEEE Trans. Magn. **27**, 2863 (1991).
[4] M. Hidaka and L. A. Akers, Extended Abstracts of the Third International Superconductive Electronics Conference, 164 (1991).
[5] K. Nakajima, H. Sugahara, A. Fujimaki, and Y. Sawada, J. Appl. Phys. **66**, 949 (1989).
[6] Y. Mizugaki, K. Nakajima, Y. Sawada, and T. Yamashita, The Transaction of the Institute of Electronics, Information and Communication Engineers, **J74-C-II**, 812 (1991) (in Japanese).
[7] H. Kroger, L. N. Smith, and D. W. Jillie, Appl. Phys. Lett. **39**, 280 (1981).
[8] M. Gurvitch, M. A. Washington, and H. A. Huggins, Appl. Phys. Lett. **42**, 472 (1983).
[9] N. Fujimaki, H. Tamura, T. Imamura, and S. Hasuo, IEEE Trans. Electron Devices **35**, 2412 (1988).
[10] I. Kurosawa, H. Nakagawa, S. Kosaka, M. Aoyagi, and S. Takada, IEEE J. Solid-State Circ. **24**, 1034 (1989).
[11] D. W. Tank and J. J. Hopfield, IEEE Trans. Circ. Syst. **33**, 533 (1986).