Phase mode Josephson computer system

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Phase Mode Josephson Computer System

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(Invited Paper)

Abstract—**We present a basic idea for the operation of a phase mode Josephson computer system, which is expected to be superior to a voltage mode Josephson computer in several respects. In a phase mode system, device operation depends on the existence of many stable states differing from each other by integer multiples of 2π in the phase plane. As an example, we propose a simple model of a complete phase mode computing system in the present paper, and discuss the basic computer elements and the instructions in this system. The total system is considered to be a prototype of quantum computer systems where physical quantum states are employed as logic states for information processing.**

I. Introduction

SUPERCONDUCTING Josephson computer elements have great potential for future computer systems, because of their high-speed switching time (~ 10 ps) and low power dissipation (~ 500 nW per circuit) [1]. The thermal energy is about 100 times smaller at 4 K than at 360–380 K where semiconductor circuits are operated. This leads to smaller thermally induced electrical noise, and helps to maintain good signal-to-noise ratio even when signal bandwidth is increased and signal energy is reduced.

In the present paper we discuss one of the simplest models of Josephson computer systems (phase mode system) [2], in which quantized vortices of magnetic flux (fluxoids) are employed as information bits [3], and in which all logic functions are achieved by interactions between fluxoids [4], in contrast to a voltage mode system, whose operations are based on the existence of two stable current carrying states at $V = 0$ and $V = V_{gap}$ [5] (V_{gap} is the voltage corresponding to the superconducting gap energy). The phase mode system is superior by more than two orders of magnitude in power dissipation to the voltage mode system because of the small amplitude and short duration of signal voltages. In spite of small amplitude and short duration, the signal does not decay because of flux quantization. The employment of the particle-like characteristics to the data processing system would remove the uncertainty of the binary identity that is observed in ordinary digital circuits [6]. The phase mode devices have the same switching time as the voltage mode [7]. The "latching" mode of operation is used in the voltage mode circuits; therefore, they are required to be reset in each cycle. On the other hand, in the phase mode circuits, the latching mode of operation is not used.

Phase mode Josephson LSI circuit chips, although quite different in their principle of operation, may be fabricated quite similarly to voltage mode Josephson LSI chips. The data processor presented here is estimated to be superior in processing speed, information density, and power loss to the ordinary voltage mode system. The total system presented is also considered to be a prototype of future quantum computer systems, where physical quantum states are employed as logic states for information processing in a molecular device, the ultimate device of miniaturization.

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II. Fundamental Properties of Fluxoids

A Josephson junction can be represented by the equation

$$\frac{d^2\phi}{dt^2} + \Gamma \frac{d\phi}{dt} + \sin\phi = \gamma \tag{1}$$

where ϕ is the phase difference of the junction between two superconductors, Γ represents the nonlinear conductance of the junction, and γ is the normalized bias current [6]. Let us consider a superconducting ring composed of several Josephson junctions. The circulating current I satisfies the equation:

$$\frac{\Phi_o}{2\pi} \sum_i \sin^{-1}\left(\frac{I}{I_{ci}}\right) + LI = n\Phi_o, \qquad n = 0, 1, 2, \cdots \tag{2}$$

where Φ_o is the flux quantum, I_{ci} is the maximum dc Josephson current of ith junction, and L is the self-inductance of the ring. The left-hand side of (2) is quantized in units of Φ_o, called a "fluxoid," which represents a flux quantization if we neglect the first term of (2) in a thick superconductor ring without junctions. The fluxoid is employed as an information bit in the following phase mode computer design, and the superconducting rings composed of Josephson junctions are basic elements of the phase mode system. One can use discrete Josephson transmission lines (DJTL's) as lead lines to transmit single fluxoids. The transmission of signals between elements is carried out by using the DJTL's, each of which is represented by the equation:

$$\beta(\phi_{i+1} - 2\phi_i + \phi_{i-1}) - \frac{d^2\phi_i}{dt^2} - \Gamma \frac{d\phi_i}{dt} = \sin\phi_i - \gamma \tag{3}$$

where β and ϕ_i are a dimensionless parameter inversely proportional to the loop inductance of a unit section of the DJTL, and the phase difference of ith junction, respectively. A soliton (nonlinear solitary wave) in a Josephson transmission line or a DJLT is called a "fluxon" in general, so we also use a "fluxon" for a soliton in DJTL's. On the other hand, we use a "fluxoid" emphasizing the first term of (2) to represent a soliton in a fluxoid transmission line (FTL) [9], which contains extra Josephson junctions in each unit section of DJTL as shown in the following.

We have reported the observation of fluxon–antifluxon collision processes of all types (annihilation, passing through, and pair creation) in a DJTL [10], [11]. An antifluxon has the inverse twining of vortex to a fluxon vortex. The collision processes were directly measured not only in time but also in space by a Josephson sampling system. The observed characteristics were useful for the design of phase mode data processing circuits. However, the spatial dimension of a fluxon in the DJTL was too large for integrated digital circuits. The size of a fluxon is generally a function of the loop inductance of a unit section of the DJTL, which has a strong dependence on the circuit layout. This dependence makes circuit design complex. The use of kinetic inductance of junctions has been proposed for miniaturization of these circuits [12]. A series of n junctions has the

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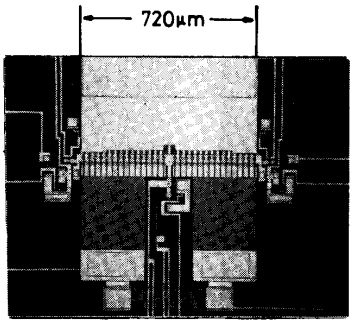


Fig. 1. Fabricated fluxoid transmission line.

following kinetic inductance:

$$L_J = n\Phi_o\phi/2\pi I_c \sin\phi. \quad (4)$$

L_J depends on the critical current of the junction, but not on the circuit layout. We have made experimental and numerical investigation of the basic propagation characteristics of an FTL.

Fig. 1 shows a photograph of an FTL that was fabricated by use of a conventional niobium circuit technology [13]. The superconducting circuit comprises four components: a Josephson sampler, an FTL, and two identical pulse generators. The FTL is composed of 31 parallel Nb/AlOx/Nb junctions 4 μm × 4 μm in size with 1.65-Ω shunt resistors, and of 60 additional serial junctions for kinetic inductance. Each single loop of a unit section of FTL has two extra junctions for kinetic inductance. The critical current of each extra junction is 2.6 times larger than that of a parallel junction. The measured total critical current I_o of the FTL is 15.5 mA, which corresponds to the total critical current of the 31 parallel junctions. We have estimated the loop inductance L of each unit section as $LI_c/\Phi_o = 0.77$, where L is composed of both normal and kinetic inductance and I_c is the critical current of a single parallel junction.

Fig. 2(a) shows a propagating fluxoid waveform obtained by using the Josephson sampler [7]. Fig. 2(b) and (c) show the numerical results for the voltage waveform of a propagating fluxoid and the time dependence of the phase differences of the junctions, which are indicated in the inset of Fig. 2(c), respectively. Fig. 3 shows the spatio-temporal evolution of waveforms of a fluxoid-antifluxoid pair passing through each other. The measuring system is basically an ordinary Josephson sampler with an extra electrical delay in addition to a mechanical delay. The relative position of the pair in the FTL, or equivalently the sampling time after the introduction, is controlled by the mechanical delay. The absolute position of the center of gravity of the pair with respect to the measuring point is scanned by the electric delay, which controls the time difference of introducing a fluxoid and an antifluxoid. Scanning the center of the pair for fixed relative position is equivalent to scanning the measuring position for fixed pair position [10], [11]. In Fig. 3, the two peaks of the fluxoid and the antifluxoid merge into a higher single peak at the collision, then they recover the original forms.

The positions of the fluxoid and the antifluxoid were plotted as a function of time in Fig. 4. Fig. 4 shows a negative phase shift (positive time delay), which is the same as the interaction of a fluxon pair on the DJTL with loss and acceleration. Our numerical calculation using the experimental loss parameter shows that the phase shift is always negative, independent of the line bias

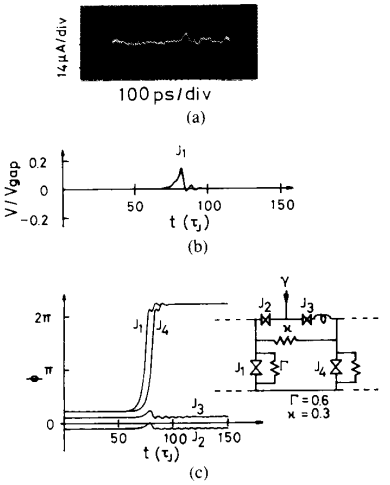


Fig. 2. (a) Experimentally obtained waveform of a propagating fluxoid on an FTL. (b) and (c) Numerical results for the voltage waveform of the propagating fluxoid, and for the time dependence of the junction phase differences of the FTL, respectively.

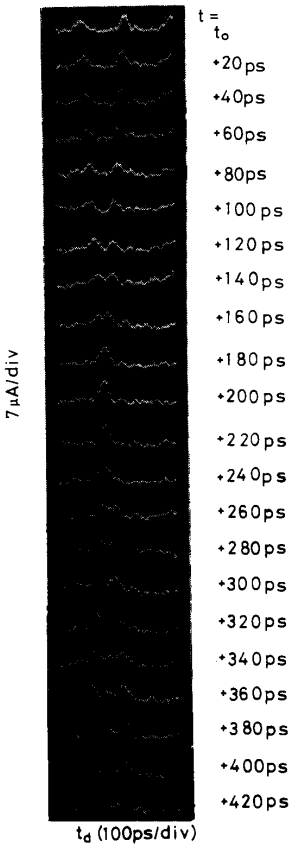


Fig. 3. Fluxoid-antifluxoid passing through waveforms in time and space. The unit of vertical axis is 7 μA/div. The horizontal axis is proportional to the distance l between two fluxoids in the FTL, as $l = ut_d$, where u and t_d are the constant velocity of the fluxoid and the electrical delay time of the sampling system, respectively. The time indicated at the right-hand side for each waveform is directly obtained from the mechanical delay time of the sampling system. The line bias current I_b is 9.27 mA.

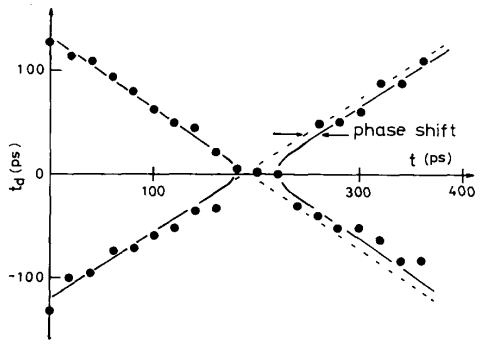


Fig. 4. Experimentally obtained (●) fluxoid-antifluxoid collision trajectory which were plotted by use of the result shown in Fig. 3. The vertical axis is proportional to the distance $l = ut_d$ in the FTL, where u and t_d are the constant velocity of the fluxoid and the electrical delay time of the sampling system, respectively.

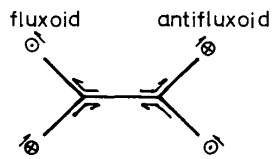


Fig. 5. Line crossing of DJTL or FTL can be accomplished by use of two p.d. branches. When a fluxoid-antifluxoid collision occur simultaneously, the loss parameter should be properly chosen not to incur an annihilation.

current, and that the magnitude of the phase shift decreases with increasing line bias current. It is shown by the simulation that the collision process of a fluxoid pair on the FTL has three possible outcomes: annihilation, passing through, and pair creation. These results show that we can use both the FTL and DJTL as lead lines for signals.

In practical use, branching and crossing of lead lines are required. The main functions of branching are "FAN OUT" and "FAN IN." The FAN OUT is accomplished by using the phase conserving (p.c.) branch that was previously reported [8], [14], [15]. Numerical and experimental results have shown that the p.c. branch provides the FAN OUT function over a wide range of circuit parameters (for example, line bias currents). The FAN IN function is accomplished by using the phase distributing (p.d.) branch that was also reported [8], [15]. The FAN IN function of the p.d. branch also has a wide operational range.

If all Josephson junctions on a chip are fabricated in one process step, a simple crossing over of FTL's or DJTL's cannot be realized. However, a line crossing can be accomplished by use of two p.d. branches, as shown schematically in Fig. 5.

III. Simple Models of Circuits and System

In this section we discuss qualitatively the principle of logic operation in a phase mode system, which has some similarity to that of the neuristor [16] and the magnetic bubble device [17]. In a phase mode system, a Josephson junction is used as a gate controlling the transit of a single magnetic flux quantum or a single fluxoid that is conserved and localized in space. The phase mode circuits advantages in both dc-coupled and ac-coupled logic circuits. They do not require maintenance of accurate voltage levels at various interconnections or precise coincidence of the pulses for the logical AND operation. They also have the

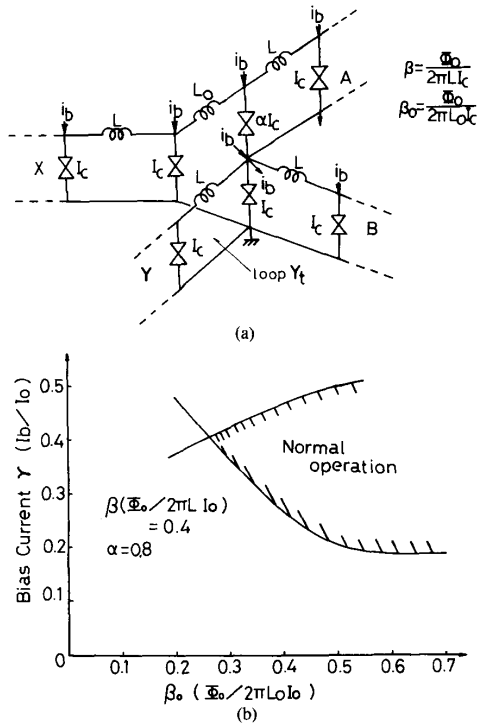


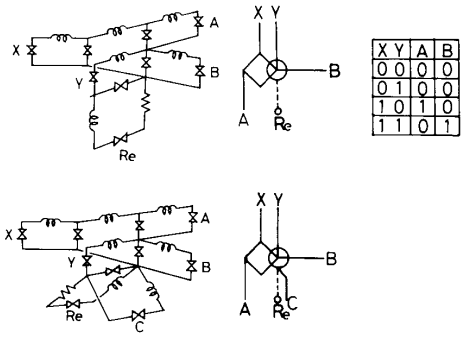
Fig. 6. (a) Equivalent circuit for ICF gate. (b) Numerical result for the normal operation of the ICF gate in the circuit parameter space.

permanent storage property of fluxoids that provides a variable delay. A propagating fluxoid causes voltage pulse of about a 10-ps duration, which depends on critical current density. It might look difficult to synchronize many 10-ps signals for realization of logic operations between them. However, a fluxoid can be localized in space during an arbitrary interval. Therefore, one fluxoid can be held until other fluxoids arrive to interact with it. The particle-like character of fluxoids removes the uncertainty of the binary identity.

On the other hand, a phase mode system requires the elimination of residual fluxoids after some logic operations are performed. For example, two input fluxoids create an output fluxoid in an AND circuit, and then one of the input fluxoids has to be eliminated. Elimination of a fluxoid is easily realized by inserting a resistor in a part of the superconducting ring, as it breaks the quantization condition. The other way to eliminate fluxoids is to make a fluxoid collide with an antifluxoid under suitable conditions, as shown in the previous section.

We have already reported on the construction of basic logic circuits, for example, AND, OR, and NOT, in our previous papers [4], [18]. But combinations of AND, OR, and NOT basic circuits are not always desirable to make a large phase mode system in terms of practical circuit construction. It seems that one should take an INHIBIT circuit as the most basic circuit in the phase mode system for circuit simplicity. It can be proven in terms of Boolean algebra that INHIBIT as well as NAND, NOR, and IMPLICATION is a universal operation. From this, it is clear that all logical functions can be constructed by combination of INHIBIT circuits. It is easy to make an INHIBIT circuit controlled by fluxoids (ICF gate) in the phase mode system.

Fig. 6(a) shows the equivalent circuit of the ICF gate, which



X	Y	A	B
0	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1

Fig. 7. Simplified equivalent circuits, symbols, and the truth table for the ICF gates.

is a combination of p.d. and p.c. branches. One input X and two outputs A and B compose a p.d. branch. One output B and two inputs X and Y compose a p.c. branch. The preliminary experimental results for the operation of an ICF gate have been reported [15]. The following functioning of the ICF gate can be expected from the experimental results and numerical simulations. A fluxon from input Y stops at the branch point (loop Y_t in Fig. 6(a)), and it remains trapped. A fluxon from input X is emitted from output A under the condition of no trapped fluxon from input Y. When a trapped fluxon from input Y exists, a fluxon from input X is combined with the trapped fluxon, and then it is emitted from output B. The A output DJTL is not grounded. We believe this fact does not create any problems in the phase mode system. The reasons are as follows: 1) electromagnetic field cannot penetrate into superconductors except for penetration depth, 2) signals are localized flux, and 3) the absolute value of phase is not a physical reality.

Numerical simulations show that the above mentioned normal operation of the ICF gate is accomplished within the indicated area of parameter space in Fig. 6(b). Fig. 7 shows equivalent circuits and symbols of the ICF gate used in this paper. A and B outputs in Fig. 7 represent INHIBIT and AND, respectively, as shown in the truth table of Fig. 7. "Re" in Fig. 6 denotes a reset terminal to eliminate or to pull out a trapped fluxon into the line C. The reset margin of the ICF gate is calculated by numerical simulations to be about $\pm 15\%$ for the bias current used.

A. Terminal

In the following discussion we choose the wordlength to be 6 bits for convenience in designing a very simple processor. But by the combination of computer elements described in the following sections larger processors can be designed.

The bus system in the phase mode requires a special design because of the particle like properties of fluxoids. Terminals I and II shown in Fig. 8 are used to control the direction of data transfers. The simple lines in the following figures denote FTL's or DJTL's, and the small circle denotes a p.c. branch (FAN OUT). Terminal I, which is the simple combination of ICF gates, can control transfer of 6-bit data from a bus to a register. The arrows denote the propagating directions of fluxoids. The upper six lines transmit 6-bit data composed of fluxoids, and the bottom line transmits a control signal of a single fluxoid. The set of six vertical lines with arrows pointing downward is connected to a register. When a single fluxoid comes down from the top of the figure along the vertical line with an arrow, the incoming

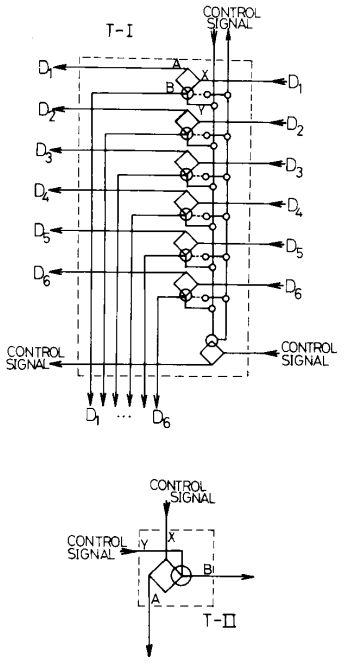


Fig. 8. Terminal I and II gates.

fluxoid sets a single fluxoid to the Y terminal which stores a fluxoid. When a set of fluxoids composed of 6-bit data and a single control fluxoid arrive at the terminal under this condition, the set of 6-bit data fluxoids propagates downward and is led to a register. Simultaneously, the control fluxoid is led upward, resetting the residual fluxoids at each bit of terminal which had been set by the initial control fluxoid and had been left there in the case of bit signal equal to "0." The control fluxoid is eliminated by itself at the resistor of the Re terminal of the ICF gate when no residual fluxoid has been left in the case of bit signal equal to "1." When no fluxoid is trapped at the ICF gate, a set of data and control fluxoids arriving at the terminal propagate leftward, passing through the terminal. Thus the fluxoids for one data word propagate downward or leftward depending on whether the control fluxoids from the top are being set or not. In order to perform the terminal operation, each fluxoid should be set at the ICF gates before the arrival of the data fluxoids. The terminal II gate in Fig. 8 is a single ICF gate.

B. Decoder

One can easily construct a tree matrix type decoder by a slight modification of the terminal I shown in Fig. 8. An example of the decoder is shown in Fig. 9, which may be used as the control unit of the model processor in the following discussion. In Fig. 9, the set of seven horizontal lines with arrows pointing right would be a data bus. The top line of the bus transmits a control signal composed of a single fluxoid. The other six lines transmit data composed of fluxoids, and the data fluxoids are set at the ICF gates. The control signal propagating on the top line passes through the p.c. branch, and then one of two control fluxoids is led to one of eight lines, which are vertical lines with arrows pointing downward and indicated as "OPERATION." Another control fluxoid is led to one of 16 lines, which are vertical lines with arrows pointing downward and indicated as "ADDRESS."

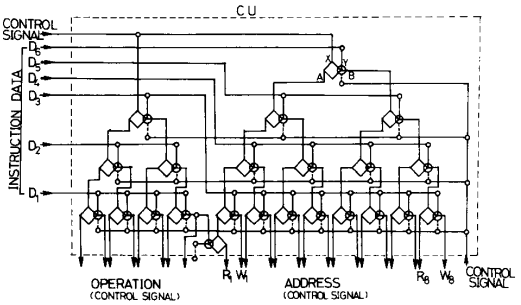


Fig. 9. Decoder circuit. This circuit is used as the control unit for the system shown in Fig. 14.

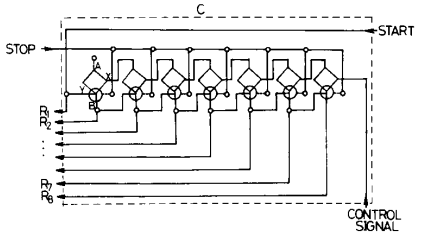


Fig. 10. Counter circuit. This circuit is used as the program counter for the system shown in Fig. 14.

The line where two control fluxoids should propagate is selected depending on whether each bit of the 6-bit data is "1" or "0" according to the characteristics of terminal II. In order to perform the decoder operation, data fluxoids should be set at each ICF gate before the arrival of the control fluxoid. The fluxoid that propagates upward on the vertical line with an arrow pointing upward shown in the right-hand side of this figure is used to reset the residual fluxoids at the end of one operation. More detailed explanation on how to use this circuit as a control unit will be given in the following discussion.

C. Counter

Circuit design of counters constructed using phase mode circuits was reported in a previous paper [18]. We design in this section a program counter that will be used as a part of the model processor in the next section. The counter is shown in Fig. 10. The top horizontal line with an arrow pointing left transmits a single fluxoid signal to start counting. One of the start signals is led to the first output line R_1 of the counter, which is the top horizontal line of the eight horizontal lines with arrows pointing left. Another start signal is led to the first ICF gate and is set there. The vertical line with an arrow pointing upward in the right-hand side of the figure transmits the input fluxoids to be counted. The single input fluxoid passes through the ICF gates one by one from the right-hand side. When the input fluxoid arrives at the first ICF gate, it is emitted from B. Then one of the two fluxoids is led to the second output line R_2 of the counter. The other fluxoid is led to the next ICF gate and set there. Each counting operation shifts the trapped fluxoid. The horizontal line with an arrow pointing right transmits a stop signal to reset the fluxoid trapped at one of the ICF gates.

D. Memory

Fig. 11 shows an example of a 6-bit word organized memory circuit. The capacity of the memory is 48 bits. It is easy to build

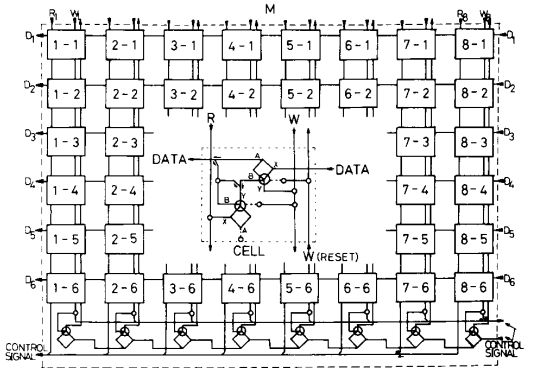


Fig. 11. 48-bit memory circuit. The first and second numbers written in each cell show the address and the bit of the memory, respectively. The detailed structure of each cell is illustrated in the center.

it up to more than 48 bits. The first and the second numbers written in each cell show the address and the bit number of the cell, respectively. The seven horizontal lines with arrows pointing left are the lines that construct a part of the bus. The bottom line transmits a control signal. The other six lines transmit a 6-bit data word. The detailed structure of each cell is illustrated in the central part of the figure, which is composed of two ICF gates. The lower ICF gate stores bit data. R and W denote the control fluxoids for reading out of the memory and for writing into the memory, respectively, which are sent from the address output of the control unit. The W signal sets fluxoids at the upper ICF gate of each cell of an address reserved, and also resets the previous data bits stored at the lower ICF gate. After that, the W signal propagates rightward on the horizontal line with an arrow pointing right, and leaves the memory. The 6-bit data propagating leftward on the bus are stored at the ICF gate of the address reserved by the W signal. The control fluxoid propagating on the seventh bus line together with the 6-bit data is led on the vertical line with arrows pointing upward. The control fluxoid resets the residual fluxoids set by the W signal, which have been left there in the case of a bit signal equal to "0." The stored fluxoids are extracted as information bits by the R signal. The extracted bit fluxoid passes through the p.c. branch, and one of two fluxoids is again stored at the same ICF gate, so that the rewriting into memory is simultaneously carried out by the bit fluxoid. The other fluxoid is led to the bus, and propagates leftward. The R signal continues to propagate leftward on the bottom line of the bus as a control fluxoid after pulling out the 6-bit data.

E. Inverter

Fig. 12 shows an example of an inverter, where the six horizontal lines with arrows pointing right transmit 6-bit data. In order for the circuit to act as an inverter, the control fluxoid should arrive after the 6-bit data is set.

F. Adder

We have already reported circuit designs of various kinds of adders constructed by phase mode circuits in a previous paper [18]. We design a parallel adder in this section that is used as a part of the model processor in the next section. The adder is shown in Fig. 13. This adder works also as a subtractor, a register, and an accumulator. In Fig. 13, a 6-bit data propagate on the six horizontal lines with arrows pointing right, except for

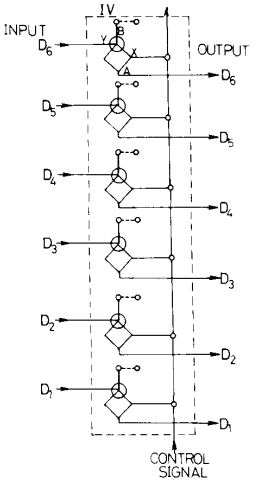


Fig. 12. Inverter circuit. This circuit is used as the 1's complementer in the system shown in Fig. 14.

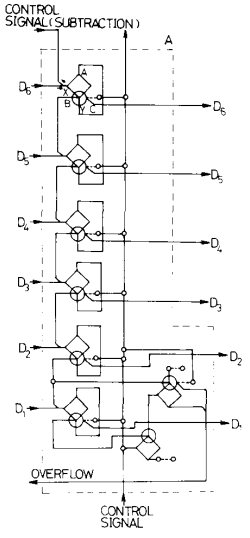


Fig. 13. Adder or accumulator. The overflow signal is led to the output shown in Fig. 14 to notice an occurrence of overflow.

the top line at the left-hand side of the circuit. A set of fluxoids that consists of a 6-bit number format is sent into the circuit from the left-hand side, and it is stored at each ICF gate. In the case of adder operation, the next set of fluxoids to be added is then sent into the circuit along the same channels. If the augend fluxoid is already stored at the ICF gate, the addend single fluxoid combines with the augend fluxoid, and they are emitted from B. The emitted fluxoid is sent to the next stage as a carry signal. The resulting sum bits are stored at the ICF gates. In the case of accumulator operation, the next set of fluxoids to be added should then be sent into the circuit. In the case of subtractor operation, the fluxoid propagating rightward on the top horizontal line should be sent into the circuit, and simultaneously data in inverted number format should be given to each bit part of the circuit to subtract from the contents. The processed

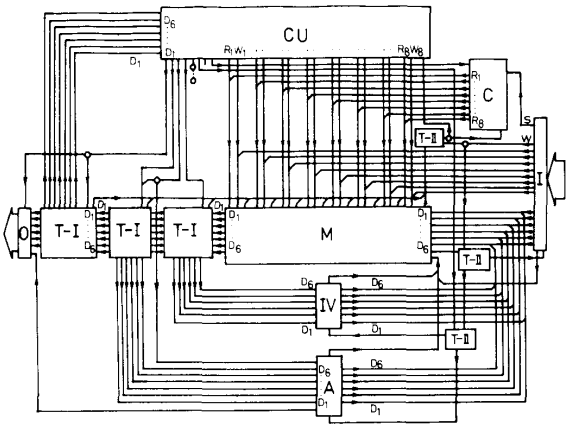


Fig. 14. System configuration of a phase-mode Josephson processor. I, C, CU, M, IV, A, O, T-I, and T-II denote input, program counter, control unit, memory, inverter, adder, output, and types I and II terminals, respectively. The lines with arrows denote FTL's or DJTL's.

results will be extracted by the fluxoid propagating upward on the vertical line with an arrow pointing upward.

G. System Configuration

The processor to be designed is the simplest kind of stored program digital system capable of performing several simple operations [6]. For convenience in designing a very simple processor, the wordlength is kept short and fixed. We choose the word length to be six bits. In the number format a decimal point is fixed. The instruction format consists of a 3-bit address, allowing eight addresses, or eight memory words, and thus the capacity of memory is 48 bits. An automatic clock system is used to demonstrate the feasibility of using the ultrashort pulses and the particle-like characteristics of fluxoids, because it does not have to use up a fixed time interval.

Fig. 14 shows the configuration of the processor. The partial units shown in Figs. 8–13 are set in each part of the system configuration in Fig. 14. In Fig. 14, I, C, CU, M, IV, A, O, T-I, T-II, and the lines with arrows denote input, program counter, control unit, memory, inverter, adder, output, terminal I, terminal II, and FTL or DJTL, respectively. S denotes the start signal, and W denotes a signal that is given manually and is initially used to store instructions and data in the memory. The number of necessary instructions of the processor is seven. The arithmetic logic unit (ALU) of the processor consists of only an inverter or 1's complementer and an adder or accumulator. ALU operations include addition and subtraction, but with a slight modification that they can also include unconditional and conditional transfers. The instructions are as follows.

1) Take a number from memory at the address reserved, and put it into the output register, which is represented as $(000XYZ)$ in the instruction format where X, Y, and Z are address bits.
2) Take a number from memory at the address reserved, and put it in the adder or add it to the contents of the adder, which is represented as $(100XYZ)$.
3) Take a number from the memory at the address reserved, and put it in the inverter, which is represented as $(110XYZ)$.

4) Take a number from the memory at the address reserved, and add it to the contents of the adder for subtraction, which is represented as ($010XYZ$).
5) Store the contents of the adder into the memory location at the address reserved, which is represented as ($001XYZ$).
6) Store the contents of the inverter into the memory location at the address reserved, which is represented as ($101XYZ$).
7) Stop the machine, which is represented as (111000).

The S signal should be sent to start the machine after writing data into the memory. The S signal is led to the program counter. The counter sends an R signal to the first address at the memory to read out the 6-bit data. After extracting the 6-bit data from the memory, the R signal propagates as a control signal on the bus together with the 6-bit data. They are led to the control unit after passing through three T-I's shown in Fig. 14. According to the values of both 3-bit operation-code and address-code of the instruction, one of the two control signals is led to one of the partial units except for memory, and another control signal is led to the memory as an R or W signal. The actions required for the control signal to 1) read and to 2) write, respectively, are explained in the following.

1) The signal takes the data from the memory, and propagates down the bus as a control signal together with the data signals. The propagating direction of the 6-bit data and the control signal is changed at one of three T-I's. The 6-bit data signals are led to the output or the adder or the inverter. The control signal is led to the control unit for reset and to the counter. The counter sends an R signal to the second address of the memory to read out the next instruction. Hence this model is an automatic clock (or self-clocking) system where it is not required to use up a fixed time interval.

2) The signal is led to the adder or the inverter after passing through the memory. It takes the data from the adder or inverter, and goes back to the memory as a control signal. The extracted data are sent to the memory and stored at the address reserved by the W signal. After passing through the memory, the W signal is led to the control unit for reset and to the counter.

If the control signal is the stop signal, which is sent from the operation part of the control unit, the control signal is led to the counter and stops the machine.

IV. Conclusion

A simple phase mode Josephson data processor system, where fluxoids are employed as information bits and all logic functions are achieved by the interactions between fluxoids, is qualitatively discussed in this paper. Our processor is binary and an automatic clock system. The system organization is quite different from the ordinary voltage mode organization, which is similar to that used in the computer systems constructed with semiconductor devices. The automatic clock system seems to be suitable to demonstrate the feasibility of using the ultrashort pulses and the particle-like characteristics of fluxoids. The reasons are as follows.

1) The single fluxoid, which is conserved and localized in space, can wait to interact with the other fluxoids. Therefore, each input signal can wait for the arrivals of the other input signals to synchronize.
2) Each input signal can know the termination of the logic circuit operation independently of the output of previous logic circuits, because all logic operations are performed by the interactions between the input fluxoids. On the other hand, in semiconductor circuits the states of input signals depend only on the output of previous logic circuits independent of the other input signals.
3) These particle-like characteristics would reduce the uncertainty of the binary identity, and the problems of critical race and hazard.
4) The automatic clock system does not have to use up a fixed time interval, so it is suitable for this logic system where ultrashort pulses are used as information signals. The propagation velocity of the signal is about one-tenth of the light velocity. Hence it takes 300 ~ 800 ps to propagate 1 cm on a chip.

Thermal noise, electrical noise, and flux trapping are important factors for constructing not only a phase mode system, but also a voltage mode system. If the disturbance from these things becomes larger than the critical current of Josephson junction, error should occur. There is no difference for this condition between the two modes of a Josephson system. We do not especially insist that the phase mode system is superior to the voltage mode system with respect to the external physical environment. But physical quantization in the phase mode system may have some advantage against the external disturbance. The physical environment affects the phase mode system in nearly the same way as the voltage mode system.

The critical current density J_c has no maximum limit for the phase mode circuits, because they do not require any switching operations on the I-V characteristics. One can also use the kinetic inductance for miniaturization of phase mode circuits. Therefore, it should be expected that one of the highest density computer systems can be constructed based on our processor design.

A Josephson device has the fastest switching speed. A phase mode Josephson computer system can be operated under the nonlatching mode, and it is free from the punchthrough [19]. So the operating speed is not limited by the cycle time of the bias current for gates. It depends only on the logic delay. The total logic delay (turn-on delay, risetime, crossing delay, and propagation delay) of the phase mode is almost the same as the voltage mode. The propagation velocity of fluxoids is one-tenth of the light velocity in Josephson transmission lines, which is originated from a large ratio of the penetration depth to the insulator thickness. In case of a voltage mode, a transmission line can be fabricated with a small ratio of the same quantity, which leads to a faster propagation velocity. This is a fault of the phase mode. But it might be possible to increase the velocity with decreasing the ratio of junction area to each unit section of a DJTL. Furthermore, parallel processing can be more easily carried out in the phase mode system compared with the voltage mode system, because all gates of the phase mode are ready to operate immediately after switching operation.

It is roughly estimated that the power loss is about 10^{-7} W/gate, because the voltage level is less than one-tenth compared with the gape voltage. The power loss of total system is the gate loss times the number of fluxoids that are moving simultaneously, because of the nonlatching mode, except for the dissipation in bias current source circuits. To achieve successful demonstration of the phase mode system, the following items must be improved:

1) the uniformity and the controllability of the maximum dc Josephson currents of many junctions that are fabricated over a large area;

2) the electromagnetic behavior, especially the problem of the magnetic flux trapping into superconducting electrodes. In the phase mode system, interfacing with external devices is not easier than that of the voltage mode system. Therefore, the bias current supply and three-dimensional interconnection between chips should be settled in the large phase mode system.

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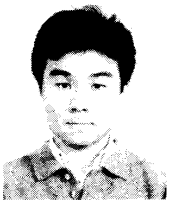

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