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Implementation of New Superconducting Neural Circuits using Coupled SQUIDs

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Abstract-A novel superconducting neuron circuit and two types of variable synapses, which are based on superconducting quantum interferometer devices (SQUIDs), are presented. A neuron circuit with good input-output isolation and steep threshold characteristics is accomplished using a combination of a single-junction SQUID coupled to a double-junction SQUID. The quantum state of the single-junction SQUID represents the neuron state, and the output voltage of the double-junction SQUID, which is operated in a nonlatching mode with shunt resistors, is a sigmoid-shaped function of the input. Both variable synapse circuits are composed of multiple shunted doublejunction SQUIDs. The first type changes its conductance value by using both superconducting and voltage states. The second variable synapse circuit changes its output current digitally by switching its bias currents. Besides numerical simulations of the circuit characteristics, we have fabricated superconducting neural chips in a Nb/AlO_x/Nb Josephson junction technology. The fundamental operation of each element and a 2-bit neural-based A/D converter have been successfully tested. A learning system with a variable synapse is also discussed.

I. INTRODUCTION

R ECENTLY, artificial neural networks have received extensive attention because of their potential for parallel and intelligent information processing. For example, they can rapidly compute good solutions to difficult optimization problems of the NP-complete class [1], and their functions can be programmed by several learning methods [2], [3]. Models of neural networks are, however, quite simple in comparison with ordinary computing devices; they consist of neuron devices which are connected to one another via synapse elements. In a network of nneurons, the activity of the *i*th neuron is described as

$$\tau \, dv_i/dt = \sum_{j=1}^n T_{ij} X_j + h_i - v_i, \qquad X_i = f(v_i), \quad (1)$$

where τ , X_i , v_i , h_i , and T_{ij} are a time constant, the output, the potential level, the threshold value, and the synaptic strength of the *i*th neuron bringing input from the *j*th one, respectively. $f(v_i)$ is a sigmoid-shaped function. Information is stored in the network as synaptic strengths.

Neural computation on a serial computer is very slow and lacks the fault-tolerance advantages of a parallel

The authors are with the Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai, 980 Japan. IEEE Log Number 9214848. architecture. Hence, if we wish to put the special features of neural networks to practical use, we need to use a fully parallel architecture. Several groups have reported the implementation of neural networks using semiconductor integrated-circuits [4]. However, power dissipation will be a serious problem when large scale networks are attempted, because of their huge number of interconnections. Accordingly, the key problem of hardware implementation of the networks is the realization of synapse devices having small size and low dissipation.

Superconducting Josephson circuits seem to be superior to semiconductor circuits for very large scale integration (VLSI) of neural networks, because of their ultra-high speed operation with very low power dissipation [5]. There are some proposals and experiments of superconducting implementation of neural networks [6]–[9]. But superconducting neural circuits, particularly synapse circuits with a variable weight, have not been sufficiently investigated yet.

We report new superconducting neuron and synapse circuits. They are composed of a combination of superconducting interferometer devices (SQUIDs) with shunt resistors. Besides the numerical simulations of the circuit characteristics, we have fabricated superconducting neural chips using a Nb/AlO_x/Nb technology, and their operation has been verified experimentally. Furthermore, a learning system using variable synapse circuit is discussed.

II. DESIGN, SIMULATION, AND MEASUREMENT OF NEW NEURAL CIRCUITS

As described above, a neural network is composed of massive neuron and synapse elements. In this section, we describe our new circuits for a neuron and a synapse. Particularly, we propose two types of variable synapse circuits.

We used JSIM [10] for the numerical simulation of circuits with Nb/AlO_x/Nb junction parameters; the Josephson critical current density $J_c = 1 \text{ kA/cm}^2$, the capacitance $C = 60 \text{ fF}/\mu\text{m}^2$, the gap voltage $V_g = 2.7 \text{ mV}$, and the product of the critical current and the subgap resistance at 2 mV (V_m value) was 20 mV.

The Josephson circuits were fabricated on a Si substrate using Nb/AlO_x/Nb tunnel junctions and Pb-In wiring with 5 μ m design rules. The targets of the J_c and the Au-In sheet resistance were chosen to be 1.0 kA/cm² and 0.96 Ω /square, respectively. Details of the fabrication process were reported in [9] and [11].

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We have designed and fabricated four types of 5×5 mm² chips which have 38 pads. The 2-inch wafer was sectioned to 36 chips. The junctions of the SQUIDs are $5 \times 5 \ \mu\text{m}^2$ or $10 \times 10 \ \mu\text{m}^2$. The average and the standard deviation of the J_c and the sheet resistance were 1.1 kA/cm², 0.19, 1.1 Ω /square, and 0.13, respectively.

During the measurement in liquid helium, the chips were shielded from environmental static magnetic fields by a double permalloy cylinder.

A. Neuron Circuit with Fixed Synapse

Fig. 1 shows our previous neuron circuit with fixed synapses [8], [9]. The threshold function is realized by using superconducting and voltage states of Josephson junctions. In this circuit, the equation of the current flowing to the *i*th neuron junction, which corresponds to (1), is described as

$$\sum_{j=1}^{n} (L_{ij}/R_{ij})(di_j/dt)$$

$$= \sum_{j=1}^{n} (1/R_{ij})V_j - \sum_{j=1}^{n} (1/R_{ij})V_i^* + I_i - (u_i + i^*)$$
(2)

$$i^* = \Phi_0 / (2\pi L_{JTL}) \left| (V_i^* - V_i) \, dt \right|,$$

where L_{ij} , R_{ij} , i_j , V_i , I_i , u_i , i^* , Φ_0 are the resistance and inductance values which connects the *j*th output to the *i*th input, the current flowing from the *j*th to the *i*th neuron, the voltage, the external bias current, the current flowing the *i*th neuron, the output current, and a flux quantum, respectively. The existence of i^* and the second term on the right-hand side is due to the incomplete input-output isolation. On the special condition that all of L_{ij}/R_{ij} are equal to τ , (2) can be rewritten as

$$\tau d(u_i + i^*)/dt = \sum_{j=1}^n (1/R_{ij})V_j - \sum_{j=1}^n (1/R_{ij})V_i^* + I_i - (u_i + i^*) \quad (3)$$

Equation (3) has the same form as (1) except for i^* and the second term on the right-hand side. Furthermore, if the time constants, L_{ij}/R_{ij} , are smaller than the switching time of the neuron junction (about 10 ps in simulation), we can neglect the left-hand side of (2). The equation after the neglect, except for the terms of i^* and V_i^* , corresponds to the simplest neuron model as follows,

$$v_i = \sum_{i=1}^{n} T_{ij} X_j + h_i.$$
 (4)

To reduce the second term in (2), we attach a superconducting inductance parallel to the neuron junction. Then the neuron junction works as the gate junction of a single-junction SQUID, and no dc-voltage appears across the junction. Furthermore, the quantum state "0" and "1" of the single-junction SQUID can be used as a neuron

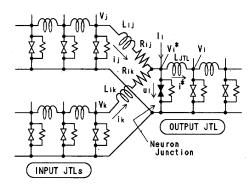
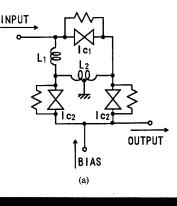


Fig. 1. Scheme of our previous neuron circuit with fixed synapses [7], [8].



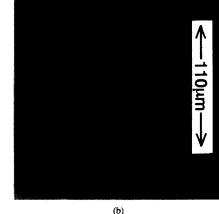


Fig. 2. New neuron circuit of coupled SQUIDs. (a) Equivalent circuit. (b) Photograph of the fabricated circuit. The circuit parameters are designed as $Ic_1 = 0.25$ mA, $Ic_2 = 1.0$ mA, $L_1 = 0.83$ pH, and $L_2 = 0.82$ pH. The double-junction SQUID is shunted by two 0.24 Ω resistors and operated under nonlatching mode.

state. The quantum state can be read out by a biased double-junction SQUID coupled to it. Then the output voltage (the frequency of fluxons) of the double-junction SQUID corresponds to the neuron output.

Fig. 2(a) and (b) show the equivalent circuit and the microphotograph of the new neuron circuit which is composed of the coupled SQUIDs (a single-junction SQUID

with a double-junction SQUID). To make the coupling stronger between the single-junction SQUID and the double-junction SQUID, we connect the inductances directly instead of using magnetic coupling. The center of the inductance L_2 is grounded for input-output isolation. The threshold characteristics (critical current pattern) of the coupled SQUIDs is determined by three parameters; $\alpha = Ic_1/Ic_2, \ \beta_1 = (L_1 + L_2)Ic_1/\Phi_0, \ \text{and} \ \beta_2 =$ $L_2 I c_2 / \Phi_0$. Fig. 3(a) and (b) show the calculated and the experimental threshold characteristics of the coupled SQUIDs. The calculation was executed at $\alpha = 0.25$, $\beta_1 =$ 0.20, and $\beta_2 = 0.40$ using the linearization method [12]. The critical current of the double-junction SQUID decreases abruptly when the quantum state of the singlejunction SQUID changes from "0" to "1". In the fabricated circuit, the quantum state could be read out by the 83–97% biased double-junction SQUID. Fig. 4(a) and (b) show the numerical and the experimental results, respectively, for input (current)-output (voltage) characteristics of the neuron circuit. The simulated and designed values of circuit parameters for Ic_1 , Ic_2 , L_1 , L_2 , a load resistor, were 0.25 mA, 1.0 mA, 0.83 pH, 0.82 pH, and 0.24 $\Omega,$ respectively. The fabricated inductances, L_1 and L_2 , were 0.80 pH and 0.81 pH, respectively. The 90% biased double-junction SQUID was shunted by two 0.24 Ω resistors and it was operated under nonlatching mode with Mc-Cumber parameter $\beta_c = 1$ [13]. There is no hysteresis in the both input-output characteristics because β_1 is designed to be small as 0.2. Fig. 4 proves that this circuit is able to work as a neuron with sigmoid-shaped transfer function. The results of the simulations have also proved that this neuron circuit has a good input-output isolation, and that it can follow an input signal as high as 5 GHz with a load inductor of 4 pH and a load resistor of 0.24 Ω .

It can be seen from (2) and (3) that the conductance value of the resistor, $1/R_{ij}$, represents the synaptic strength. The inhibitory synaptic connection $-T_{ij}$ is accomplished by $-V_i$ instead of $-(1/R_{ij})$. This is consistent with Dale's principle which states that the synapses from one neuron do not have both characteristics of excitation and inhibition. Fig. 5(a) shows the 2-bit analog to digital (A/D) converter of the correct reaction neural network (CRANN) [14]. An A/D converter is a good example of an optimization problem [15]. The network consists of two neuron circuits, one synapse resistor, analog input lines, and additional lines $(I_{MSB}$ and $I_{LSB})$ which are used to control the threshold of each neuron. The double-junction SQUIDs of the neuron circuits are biased to realize the inhibitory synaptic connection. Fig. 5(b) and (c) show the numerical and the experimental results for the operation of the 2-bit A/D converter, respectively. The output voltages of the most significant bit (MSB) and the least significant bit (LSB) have negative values. Fig. 6 shows the input-output characteristics of the A/D converter. The MSB output suppresses the LSB activity to represent "10" state. This A/D converter can operate with an input frequency larger than 1 MHz which was the maximum frequency limited by the conventional high-gain

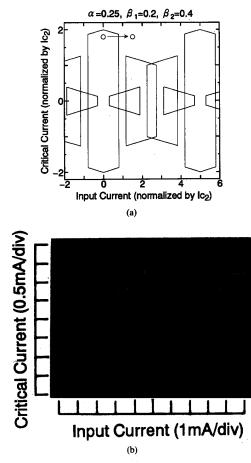


Fig. 3. Threshold characteristics (critical current patterns) of the coupled SQUIDs. (a) Numerical results calculated by using linearization method at $\alpha = 0.25$, $\beta_1 = 0.20$, and $\beta_2 = 0.40$. (b) Experimental result.

measurement equipment. It was confirmed by simulation that this network responds to input signals with frequencies as high as 500 MHz.

B. Variable Synapse Circuit (I): Variable Resistance Type

As described above, the conductance value of the resistor which connects two neurons represents the synaptic strength. One of our new variable synapse circuits is variable resistance type which is shown in Fig. 7(a). In this circuit two shunted double-junction SQUIDs are connected in series to the output line. The double-junction SQUIDs are used in both of the two states; superconducting state and voltage state. Fig. 7(b) shows the simulated current-voltage characteristics of this circuit. When no control current is supplied to any double-junction SQUIDs, they are superconducting and no voltage appears across them. When control current, I_1 or I_2 , is supplied to one of the double-junction SQUIDs and the input current exceeds its critical current, the resistance value increases up to that of shunt resistors after the double-junction SQUID switches to the voltage state, as shown in Fig. 7(b) by dash lines. It means that the conduc-

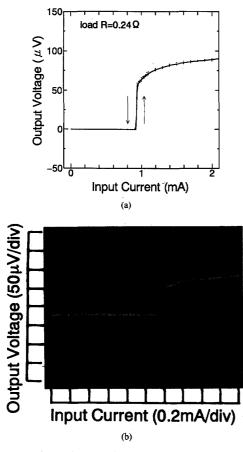


Fig. 4. Input (current)-output (voltage) characteristics of the neuron circuit with a load resistor. (a) Numerical result with a load resistor 0.24 Ω . The double-junction SQUID is biased to 90% of 2*I*c₂. (b) Experimental result. The double-junction SQUID is biased to 88% of 2*I*c₂.

tance value of the circuit, $1/R_{ij}$, can be changed by a control current. Fig. 7(c) shows the experimental results of current-voltage characteristics. The fabricated inductances L_1 and L_2 were both 1.6 pH. Because the fabricated double-junction SQUID has no damping resistors, some resonance steps are observed.

C. Variable Synapse Circuit (II): Variable Current Source Type

Fig. 8(a) shows the second type of variable synapse circuit having a variable current source. This circuit consists of two shunted double-junction SQUIDs which are magnetically coupled to the output line of a neuron, and which are connected directly to the next neuron through a resistance R_0 . The shunted double-junction SQUIDs are operated in the nonlatching mode. If no bias current is supplied to either double-junction SQUID, no output of the synapse circuit comes out to the next neuron. When one or more double-junction SQUIDs are externally biased and their critical currents are suppressed by the neuron output, they switch to the voltage state and let an

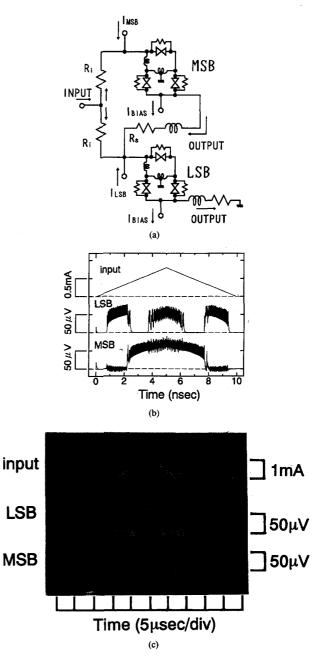


Fig. 5. 2-bit analog to digital (A/D) converter of the correct reaction neural network (CRANN). (a) Equivalent circuit. R_i and R_s are designed to be 0.94 Ω and 0.24 Ω , respectively. (b) Numerical and (c) experimental results of the A/D converter operation. The outputs of the most significant bit (MSB) and the least significant bit (LSB) were experimentally measured as their voltages. The output currents and voltages of each bit are represented as inverted values.

output current flow to the next neuron. If we choose the resistance values of shunt resistors of the double-junction SQUIDs as $R_1 = R_0$ and $R_2 = 2R_0/5$, the ratio of each averaged output current to the next neuron becomes 2:1. Therefore, we are able to change the current

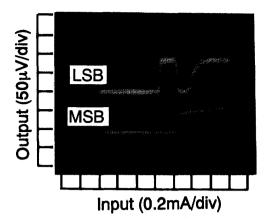


Fig. 6. Input-output characteristics of the fabricated A/D converter. The MSB output suppresses the LSB activity to let "10" state appear.

flowing to the next neuron digitally by switching the bias current of the double-junction SQUIDs. Fig. 8(b) shows the numerical result of the operation of Fig. 8(a). The current flowing to the next neuron is changed digitally by the bias currents to the double-junction SQUIDs. Fig. 8(c) shows the experimental result of the output current from the synapse in Fig. 8(a) as a function of the neuron input for four states of the synapse double-junction SQUIDs. The synapse output current was measured as the sum of the voltage across the R_0 by using a differential amplifier. The fabricated mutual inductance was 1.9 pH. It was confirmed that the external currents can control the synapse output by 2^2 levels.

III. DISCUSSION

A. Neuron Circuit

As described above, the coupled SQUIDs work as a neuron with a sigmoid-shaped function and good input-output isolation. The power dissipation was estimated as 0.26 μ W with a load resistor of 0.24 Ω . The area occupancy of the fabricated circuit shown in Fig. 2(b) was $130 \times 110 \ \mu$ m², which was designed with $J_c = 1 \ kA/cm^2$ and 5 μ m rule. Assuming $J_c = 10 \ kA/cm^2$ and 1 μ m design rule, the area occupancy of a neuron can be reduced as much as a factor of 1/50. This circuit does not use magnetic coupling, and hence, it might be possible to cut down the cell area further by a factor of 1/100 with submicron design rule by replacing geometric inductance with kinetic inductance [16], [17].

The margin for the bias current of the fabricated neuron circuit is not large, about $\pm 8\%$. As for the inductance values, they might be too small to eliminate the effects of the parasitic inductances. These problems will be solved by parameter optimization. For example, it will be possible to increase the margin up to about $\pm 30\%$ for the neuron circuit [12].

If the input current to the single-junction SQUID of the neuron increases or decreases without limit, the double-junction SQUID switches between the superconduct-

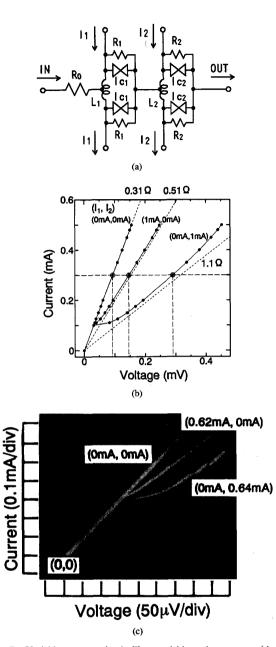


Fig. 7. Variable synapse circuit (I); a variable resistance type (three values). (a) Equivalent circuit. (b) Numerical and (c) experimental results of current-voltage characteristics of the circuit. The circuit parameters are designed as $Ic_1 = Ic_2 = 0.25$ mA, $L_1 = L_2 = 1.0$ pH, $R_0 = 0.31 \Omega$, $R_1 = 0.40 \Omega$, and $R_2 = 1.5 \Omega$.

ing state and the voltage state periodically, which causes the limitation of fan-in. Thus an input current limiter should usually be put before a neuron circuit in order to keep its sigmoid-shaped transfer function. The input limiter increases the number of fan-in. On the other hand, a nonmonotonic neuron model has been proposed to improve the dynamics of autocorrelation associative memory [18]. Hence the periodic output of the coupled SQUIDs

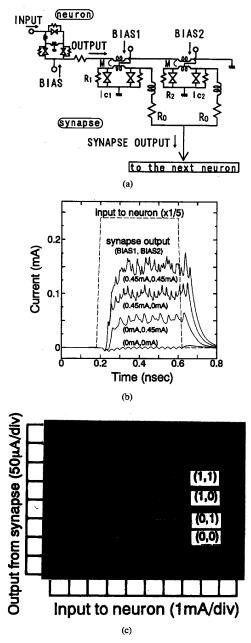


Fig. 8. Variable synapse circuit (II); a variable current source type (2^2 values) . (a) Equivalent circuit. (b) Numerical result of the operation of (a). (c) Experimental results of the neuron input-synapse output characteristics. The circuit parameters are designed as $Ic_1 = Ic_2 = 0.25 \text{ mA}$, M = 3.2 pH, $R_0 = 0.94 \Omega$, $R_1 = 0.94 \Omega$, and $R_2 = 0.38 \Omega$.

with larger input range would enhance the ability of associative neural networks.

We use an ordinary superconducting line to transmit the output fluxons of a neuron. If it is necessary for a neuron circuit to drive a lot of another neurons, we can use biased JTLs, which are active transmission lines, at the point of the branches. Numerical simulation has proved that the fan-out operation of the phase-conserving branch [19], [20] makes it possible to distribute fluxon array to plural neurons, though the use of JTLs might reduce the integration scale.

B. Variable Synapse Circuit

We have proposed and demonstrated two types of new variable synapse circuits.

The area occupancy of a fabricated double-junction SQUID of the variable resistance type was $120 \times 115 \ \mu m^2$. There are two problems in this circuit. The number of double-junction SQUIDs required to achieve *n* levels of synaptic strength is as large as (n - 1). The other problem is that this circuit changes the load impedance of a neuron directly, which may cause the change of the neuron output level.

On the other hand, one double-junction SQUID of the fabricated synapse circuit of variable current source type occupied $120 \times 75 \ \mu m^2$. In this circuit, the number of double-junction SQUIDs required to achieve *n* synaptic levels is reduced to $\log_2 n$. The load impedance of a neuron circuit is almost fixed.

Accordingly, the synapse of a variable current source type is more advantageous than that of a variable resistance type.

If the synapse control signals are not supplied from an external computer, it is necessary to construct the internal control circuit. Using coupled SQUIDs with $\beta_1 \approx 1$ instead of double-junction SQUIDs has probability of solving this problem. The single-junction SQUID would work as a flux-quantum memory which could control the critical current of the coupled double-junction SQUID.

C. Learning System

Learning, which is one of the special features of neural networks, means self-organization of a network by changing synaptic strengths according to a certain learning rule. Hebb's learning rule is one of the learning rules which receive broad support. It says that if both the *i*th and the *j*th neurons fire at the same time, the excitatory synapse strength T_{ii} has a greater chance to become larger.

Fig. 9 shows the schematic diagram to implement Hebb's rule into the variable current source type synapse. In the learning process, the outputs of the *i*th and the *j*th neuron come into an AND circuit and its output is added at a Counter. The Counter supplies bias currents to the synapse circuit directly, or produces write signals to the coupled SQUIDs memory described above. Then the synaptic strength T_{ij} increases according to Hebb's rule. The AND and the Counter circuits can be constructed by conventional Josephson digital circuits including single-flux-quantum systems [21]–[23], which we are investigating at present.

IV. CONCLUSION

Novel superconducting circuits for a neuron and two types of variable synapses, which are based on SQUIDs, are presented. Josephson circuits seem to be superior for VLSI of the neural networks because of the high-speed operation under very low power dissipation. A neuron

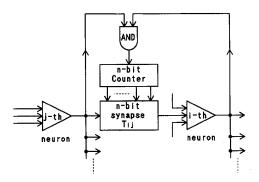


Fig. 9. Schematic diagram of the implementation of Hebb's learning rule with the *n*-bit synapse of a variable current source type.

circuit with good input-output isolation and steep threshold characteristics is accomplished using a combination of a single-junction SQUID coupled to a double-junction SQUID. The quantum state of the single-junction SQUID represents the neuron state, and the output voltage of the double-junction SQUID, which is operated under a nonlatching mode with shunt resistors, is a sigmoid-shaped function. One of the variable synapse circuits changes its conductance value digitally. Another variable synapse circuit is a variable current source in which the output current can change digitally. Both synapse circuits consist of multiple shunted double-junction SQUIDs. Besides numerical simulations of the circuit characteristics, we have fabricated superconducting neural chips using a Nb/AlO_x/Nb Josephson junction technology. The fundamental operation of each element and a 2-bit A/D converter are successfully demonstrated. A learning system based on Hebb's rule with variable-current-source type of synapse is also discussed.

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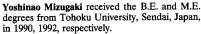
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