Fluxoid motion in phase mode Josephson switching system

FLUXOID MOTION IN PHASE MODE JOSEPHSON SWITCHING SYSTEM

K. Nakajima, G. Oya, and Y. Sawada
Research Institute of Electrical Communication,
Tohoku University, Sendai 980, Japan

Abstract

We have investigated the possibility of the phase mode operation, i.e. the mode to transfer the fluxoid, not to transfer the voltage pulse, of Josephson switching system by fabricating a rsistively coupled D.C. SQUID's array and 4J-loop which are expected to be advantageous in miniaturization by using its large kinetic momentum effect. The threshold characteristics of these superconducting loops and its LI_c dependence agreed with the theoretical predictions. The phase mode logic actions were verified to operate really in a resistively coupled D.C.SQUID's and a coupled D.C. SQUID with a 4J-loop. A computer simulation showed that a resistively coupled SQUID's array acts both on phase mode and voltage mode by changing the circuit parameters, but that the two modes are clearly separated in a parameter space. Finally we have shown a total system configuration of the phase mode operation. For the power loss and the information processing speed, the phase mode was verified to have an advantage over the ordinary voltage mode by two orders of magnitude.

Introduction

We have investigated in this paper the possibility of the phase mode operation[1] of Josephson switching system by fabricating a resistively coupled D.S.SQUID's array and 4J-loop's which are superconducting loops containing four series Josephson junctions and show large kinetic momentum quantum effect.[2] The voltage mode devices which are actively being investigated and constructed nowadays depend for its operation on the existence of two stable current carrying states at V=0 and $V=V_{gap}$.[3] On the other hand the phase mode devices depend on the many stable states separated from each other by 2π in the phase difference plane. In the phase mode all logic function can be achieved with the interactions between fluxoids which are employed as information bits without occupying voltage states. Although two kind of phase mode action have already been reported as flux shuttle and soliton device[5] by using continuous Josephson lines, we report in this paper the first phase mode operation in the circuits constructed by D.C.SQUID and 4J-loop where one can expect higher density system.[2] To study the difference in characteristics of the two modes, a computer simulation was done for a resistively coupled nonsymmetrical D.C.SQUID's array which showed that a resistively coupled SQUID's array acts both on phase mode and voltage mode by changing the circuit parameters, but that the two modes are clearly separated in a parameter space. Finally we have shown an example of total system configuration of the phase mode operation.

Fabrication and characteristics of basic elements

We have fabricated D.C.SQUID's and 4J-loop's by using Pb alloy and rf plasma oxidation. The fabrication process is the following, 1). a 4000Å-thick niobium layer is deposited on a Si wafer by electron beam evaporation, 2). the surface of niobium layer is anodized by 1000Å, 3). SiO is deposited as an insulating layer with a thickness of 3000Å, 4). 1000Å thick resistors are deposited using a AuIn alloy, 5). a 1500Å-thick base-electrode is formed by sequential evaporation of gold, lead, and indium, 6). A SiO layer with thickness of 3000Å is formed to demarcate the circular junction areas, 7). A tunneling oxide barrier is formed by rf plasma oxidation method, 8). A 4500Å-thick counter electrode is deposited by the successive evaporation of lead, gold, and lead. The 4J-loop we have fabricated has four junctions of 5 μm diameter. The minimum line width of the pattern is 10 μm.

The most basic characteristics of 4J-loop's are threshold patterns which demarcate the voltage states and the non-voltage states of 4J-loop's. Figure 1 shows the calculated threshold patterns of a 4J-loop by using a linearized approximation. The equivalent circuit is shown in the inset. In the figure the I_c's of the four junctions are same, the parameter is the value of LI_c, and the diamond-shaped patterns or triangle patterns show the quantum states of the loop. If $LI_c<\Phi_0$, the quantum states more than quantum number $n=\pm 2$ do not exist in contrast with D.C.SQUID.

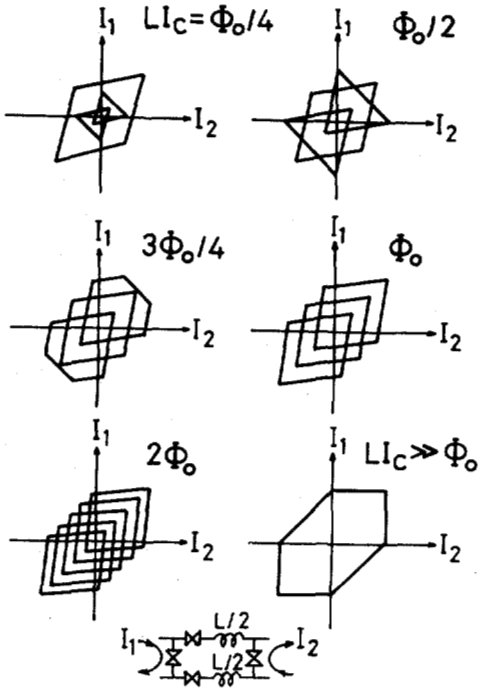

Fig.1. Threshold curves of a 4J-loop calculated by using the inset equivalent circuit and linearized approximation.

In order to obtain a threshold curve experimentally, we must observe all the junctions voltages. At present time we measure each junctions voltage individually, after that we superpose every pattern to get the whole threshold curve. Figure 2 shows the observed threshold curve where voltages of two junctions were measured. The two junctions correspond to J_1 and J_2 junctions shown in the equivalent circuit in Fig. 1. The whole threshold curve is shown in Fig. 3. LI_c was estimated to be $\sim 0.36\Phi_0$ from the measurement of D.C.SQUID which was fabricated in the same pattern as the 4J-loop. This estimation agrees with the theoretical prediction of Fig. 1. It can be seen from Fig. 3 that only three quantum states $n=0,\pm 1$ exist in contrast with D.C.SQUID where there are many quantum states even though LI_c is smaller than Φ_0. These quantum states and vortex transitions in the loop are used when the logic circuits

Manuscript received November 30, 1982

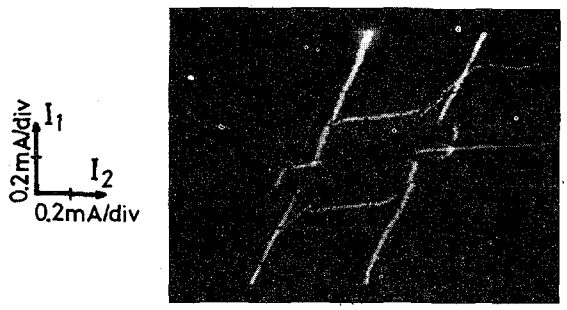

Fig. 2. Observed threshold curve of the 4J-loop where voltages of only two junctions were measured which correspond to J_1 and J_2 junctions shown in the equivalent circuit in Fig. 1.

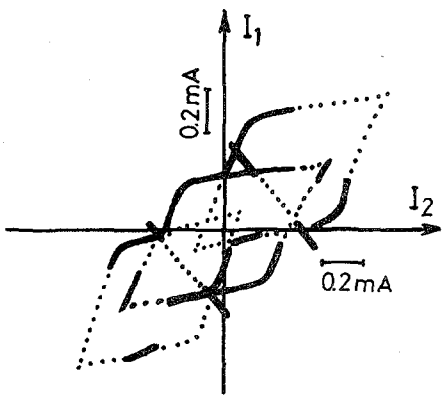

Fig. 3. Observed whole threshold curve of the 4J-loop. LI_c is estimated about $0.36\Phi_0$. I_1 and I_2 correspond to I_1 and I_2 shown in Fig. 1, respectively.

are operated in the phase mode. D.C. SQUID and 4J-loop are valuable basic elements for the phase mode logic system.

Experimental logic operation

We have fabricated elementary logic circuits of phase mode system which are constructed of the resistively coupled D.C.SQUID's or 4J-loop's. Figure 4 shows a 2-input phase mode logic circuit consisting of four D.C.SQUID's connected by AuIn alloy resistors, and its simplified equivalent circuit. The each circular Josephson junction has a diameter of 8 μm, and minimum line width is 10 μm. This circuit was constructed to confirm SHIFT, OR, and AND logic operations in phase mode.

As the first step of logic operation, resistvely connected D.C.SQUID's 2 and 3 of the circuit were used to examine the shift of a single fluxoid from 2 to 3. Figures 5(a) and 5(b) show the threshold curve of SQUID 2 and I-V chracteristics of SQUID 3, respectively, LI_c's of SQUID's 2 and 3 were $1.8\Phi_0$ and $0.3\Phi_0$, respectively. SQUID's 2 and 3 were used as a generator and a detector of a fluxoid, respectively. First the bias current I_{gb} for SQUID 2 was applied to set SQUID 2 in the state of n=0, and to determine the propagating direction of a fluxoid. But it is required that I_{gb} is smaller than the smallest value of the voltage transition part of threshold curve of SQUID 2. Then I_{gc} was applied in the direction shown in the equivalent circuit of Fig. 5 and increased until the SQUID 2 switches from n=0 to n=1 state. By this operation a single fluxoid is to be sent into the inside of SQUID 2

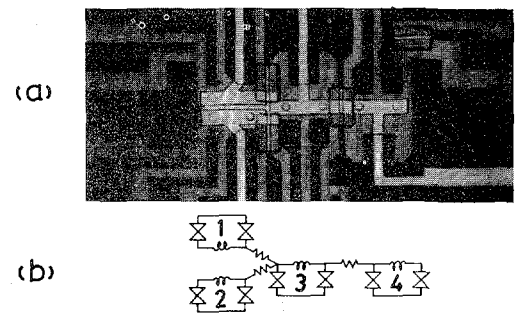

Fig. 4. (a) Photograph of a fabricated 2-input phase mode logic circuit consisting of four D.C.SQUID connected by AuIn alloy resistors. (b) Its simplified equivalent circuit.

through the left side junction. When I_{gc} is reset to 0, the state of n=1 is no more stable, so the fluxoid inside would be emitted through the right side junction. These motions are expected by the threshold curve of SQUID 2. We can measure the individual threshold curve of SQUID 2 and 3, because they are decoupled by a resistor. Inductive coupling would be more essential than the resistive coupling in the phase mode operation, if we do not have to measure the threshold curve of each SQUID. The fluxoid emission is accompanied by a current pulse sent to SQUID 3 through the connecting resistor between SQUID 2 and 3. If SQUID 3 is enough biased it would be switched to a voltage state by the trigger of the small current pulse from SQUID 2. Therefore a detection of fluxoid shift is achieved by observing the voltage of SQUID 3.

Figure 6(a) shows an experimental SHIFT logic operation observed by using the SQUID 2 and 3 whose characteristics are shown in Fig. 5. Notice that Vd appears without Vg appearing in this mode. It was confirmed in this measurement that the voltage transition of the detector did not occur when I_{gc} was reduced to zero. The voltage mode operation was also verified to be achieved in our circuits as CIL gates by changing bias current and control current conditions. For a comparison the voltage mode operation in the same circuit is shown in Fig. 6(b). Notice that Vd appears in the existence of both Vg and Vd. The SHIFT logic operation shown in Fig. 6(a) is also achieved by using SQUID 1 and 3, so this operation corresponds to OR logic in the phase mode.

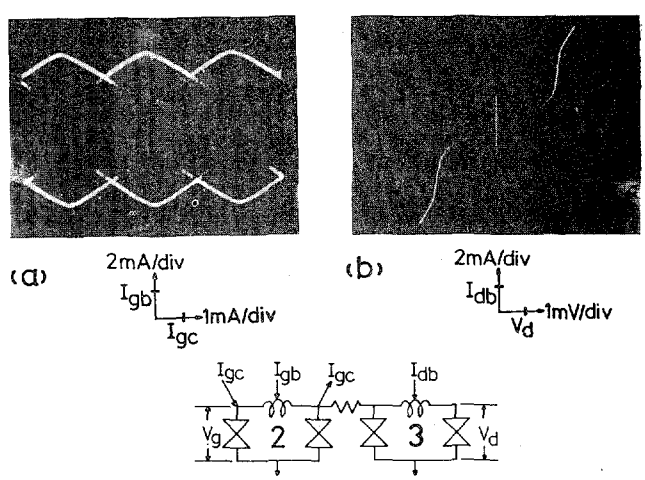

Fig. 5. Threshold curve (a) and I-V characteristics (b) of SQUID 2 and SQUID 3 shown in Fig. 4, respectively.

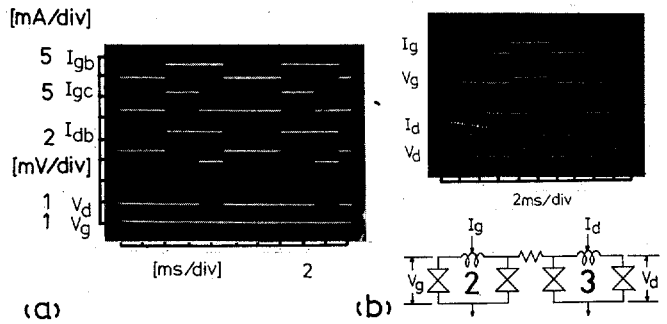

Fig. 6. (a) Experimental SHIFT or OR logic operation in the phase mode circuit shown in Fig. 4.
(b) Voltage mode operation in the same circuit.

An AND logic operation in the phase mode is shown in Fig. 7. Notice that Vd appears in the existence of both I_{gc1} and I_{gc2} which are the control currents of SQUID 1 and 2, respectively. It was confirmed in this measurement that Vd did not appear, when either I_{gc1} or I_{gc2} was reduced to zero. In this case the value of the connecting resistor was so small (~0.08Ω) that the generators voltage appeared by the reflection from the detector.

These phase mode action have also been observed in a circuit of a resistively coupled D.C.SQUID and a 4J-loop. In order to confirm the phase mode operation, a Josephson sampling system are being prepared.

Phase mode operation separated from voltage mode

To study the difference in characteristics of the two modes, a computer simulation was done for a resistively coupled nonsymmetrical D.C.SQUID's array which are ordinarily used as the voltage mode devices as shown in Fig. 8. This circuit acts on both the phase mode and the voltage mode depending upon the circuit parameters. The phase and the voltage mode actions in the same circuit are separated from each other in the circuit parameter plane, having a clear boundary as shown in the same figure where $\gamma=Ib/Ic$, $\alpha=Rc(2\pi IcC/\Phi_0)^{1/2}$, $\Gamma=G(\Phi_0/2\pi IcC)^{1/2}$, $2\pi LIc=0.5\Phi_0$, $2\pi LcIc=0.4\Phi_0$. ○ and ▲ denote the phase and the voltage mode regions respectively. ■ denotes the signal attenuation region. It can be seen from the figure that the phase mode operation can be achieved in the region of smaller γ compared to the voltage mode operation. The voltage hold time in the phase mode is nearly equal to the switching time of a junction ~10ps, but in the voltage mode that is equal to the cycle time ~ns owing to the latching mode. Therefore, for the power loss and the information processing speed and density, the phase mode system have an advantage over the voltage mode system more than two order.

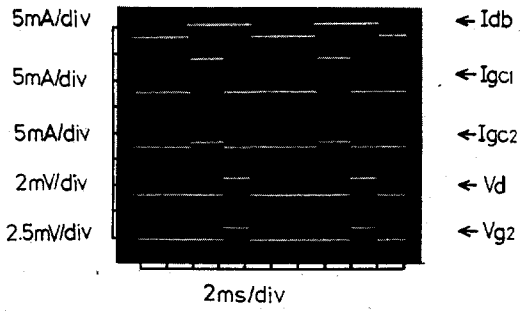

Fig. 7. Experimental AND logic operation in the phase mode circuit shown in Fig. 4.

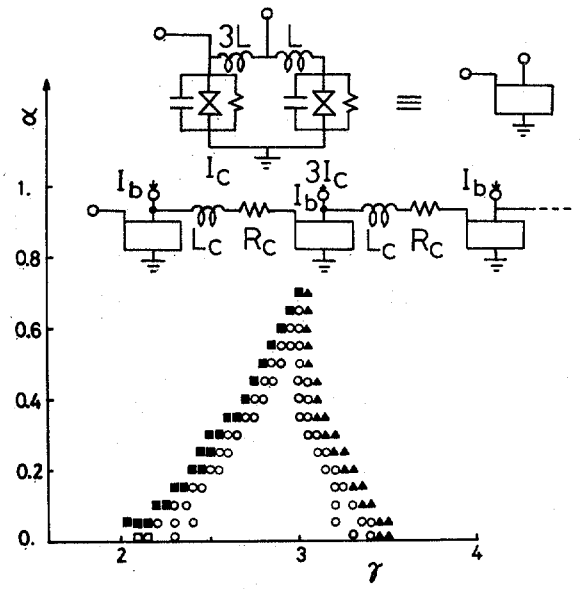

Fig. 8. Signal transport regions in the circuit parameter plane which circuit is shown on the upside. ○ and ▲ denote the phase and the voltage mode regions, respectively. □ denotes the signal attenuation region.

Total phase mode computer system

Individual logic functions of the phase mode system have been already proposed by us.[6] But systematic computer operations in the system has not been investigated yet. The system operation in the phase mode is largely different from in the ordinary voltage mode which is similar the one used in a computer system constructed by semiconductor devices. We present a simple but total phase mode Josephson computer system in this section. The computer is binary and asynchronous. Word length is 6 bits. The instruction format consists of the 3-bit operation-code part and the 3-bit address part. So capacity of memory is 48 bits. Available instructions of the maching is 7. The number of Josephson junctions to be used in the computer is estimated to be about 8000, without counting the parts of signal transmission lines. In the system five elements to be constructed by oxide tunnel junctions are used which are D.C.SQUID, 4J-loop, resistor, discrete Josephson transmission line (DJTL), and trigger turning

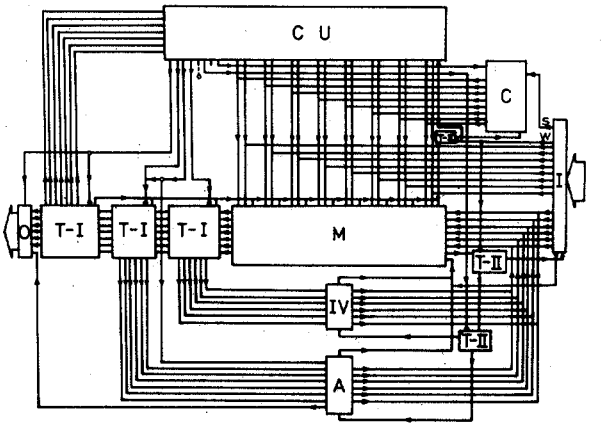

Fig. 9. System configuration of a phase mode Josephson computer.

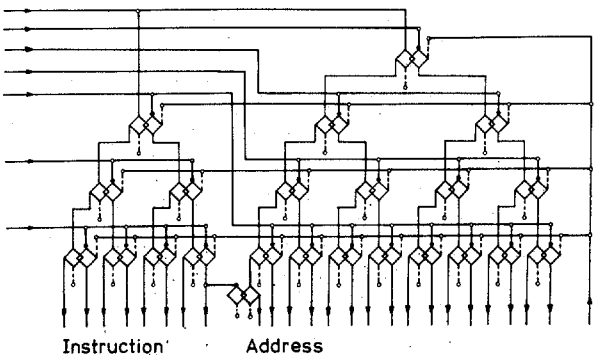

Fig. 10. Control unit of the phase mode Josephson computer system shown in Fig. 9.

point (Ttp). Figure 9 shows the configuration of the computer where I, C, CU, M, IV, A, O, T-I, and T-II denote input, counter, control unit, memory, inverter, adder, output, terminal I and II, respectively. S and W are signals to start the machine and to store data in the memory by manual, respectively. Lines with arrows, circles, and broken line denote DJTL's. Ttp's, and resistor. Solid circles mean setting operations of a single fluxoid. For example, the control unit is shown in Fig. 10 where double squares denote the function shown in Fig. 11. The bold line used in Fig. 11(1) denotes a annihilation function of two colliding fluxoids as shown in its right hand side. Sqares denote 4J-loop's. The function of Fig. 11(1) is explained by using the truth table also shown in this figure, namely, the propagating direction of fluxoid from I is switched to the output a or b depending upon the fluxoid setting at the 4J-loop. It is expected that this function is also accomplished by the construction of Fig. 11(2). The symbol which is used to denote this function is the right hand side in the figure. The control unit shown in Fig. 10 as same as the other computer elements in our system is constructed by using many basic elements shown in Fig. 11. The address part of the control unit is connected with the memory. The basic method of the machine operation is that the propagating directions of a single fluxoid are controlled by the single fluxoid setting at a 4J-loop on the way of the propagating fluxoid. A more detailed explanation of the machine operation will be presented in a forthcoming paper.[7]

Conclusion

We have investigated the possibility of the phase mode operation of Josephson switching system by fabricating a resistively coupled D.C.SQUID's array and 4J-loop which are expected to be advantageous in dense packing by using its large kinetic momentum effect. The threshold characteristics of these superconducting loops and its LIc dependence agreed with the theoretical predictions. The phase mode logic actions SHIFT, OR, and AND were verified to operate really in a resistively coupled D.C.SQUID's and a coupled D.C.SQUID with a 4J-loop. A computer simulation showed that a resistively coupled SQUID's array acts both on phase mode and voltage mode by changing the circuit parameters, but that the two modes are clearly separated in a parameter space. Finally we have shown a total system configuration of the phase mode operation. It is roughly estimated that the machine will provide about 200MIPS of computing power. The power loss is about 10^{-7}w/gate, and is about μW in the total system without counting the dissipation of current source part. It would be expected that for utilizing fluxoids as information bits the phase mode system is more favourable to data flow machine than voltage mode system.

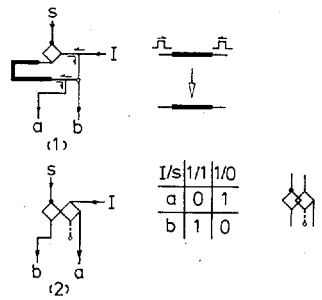

Fig. 11. Basic elements of the phase mode computer system. Squares denote 4J-loop's. S and I denote a setting fluxoid and a input fluxoid, respectively. a and b are two outputs. Circuits (1) and (2) have the same function which is explained by the truth table inset in this figure. The right side figure is a symbole for the circuits.

References

1. K. Nakajima and Y. Onodera, 'Logic design of Josephson network II". J. Appl. Phys., Vol. 49, pp.2958-2963, 1987.

2. K. Nakajima and Y. Sawada, "Numerical analysis of vortex motion in two-dimensional array of Josephson junctions", J. Appl. Phys., Vol. 52, pp. 5732-5795, 1981.

3. J. Matisoo, "Overview of Josephson technology logic and memory", IBM J. Res. Develop., Vol. 24, pp. 113-129, 1980.

4. T. A. Fulton and L. N. Dunkleberger, "Experimental flux shuttle", Appl. Phys. Lett., Vol. 22, pp. 232-233, 1973.

5. T. V. Regeevakumar, "A soliton device", IEEE Trans. Mag., Vol. MAG-17, pp. 591-594, 1981.

6. K. Nakajima, Y. Ogawa, and Y. Onodera, "Computer logic circuits using flux quantum transmission lines", Systems computers controls, Scripta electronica japonica III, Vol. 8, pp. 35-43, 1977.

7. K. Nakajima and Y. Sawada, "Phase mode Josephson computer system", to be published.