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We present experimental results on elementary phase-mode Josephson circuits whose combinations enable us to construct a total data processing system which is expected to be superior to the ordinary voltage-mode Josephson computer in several respects. In the phase-mode system a device depends for its operation on the existence of many stable states differing from one another by integer multiples of 2π in the phase plane. The total system is considered to be a prototype of quantum computer systems where physical quantum states are employed as logic states of information processing. By using the fabricated elementary circuits composed of SQUIDs and two types of branching points we have experimentally confirmed AND, FAN-OUT, FAN-IN operations, etc. We have also proposed an INHIBIT circuit, and presented the experimental results on the INHIBIT circuit.

I. INTRODUCTION

A superconducting Josephson computer system has great potential as one of the future computer systems because of its high-speed switching time (~ 10 ps) and low-power dissipation (~ 500 nW per circuit).[1] To realize ultra-high-performance computers dense packaging is required to avoid the propagation delay of signals due to the maximum light velocity. A problem in dense packagings with current and projected semiconductor large-scale integration (LSI) circuits of sufficiently high performance arises due to the high levels of power dissipated on chips during circuit operation. Although future miniaturization of semiconductor circuits will reduce power dissipation per circuit, it will not alleviate this problem in semiconductor technology, since the density of circuits would go up faster than the rate with which the power per circuit decreases, thus causing the chip power density to remain high, especially when higher switching speed is demanded.

Since the power dissipation of Josephson circuits, for current experimental circuits, is more than three orders of magnitude smaller than for semiconductor devices, they may not suffer from this problem. Low dissipation also permits resistive termination of all strip lines on-chip. The low operating temperature of Josephson circuits allows the use of superconducting strip lines and ground planes with zero electrical resistance. The thermal energy is about 100 times smaller at 4 K than at 360–380 K where semiconductor circuits are operated. This corresponds to a smaller thermally induced electrical noise, and helps to maintain a good signal-to-noise ratio even when signal bandwidth is increased and signal energy is reduced.

We have presented a phase-mode system, a model of Josephson computer systems in which quantized vortices accompanied by magnetic flux (fluxons) are employed as information bits, and in which all logic functions are achieved by interactions between fluxons.[2] In contrast, ordinary voltage-mode system operations are based on the existence of two stable current carrying states at $V=0$ and $V=V_{\rm gap}$.[1] ($V_{\rm gap}$ is the voltage corresponding to the superconducting gap energy.) The phase-mode system is superior in power dissipation by more than two orders to the voltage-mode system, and it has a faster switching time than that of the voltage mode.[3] The voltage-mode circuits are used in the so-called "latching" mode of operation in which they have to be reset in each cycle by reducing bias currents. On the other hand the phase-mode operation does not require any reductions of the bias currents, and therefore is free from punch-through phenomena.[4] The voltage-mode logic gates are current-controlled devices which are switched by currents through their control windings. These circuit operations in the voltage-mode might lead to complex changes of current paths and therefore complex changes of magnetic fields surrounding the circuits. These changes of magnetic fields, the main cause of the circuit errors, induce the flux trappings in the circuits. On the other hand the phase-mode logic gates are fluxon-controlled devices, which are switched by fluxons. This circuit operation does not induce complex changes of current paths. The voltage-mode system requires the gap voltage ($\sim$mV) to distinguish logic states, while the phase-mode system does not require any dc voltage. Logic states are distinguished by the number of fluxons in the phase-mode system. The fluxon number is conserved inside the superconducting circuits. A biased Josephson transmission line (JTL) is an active transmission line for fluxon propagations, and propagating directions of fluxon are decided by the bias current direction and the polarity of the fluxon when a fluxon propagates on this line. A propagating fluxon causes a $\sim$10-ps and $\sim$100-μV voltage pulse. But in static states no voltage and thus no power dissipation is associated with the fluxon because it consists of the superconducting current vortex. The use of these particlelike characteristics on the active transmission lines (JTLs) would remove the uncertainty of the binary identity in a data processing system. Also, one can easily construct storage circuits or memory circuits with them. To achieve complete phase-mode operations, at least two kinds of branches of the JTL and a universal operator constructed by JTLs is required.[2,5] We have already reported the experimental results for a fluxon-antifluxon annihilation on a JTL[6] and a FAN-OUT operation (fluxon creation) of one kind of JTL branch.[7]

In this paper we present experimental results of two kinds of branch circuits composed of discrete Josephson transmission lines which show AND, FAN-OUT, FAN-IN oper-

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ations, and switching operations for propagating direction of fluxons. Next we discuss the ICF (INHIBIT controlled by a fluxon) gate which is one of the universal operators in Boolean algebra. We also present preliminary experimental results for the ICF gate composed of the two kinds of branch circuits. These experimental results show that the phase-mode logic elements perform expected functions, and the combinations of the elements would enable us to construct a total logic system. The phase-mode Josephson LSI circuit chips, although quite different in their principle of operation, can be fabricated similarly to the voltage-mode Josephson LSI chips.[8,9] A data processor of the phase mode is estimated to be superior in processing speed, information density, and power loss to the ordinary voltage-mode system.[10] The total system is considered to be a prototype of the future quantum computer systems where physical quantum states are employed as logic states of information processing in a molecular device, the ultimate device of miniaturization.

II. TWO BRANCHES AND THEIR COMBINATION

In order to achieve all necessary logic functions by using interactions between fluxons, one has to investigate the various characteristics of fluxons on the Josephson transmission lines (JTLs). The JTL we use is discrete as shown in Fig. 1, because the discrete JTL is convenient for constructing line branches. We have already proposed[5] the two kinds of branch circuits shown in Fig. 1. All logic functions can be made by using the two branch circuits.[2] The following phase relations hold, respectively, at the first and the second branch points in Fig. 1,

$$\phi_1|_{bp} = \phi_2|_{bp} = \cdots = \phi_N|_{bp} , \tag{1}$$

$$\sum_{i=1}^{N} \phi_i|_{bp} = 2\pi n \quad (n \text{ is an integer}) , \tag{2}$$

where ϕ_i is the phase difference of the ith line branch, and N, the number of branches, is 3 in the following experiments. From these equations we call the first branch the "phase-conserving branch (p.c. branch)," and the second branch the "phase-distributing branch (p.d. branch)."

The expected behavior of a fluxon at the p.c. branch circuit is as follows.

(1) The propagating fluxon stops at the p.c. branch point, when the speed of the fluxon is below a critical value.[5] The resting fluxon can be reset by the second fluxon which is sent to the branch point through the second line. Then two fluxons combine with each other, and propagate on the third line as one fluxon ("SET and RESET" operation or "AND" operation).

(2) The single fluxon propagating into any one branch of the p.c. branch point will initiate a single fluxon on each of the two connected branches under the requirement of the magnetic flux continuity, when the fluxon has enough kinetic energy ("FAN-OUT" operation or fluxon creation). We have already reported the experimental results confirming the second expected behavior ("FAN-OUT").[7] In that experiment our Josephson sampler caught the fluxon waveform and confirmed that a single fluxon input initiated a single fluxon on each of the other two branches. These characteristics can be used as a FAN-OUT operation or a bit creation in logic systems.

The expected behavior of a fluxon at the p.d. branch circuit is as follows.[5]

(1) When a single fluxon of an intermediate kinetic energy propagates on any one line toward the p.d. branch point, it will initiate a single fluxon on only one of the connected lines. Namely, the initial fluxon will be led to only one of the connected lines ("line selection"). This behavior can be used as a switching operation for propagating directions of fluxons or a FAN-IN operation in logic systems.

(2). When the initial fluxon has a small kinetic energy (a small line bias current), it stops at the branch point.

(3) When the initial fluxon has a large kinetic energy (a large line bias current), it will initiate a single fluxon on each of the two connected branches, and an antifluxon will be sent back to the input line (a pair creation). Namely a fluxon-antifluxon pair is created under the requirement of the quantum mechanical condition.

The nonlinear switching device which is used in our logic circuits (phase mode) is a Josephson junction. But the switching operations of the devices are different from those of the ordinary voltage-mode system. In the phase-mode system the Josephson junction is used as a gate controlling the transit of a single magnetic flux quantum or a single fluxon which is localized in space and conserved as a whole. The propagating fluxon causes ~10-ps voltage pulse. It might look difficult to have synchronization among plural signals of such a short duration to realize logic operations. However, this is not the case. Since a fluxon can be held at a particular point of space, such as a branching point during an arbitrary time interval, the fluxon may wait at the point for other fluxons to arrive for the interaction with it. This particlelike character would remove the uncertainty of the binary identity. It also means that a storage circuit or a memory circuit can be easily constructed. The phase-mode circuits possess the advantages that they do not require a maintenance of accurate voltage levels at various interconnections nor a precise coincidence of the pulses for the logical AND operation. So they have advantages in both dc coupled and ac coupled logic circuits. They also have the permanent storage property of fluxons which provides a permanent delay and a bit storage.

We have already reported the experimental and the numerical results on the construction of basic logic circuits, for example AND, OR, and NOT, in our previous papers.[2,10] But the combinations of the AND, OR, and NOT basic circuits are

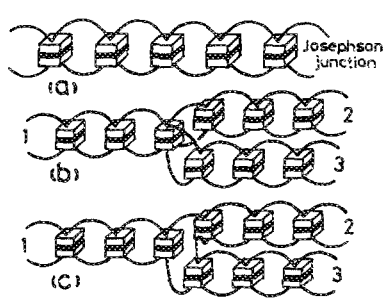


FIG. 1. Discrete Josephson transmission line (a), phase-conserving branch (b), and phase-distributing branch (c).

not always desirable to make a large phase-mode system in terms of the practical circuit construction. It seems that one should take an INHIBIT circuit as the most basic circuit in the phase-mode system for the circuit simplicity. Of course it is clear that all logical functions can be constructed by the combination of INHIBIT circuits, because INHIBIT as well as NAND, NOR, and IMPLICATION are universal operations in terms of Boolean algebra. An INHIBIT circuit shown in Fig. 2 is easily constructed by the combination of a p.c. branch circuit with a p.d. branch circuit.

Figure 2(a) shows an equivalent circuit of the INHIBIT circuit (INHIBIT controlled by fluxon; ICF gate). One input X and two outputs A and B compose a p.d. branch circuit. One output B and two inputs X and Y compose a p.c. branch circuit. A fluxon from input Y stops at the branch point, and it is kept trapped. A fluxon from input X is emitted from output A under the condition of no trapped fluxon from input Y (p.d. branch characteristics "line selection"). When a trapped fluxon from input Y exists, a fluxon from input X is combined with the trapped fluxon, and it is emitted from output B (p.c. branch characteristics "AND"). Therefore the following logic functions are obvious,

$$A = X \cdot \bar{Y}, \quad B = X \cdot Y. \tag{3}$$

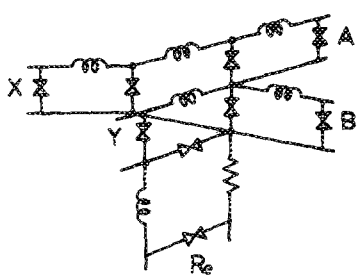
Figure 2(b) shows the truth table of the ICF gate. "Re" in Fig. 2 means a reset terminal to eliminate a trapped fluxon from Y by using an antifluxon and pair annihilation characteristics. When $X = 0$ and $Y = 1$, the trapped fluxon should be eliminated to recover the gate. The operation margin of the ICF gate is calculated by numerical simulations to be about 30% for the bias current used.

III. EXPERIMENTAL RESULTS AND DISCUSSION

There are two methods to detect a fluxon in the experiments. The one method is to use a Josephson sampler.[7] One can obtain a propagating fluxon waveform by using the Josephson sampler. Another method is to use a sense SQUID which is mutually coupled to the end section of JTL. The latter method is convenient for the confirmation of logic operations. We used the Josephson pulse generator for introducing a fluxon into the circuit. The Josephson pulse generator comprises a three-junction SQUID and a single coupling junction. It is coupled to the end of the JTL through a coupling junction and a resistor. By using a Josephson sampler we observed propagating fluxon waveform on a JTL to investigate the input characteristics of the Josephson pulse generator for the JTL. The JTL was fabricated on a Nb ground plane using Pb-alloy planar-junction technology for evaporation, liftoff, and rf plasma oxidation. The minimum linewidth is 4 μm. Figure 3(a) shows the observed waveform of a single fluxon propagating on the JTL without branches for four values of the line bias current. The critical current for the total JTL is 12.9 mA. No fluxon is introduced into the JTL when the bias current is smaller than 7.46 mA. And it can be seen from the figure that the large bias current causes a flux-flow state on the JTL. The waveform agrees with the result of the numerical simulation shown in Fig. 3(b). These detection and input systems have been used in the following experiments.

A. Phase conserving branch

Figure 4 shows a photograph of the p.c. branch circuit. It was fabricated according to the same specification as the above mentioned JTL. To experimentally verify the first behavior ("AND") we have measured the p.c. branch circuit shown in Fig. 4. Each of the three JTL branches has nine junctions whose size is $4.4 \times 4.4\ \mu m^2$. The spacings between the junctions are 60 μm. The total critical current of the circuit is 6.5 mA. Each discrete section of the Josephson line has a 0.61-pH inductance and a 3.0-Ω damping resistance. Each junction is shunted by a 0.6-Ω resistance. The configuration of the JTL is of the overlap type to make the bias



(a)

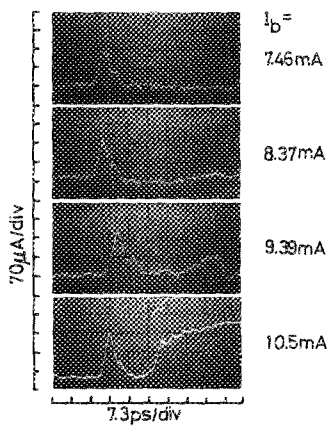
Truth Table

X	Y	A	B
0	0	0	0
0	1	0	0
1	1	0	1
1	0	1	0

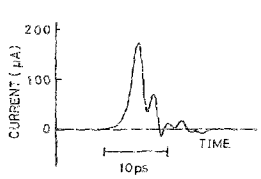
A: INHIBIT
B: AND

(b)

FIG. 2. (a) INHIBIT controlled by fluxons (ICF gate), X and Y are inputs, A and B are outputs, Re is a reset terminal. (b) Truth table of the ICF gate.



(a)



(b)

FIG. 3. (a) Experimentally obtained waveforms of a propagating fluxon on a discrete Josephson transmission line (JTL) for four values of a line bias current; its waveform was measured with a Josephson sampler. (b) Numerical result for the waveform of a fluxon which is propagating on a JTL with a bias current I_b = 8.37 mA. It corresponds to the second experimental result in (a).

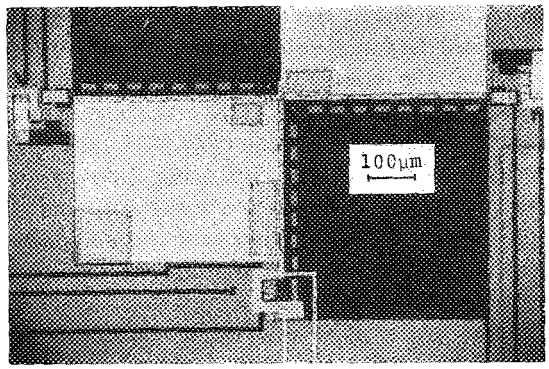


FIG. 4. Photograph of a fabricated p.c. branch circuit.

current flow uniformly. The two branches of the line are used as inputs, and the third branch is used as an output.

Figure 5 shows the experimental results of the functional testing for the p.c. branch circuit. No fluxon is introduced into the JTL from 0- to 2.70-mA line bias currents. The threshold value is mainly dependent upon the property of the input circuit. The first expected behavior ("AND" or "SET and RESET" operation) of the p.c. branch circuit is observed between 2.70- and 3.03-mA bias currents. The second expected behavior ("FAN-OUT" operation) is observed between 3.03 and 3.10-mA bias currents. The input trigger causes a finite steady voltage in the JTL between 3.10- and 6.5-mA bias currents which corresponds to a flux-flow state on the JTL. Figures 5(a) and 5(b) show examples of the experimental data for AND and FAN-OUT operations, respectively, observed by using sense SQUIDs coupled to the JTL.

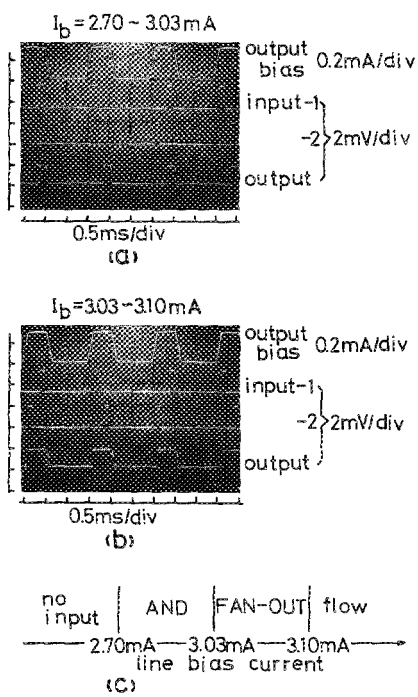


FIG. 5. Experimental results of an "AND" operation for a p.c. branch (a), of a "FAN-OUT" operation (b), and operation margin of the p.c. branch as a function of the bias current (c).

In the photographs the first line shows the bias current of the sense SQUID (fluxon detector) for the output detection, the second and third lines show the voltages of the two input Josephson pulsers (fluxon generators), respectively. A fluxon is introduced into the JTL at the rising voltage edge of the pulse generated by the input Josephson pulser. The fourth line shows the voltage in the fluxon detector; its voltage appears at the timing of the rising edge of the second input pulse in Fig. 5(a). It means that the first input fluxon is held at the branch point until the arrival of the second input fluxon. On the other hand the detector voltage appears at the timing of the first input pulse in Fig. 5(b). It means that the first input fluxon is led to the output immediately without being trapped at the branch point. This result agrees with the numerical prediction[5] that the AND (SET and RESET) operation is performed at the lower bias current compared to the FAN-OUT operation.

B. Phase distributing branch

Figure 6 shows a photograph of the p.d. branch circuit which was fabricated according to the same specification as the p.c. branch circuit. To experimentally confirm the expected behavior we have measured the p.d. branch circuit shown in Fig. 6. The three JTL branches have 10, 11, and 11 junctions, respectively. The size of each junction is 4.4×4.4 μm^2, and the spacing between junctions is 60 μm. Each discrete section of the Josephson line has a 0.65-pH inductance and a 3.1-Ω damping resistance. The measured critical currents of the JTL branches are $I_{c1} = 4.2$ mA, $I_{c2} = 3.8$ mA, and $I_{c3} = 4.8$ mA, respectively. The first JTL branch (line 1) is used as an input, and the other two JTL branches line 2 and line 3 are used as two outputs.

Figure 7 shows the experimental results of the functional testing for the p.d. branch circuit as a function of the line bias currents. In Fig. 7 the horizontal and the vertical axes show the bias currents I_{b2} and I_{b3} for two output lines, respectively. The bias currents I_{b1} for the input line in Fig. 7(a) and for Fig. 7(b) are 2.40 and 3.03 mA, respectively. The circles in Fig. 7 denote a single fluxon propagating to the output line 2 only ("line selection" or "FAN-IN"), and the triangles denote those to the output line 3 only ("line selection" or "FAN-IN"). The solid circles denote the parameter

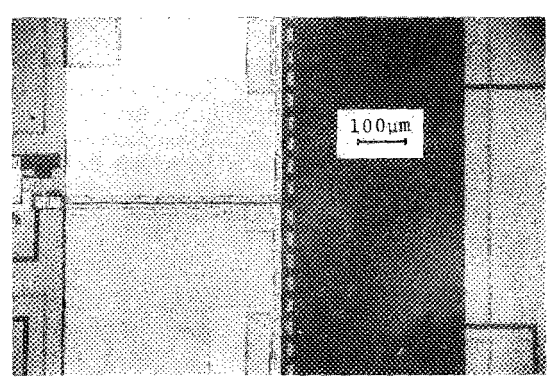


FIG. 6. Photograph of a fabricated p.d. branch circuit.

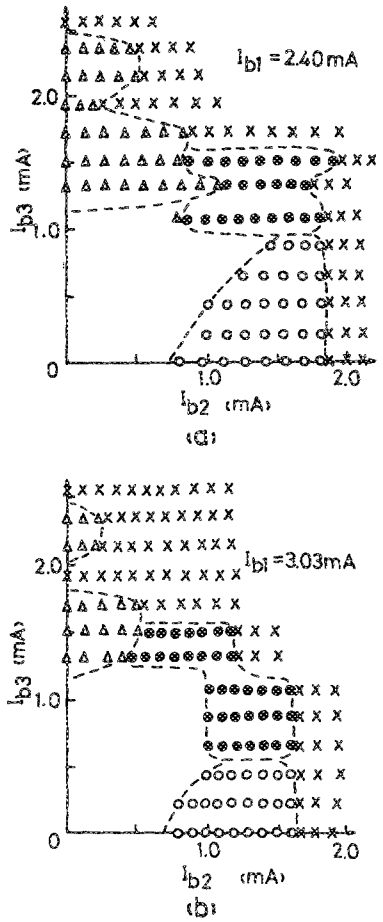


FIG. 7. Experimental results of operation margins of a p.d. branch as a function of two output-line bias currents I_{b2} and I_{b3} for two values of the input-line bias current I_{b1} which are 2.40 and 3.03 mA for (a) and (b), respectively. ×, ⊛, ○, and △ denote a flux-flow state, a fluxon-antifluxon pair creation, an emission of a single fluxon from the output-line 2 only, and that from the output-line 3 only, respectively.

values for which the signal detections are observed in both output lines; fluxon-antifluxon pair creations. The crosses denote the parameters for the occurrence of flux-flow states on the lines.

It can be seen from Fig. 7 that an input fluxon is led only to one of the output line with limited bias current. The operation margin of this action (line selection) is 20%–25% for the line bias current. The threshold value of the bias currents for line selection can be roughly estimated as follows. A fluxon is not introduced into a biased JTL when the phase of the end of the JTL is not over the input threshold phase,

$$\phi_T = \pi - \sin^{-1}\gamma , \tag{4}$$

where $\gamma \equiv I_b / I_c$ $(0 \leqslant \gamma < 1)$ is a normalized bias current. It is an unstable equilibrium point for a biased single pendulum. Since a biased JTL without any input signal should have the stable phase $\sin^{-1}\gamma$, a fluxon arriving at a p.d. branch point should be introduced to line 2 (or 3) when the following inequality is satisfied,

$$\phi_{0i} + \sin^{-1}\gamma_i > \phi_T \quad (i = 2 \text{ or } 3) , \tag{5}$$

where ϕ_{02} and ϕ_{03} are the phases given to line 2 and line 3 by the arriving fluxon, respectively. It is expected that an arrival fluxon supplies each of the two connected lines with the same phase when the bias currents for lines 2 and 3 are equal, because lines 2 and 3 are equivalent. And it may be reasonable that the ratio of ϕ_{02} to ϕ_{03} increases with an increasing bias current ratio of I_{b2} to I_{b3}. Hence we assume,

$$\phi_{02} = (1 + \gamma_2 - \gamma_3)\phi_0/2 , \tag{6}$$

$$\phi_{03} = (1 - \gamma_2 + \gamma_3)\phi_0/2 , \tag{7}$$

where $0 \leqslant \gamma_2 < 1$, $0 \leqslant \gamma_3 < 1$, and ϕ_0, the phase of the input line, would normally depend on the velocity $u(\gamma_1)$ of an arriving fluxon. One can obtain from Eqs. (5) and (6) the condition to introduce an arriving fluxon into line 2 (line selection),

$$\gamma_3 < 1 - 2\pi/\phi_0(\gamma_1) + [4/\phi_0(\gamma_1)]\sin^{-1}\gamma_2 + \gamma_2 . \tag{8}$$

It can be seen by comparing Figs. 7(a) and 7(b) that the increase of I_{b1} (γ_1) does not effect the threshold values of line selection. Therefore, it suggests that the velocity of the fluxon propagating on line 1 is already saturated for I_{b1} = 2.4–3.03 mA. This possibility is also expected from the numerical calculation.[11] Hence it may be deduced that ϕ_0 is independent of γ_1 in this experimental condition, and that ϕ_0 has the same constant value in Figs. 7(a) and 7(b).

Pair creation occurs in the higher bias region where the bias currents of the two output lines are roughly equal. It can be seen from Fig. 7 that the increase of I_{b1} pulls down the threshold values for pair creations for I_{b2} and I_{b3}. If one assumes that a pair creation occurs when the conditions obtained from Eqs. (5), (6), and (7) are satisfied both in lines 2 and 3, the difference between the threshold values of pair creations in Figs. 7(a) and 7(b) cannot be explained, because ϕ_0 seems to have the same constant value in Figs. 7(a) and 7(b). The reflection occurring at the end of line 1 is considered to play a crucial role in causing a pair creation. A fluxon reflects as an antifluxon at an open end of a biased JTL.[5] In the case shown in Fig. 7, a reflection as an antifluxon at the end of line 1 causes a pair creation to satisfy the quantum condition. The reflection condition, whether a reflected wave grows into an antifluxon or not, depends on values of a bias current. The threshold value of the bias current may be determined with Eq. (5) where $i = 1$ and ϕ_{01} is a phase increment given by a reflected wave. When an arriving fluxon chooses line 2 as the propagating direction, ϕ_{02} in Eq. (6) is carried away by the fluxon, but ϕ_{03} in Eq. (7) is not. Hence if we use ϕ_{03} as a reflected phase ϕ_{01}, we can obtain Eq. (9) from Eqs. (5) and (7),

$$\gamma_3 > 2\pi/\phi_0 - 1 + \gamma_2 - (4/\phi_0)\sin^{-1}\gamma_1 . \tag{9}$$

Equation (9) shows a threshold of pair creations and the decrease of threshold of I_{b3} with increasing I_{b1}.

The flux-flow state occurs in the highest bias region in Fig. 7. It is considered that an input fluxon stops at the branch point in the lower bias region which is the blank area in the vicinity of the origin of Fig. 7.

Figure 8 shows the numerical results of the functional testing for the phase distributing branch circuit as a function of the normalized line bias currents. It can be seen from the figures that the increase of I_{b1} largely pull down the thresholds of the pair creation for I_{b2} and I_{b3}, but that it does not largely pull down the thresholds of the single fluxon propagation to the output lines. The numerical results agree qualitatively with the experimental results.

In Fig. 7(b) the single fluxon propagation region denoted by triangles which is located at higher bias current for line 3, and which is isolated by the flux-flow region seems to appear by the interference of the three bias currents I_{b1}, I_{b2},

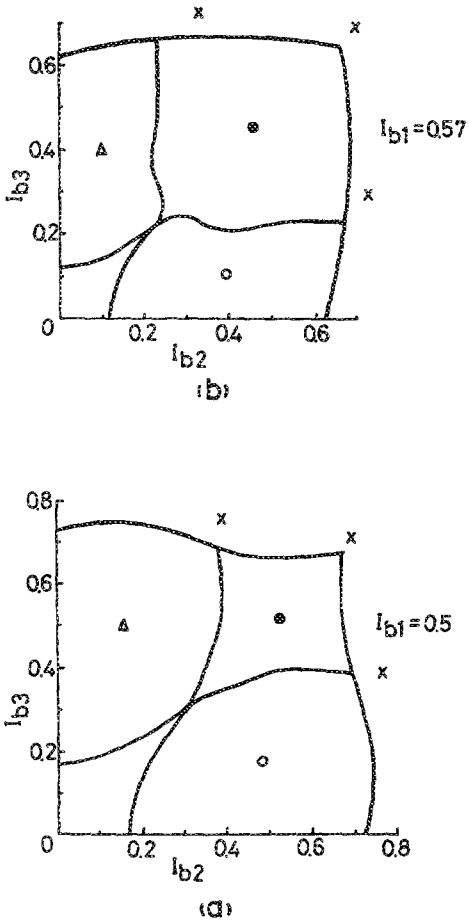


FIG. 8. Numerical results of operation margins of a p.d. branch as a function of two output-line normalized bias currents γ_2 and γ_3 for two values of the input-line normalized bias curent γ_1 which are 0.5 and 0.57 for (a) and (b), respectively. ×, ●, ○, and △ denote the same operations of the p.d. branch as indicated in Fig. 7, respectively.

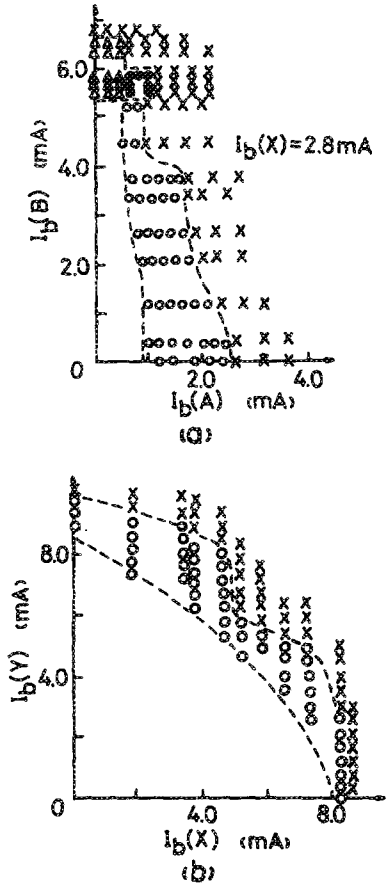


FIG. 9. Experimental results of operation margins of a ICF gate. The ICF gate was operated as a p.d. branch in (a) where the branches *X*, *A*, and *B* indicated in Fig. 2 were used, and it was also operated as a p.c. branch in (b) where the branches *X*, *Y*, and *B* were used. The horizontal and the vertical axes show the bias currents of two output branches *A* and *B* in (a), and of two input branches *X* and *Y* in (b), respectively. ×, ●, ○, and △ (a) denote the same operations of the p.d. branch as indicated in Fig. 7, respectively. × and ○ in (b) denote a flux-flow state and a "FAN-OUT" operation, respectively.

and I_{b3}, because it is expected that the occurrence of the flux-flow voltage changes the flow path of the bias currents. The difference between the experimental and the numerical results seems to be mainly caused by the interference and the nonuniformity of the bias currents, because the bias currents of our numerical calculation are held constant with respect to time, and uniform along each of line branches.

C. ICF gate

Figures 9(a) and 9(b) show the experimental results of the ICF gate. The measured circuit does not have a "Re" terminal, and it is composed of 41 $4\times4\ \mu m^2$ junctions. The line branches for the input *X*, for the input *Y*, for the output *A*, and for the output *B* have 10, 10, 11, and 10 junctions, respectively. The loop inductance of each section is 0.63 pH, and each loop inductance has a damping resistance of 3.4 Ω. In Fig. 9(a) a single fluxon is given to the *X* input only. The horizontal and vertical axes show the bias current $I_b(A)$ for the line of the output *A* and the bias current $I_b(B)$ for the line of the output *B*, respectively. The bias current $I_b(X)$ for the line of the input *X* is 2.8 mA. The circles denote that the input fluxon is emitted from the output A only. The triangles denote that the input fluxon is emitted from the output B only. The solid circles denote the pair creations. The crosses denote the occurrence of the flux-flow states. It can be seen by comparison with Fig. 6 that the propagating region is asymmetrically divided in Fig. 9(a) which is expected from the composition of the ICF gate. In Fig. 9(b) a single fluxon is given to the input Y only. The horizontal axis shows the bias current $I_b(X)$. The vertical axis shows the bias current $I_b(Y)$ for the line of the input Y, which is automatically applied to the line of the output B. The circles denote the FAN-OUT operation. The crosses denote the occurrence of the flux-flow states. Therefore the normal operation region for the bias current of the ICF gate is expected as following, 1.0 mA $< I_b(A) <$ 2.5 mA and $I_b(Y$ or B$) <$ 5.5 mA at $I_b(X) = 2.8$ mA.

IV. CONCLUSION

We have experimentally investigated the phase-mode Josephson digital circuits. The discrete Josephson transmission line (JTL), the phase-conserving (p.c.) branch of the JTL, and the phase-distributing (p.d.) branch of the JTL are

basic elements for the phase-mode digital circuits. The experimental results obtained by using Josephson samplers, sense SQUIDs, and fluxon generators have confirmed the AND (SET and RESET) operation and the FAN-OUT operation of the p.c. branch, and have also confirmed the FAN-IN, the line selection, and the pair-creation operations of the p.d. branch. And we have experimentally obtained the bias current dependence of these operations. Finally we have proposed the ICF (INHIBIT controlled by a fluxon) gate which is a combination of the p.c. and p.d. branch, and which is a basic gate to construct a phase-mode information processor. We have obtained the experimental results to show that the ICF gate has the phase-conserving and phase-distributing branch characteristics. These experimental results indicate the basic possibility for a information processor composed of phase-mode Josephson digital circuits which may be a prototype of future quantum computer systems where physical quantum states are employed as logic states of information processing.

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