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Multilevel Metallization Based on Al CVD

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1. Introduction

Our final goal is planarized multilevel metallization based on Al CVD including the device level metallization in the 0.1μm era as shown in Fig. 1. The advantages of Al- alloy based multilevel metallization over the conventional CVD-W via plug process and the novel Cu metallization are (1) lower resistivity of Al than CVD- W via, (2) stability of Al-alloy comparing with Cu, *i.e.*, diffusion barrier against interlayer dielectrics is not necessary in Al-based metallization.

We have developed Al CVD technology using DMAH $[(CH_3)_2AlH]$[1-3]; (1) selective deposition onto electrically conductive surfaces such as Si, Ti, and TiN, and (2) proposal and experimental verification of surface electrochemical reaction model for Al deposition. Several attempts on Al-CVD via-plug process have been reported.[4,5] However, few reports on Al deposition on TiN layer, which is usually exposed to air environment in the practical metallization process, have been reported. The surface pretreatment of TiN prior to Al deposition is a key issue for practical application.

In this paper, we report the plasmaless ClF_3 pretreatment prior to the Al CVD, Al deposition on TiN layer and a new MOSFET structure as device level metallization for the Al-CVD based multilevel metallization.

2. Plasmaless ClF_3 pretreatment

Surface morphology of CVD- Al on TiN has been so far insufficient for practical application. This is considered to be because native oxide of TiN surface prevents the smooth nucleation of Al at the initial growth stage. The plasmaless ClF_3 pretreatment is employed prior to Al deposition. In this work, TiN surface is typically etched 100Å in thickness at 80°C during the ClF_3 pretreatment, then Al is deposited using DMAH.

Figure 2 shows an etching rate of TiN by ClF_3. ESCA measurement has revealed that F atom remains on the ClF_3-pretreated TiN, where F atom combines with Ti not with N.[6] SIMS depth profile of CVD- Al/TiN interface shows that Cl concentration is less than 10^{19} atoms/cm^3, resulting in that corrosion has not been observed in the post deposited Al.

Figure 3 shows resistivity of Al on TiN. Aluminum films deposited below 220°C exhibits the reflectivity of over 225%@300-600nm, when the reflectivity of Si is 100%. The resistivity of 500Å- thick Al film is 3.0$\mu\Omega$cm which is close to the bulk resistivity of 2.7$\mu\Omega$cm. The slight increase in the resistivity above 240°C is mainly due to surface roughness.

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3. Aluminum deposition on TiN for multilevel metallization

[Conformal deposition, Fig. 4] Figure 4 shows SEM images of 0.5μmϕ/1.2μm- deep holes which is covered with the smooth 1000Å- thick blanket Al deposited at 180°C. The Al thicknesses on the top surface, on the side wall and on the bottom are the same, *i.e.*, 100% step coverage is achieved. This feature shows that the blanket Al can be used as a thin reflow- enhancement layer of Al- sputtering reflow process in the upper layer interconnect.

[Via filling (blanket mode), Fig. 5] Longer deposition duration of Al has resulted in the complete filling as shown in Fig. 5. Via filling and the subsequent Al- Cu sputter deposition is applicable to 1st and/or 2nd high-reliable via filling of Fig. 5(b), since Cu can be diffused into CVD-Al [5].

[Contact/via filling (selective mode), Fig. 6] For the most severe diam. contact holes, the selective deposition is promising as shown in Fig. 6.[2,3]

[Fully self- aligned metallization MOSFET, Fig. 7] As a device level application of Al CVD, we propose a new device structure of Fig. 7. The feature is to reduce the parasitic resistances for high speed MOSFET; (1) low contact resistance using $TiSi_2$ SALICIDE, (2) TiN barrier layer which is formed by self- aligned rapid thermal nitridation (RTN), and (3) selectively deposited Al on TiN for reducing the sheet resistances. Figure 7(b) shows the selective Al deposition on gate and source/drain regions after the ClF_3 pretreatment. The measured sheet resistance of 500Å- thick Al on TiN is 0.6Ω/□, which is about ten times lower than that of the conventional SALICIDE structure. The fully self- aligned metallization structure is promising for high speed MOSFET, especially for MOSFET with large gate width.

4. Summary

We have developed Al CVD on TiN with the plasmaless ClF_3 pretreatment. It has been demonstrated that the Al-CVD based multilevel metallization including the device structure is promising for the 0.1μm-era's metallization.

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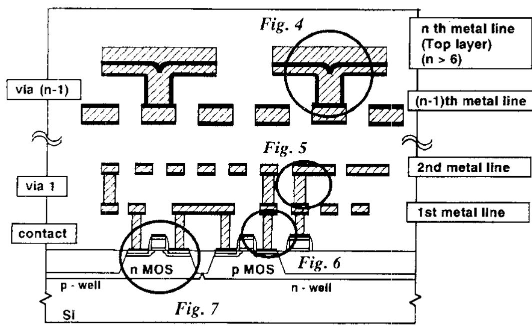


Number of interconnect layers (Logic circuits) > 6
Contact hole diameter < 0.18 μm

Requirements

(1) **Device level:** Reduction of parasitic resistances.
(2) **Contact/via holes:** Filling metal, Avoiding the different metal contact such as Al/W and Cu/W.
(3) **Metal line:** High EM/SM endurance, Grain control.
(4) **Interlayer dielectrics:** Low k material, Low thermal budget.
(5) **Planarization:** CMP

Fig. 1 Planarized CVD-Al based multilevel metallization in 0.1μm-era.

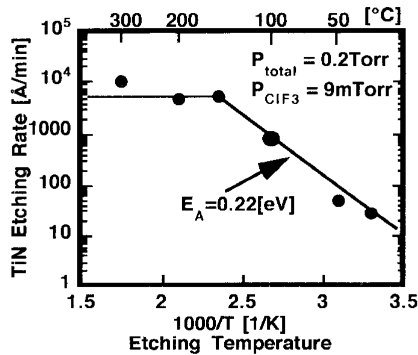


Fig. 2 TiN etching rate using ClF_3.

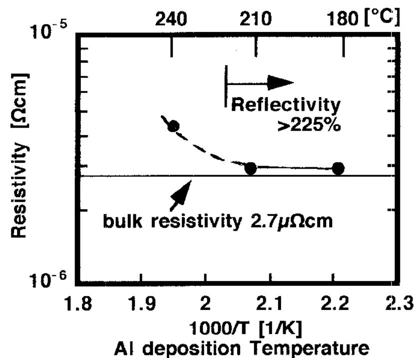


Fig. 3 Al resistivity as a function of deposition temperature. (P_{Total} = 1 Torr, P_{DMAH} = 12 mTorr)

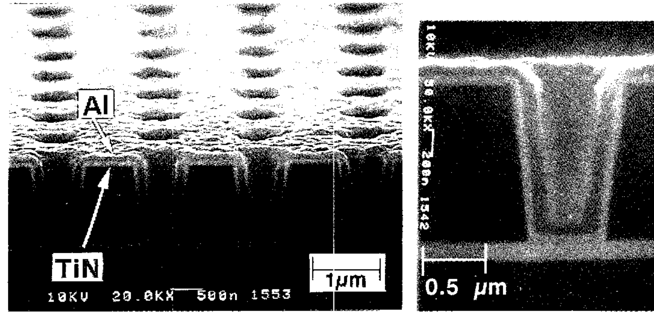
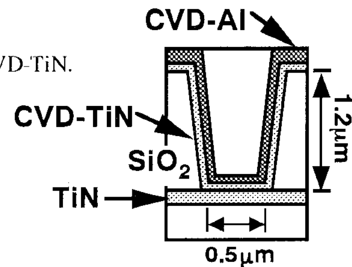


Fig. 4
Conformal Al deposition on CVD-TiN.



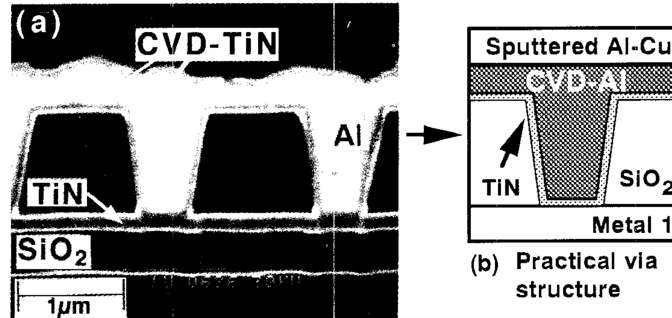


Fig. 5 Via-filling by the blanket Al.

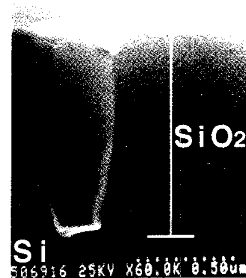
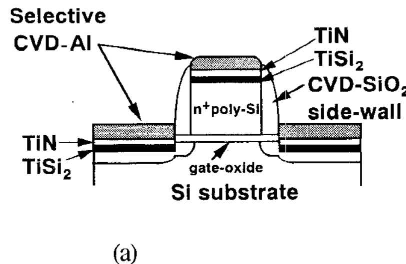
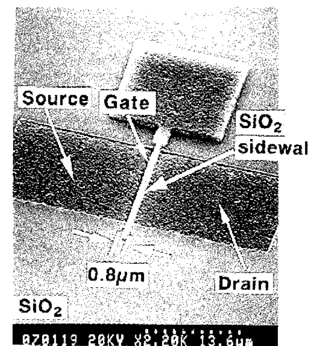


Fig. 6
Contact/via-filling by the selective Al.



(a)



(b) SEM image. Al is seletively depositied on gate and source/drain regions. The sheet resistance is dramatically reduced to be 0.6Ω/□ with Al thickness of 500Å.

Fig. 7 Fully self-aligned metallization MOSFET.

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