## 12.7 Ferroelectric-Based Functional Pass-Gate for Fine-Grain Pipelined VLSI Computation

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A fine-grain pipelined architecture that distributes pipeline registers over a logic-circuit plane like a 'logic-in-memory' structure [1] has been demonstrated to be suitable for the realization of fine-grain pipelined VLSI processors such as high-throughput FIFOs [2]. A functional pass-gate structure, in which pipeline latches are merged into switching gates by using ferroelectric devices, realizes a compact fine-grain pipelined VLSI system. Heretofore, ferroelectric capacitors have been conventionally used as simple nonvolatile storage elements [3]. Here the write operations of a ferroelectric capacitor are considered as universal switching operations under the control of two variables, so that both storage and switching functions can be performed simultaneously in a single ferroelectric capacitor.

Figure 12.7.1 shows the functional pass-gate using ferroelectric devices. The symbols $M_{w1}$, $M_{w2}$, $M_{RD}$ and $M_{RS}$ represent conventional nMOS transistors that control the voltages at two terminals of the ferroelectric capacitor $C_S$. $C_P$ is a dummy ferroelectric capacitor that converts the remnant-polarization state of $C_S$ into a corresponding voltage level by a capacitive coupling effect. The nMOS transistor $M_P$ is a pass-gate used for the series and parallel connections of the functional pass-gates, thereby realizing any complicated logic circuit.

Figure 12.7.2 shows the basic behavior of the functional pass-gate, in which operation proceeds in four phases: 'reset phase', 'operation/write phase (O/W phase)', 'retention phase' and 'read phase'. In the reset phase, the clock signal $\overline{CLK}$ and the reset signal RS are set to high, then stored data S which corresponds to the remnant-polarization state is set to 0. In the operation/write phase, the inverse of clock signal is high, then the external inputs y1 and y2 appear at the terminals of $C_S$ through the transistors, $M_{w2}$ and $M_{w1}$, respectively. When $(y_1,y_2)=(1,0)$, the remnant-polarization state corresponding to S changes to 1. Otherwise, S remains 0. In this way, an AND operation with two variables, $y_1$ and $y_2$, is performed and the result is stored into $C_S$ as the remnant-polarization states, simultaneously. If the remnant-polarization state is initially set to 1, the OR operation can be performed in the above operation/write phase. In the retention phase, gate voltage of the nMOS transistor $M_{RS}$ is pulsed high, and voltage levels on two bit-lines, BY1 and BY2, fall to GND level, then $C_S$ is discharged. In the read phase, $R_S$ falls to low and CLK is set to high, then the high voltage level is supplied to $C_S$ through the transistor $M_{RD}$. According to the remnant-polarization state, a voltage $V_A$ on node A is generated by capacitive coupling between $C_S$ and $C_P$. When S=0, $V_A$ is lower than the threshold voltage $V_{th}$ of the pass-gate $M_P$, and $V_A$ is larger than $V_{th}$ when S=1. Therefore, the remnant-polarization state on $C_S$ is read out as a switching state of $M_P$. Figure 12.7.2 also shows a timing diagram of the four phases.

Figure 12.7.3 illustrates the implementation of a serial adder using the functional pass-gate network. In the equivalent CMOS realization for a latch-based serial adder, seven latches are required as well as switching gates. Using the functional pass-gates, the serial adder can be designed compactly with a precharge-evaluate logic style. Figure 12.7.3 also shows the timing diagram in which the basic behavior of the proposed ferroelectric-based serial adder is demonstrated. When both CLK and RS inputs become high, Block1 performs the read operation, and outputs of Block1 are stored into functional pass-gates of Block2. When Block1 is in the reset scheme, match lines, ML11 and ML12, are precharged and outputs of Block1 becomes to 0. At the same time, Block2 is in the retention scheme, and $C_S$ in the functional pass-gate of Block2 is discharged.

Figure 12.7.4 shows the micrograph of a ferroelectric-based circuit chip in a 0.6μm ferroelectric/CMOS process technology. The ferroelectric-based functional pass-gate is 9.4x10.5μm², and ferroelectric capacitors, $C_S$ and $C_P$, are fabricated by using $Pb(Zr,Ti)O_3$ with 20μC/cm² remnant polarization where the $C_P/C_S$ ratio is 2. The ferroelectric-based switching operation and the read operation result in a compact circuit realization using ferroelectric capacitors. Figure 12.7.5 shows measured waveforms. According to the synchronization of the reset signal RS, four different external input states of $(y_1, y_2)$ are demonstrated. It is observed that the AND operation $y_1, \overline{y_2}$ is correctly performed. Capacitive coupling effect between two ferroelectric capacitors $C_S$ and $C_P$ makes it possible to perform high-speed switching while maintaining compact circuit realization.

A typical potential application of fine-grain pipelined VLSI computation is illustrated in Figure 12.7.6 It shows a 250MHz 54x54b pipelined multiplier which has 16 pipeline stages. The pipeline pitch is determined by the delay of a single functional pass gate.

Figure 12.7.7 provides a comparison of two pipelined multipliers: conventional static CMOS realization and the proposed one. The effective chip area is greatly reduced in the proposed pipelined system by using functional pass-gate network, because the switching gate and pipelined latch are merged in the functional pass-gate network. The advantage of compact circuits also reduces the power dissipation of the proposed functional pass-gate network, in the comparison with a corresponding CMOS implementation. Consequently, effective chip area and power dissipation of the functional pass-gate network are 30% and 49%, of the corresponding CMOS implementation, respectively.

*Acknowledgments:*

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*References:*

[1] T. Hanyu, et al., "Multiple-Valued Logic-in-Memory VLSI Based on Floating-Gate-MOS Pass-Transistor Network," Digest of Technical Papers, pp. 194-195, Feb. 1998.
[2] J.Ebergen, "Squaring the FIFO in GasP," Proc. IEEE 7th Int. Symp. on Asynchronous Circuits and Systems, pp. 194-205, March 2001.
[3] A. Sheikholeslami, P. G. Gulak, "A Survey of Circuit Innovations in Ferroelectric Random-Access Memories," Proceedings of the IEEE, vol. 88, no. 5, pp. 667-689, May 2000.

 

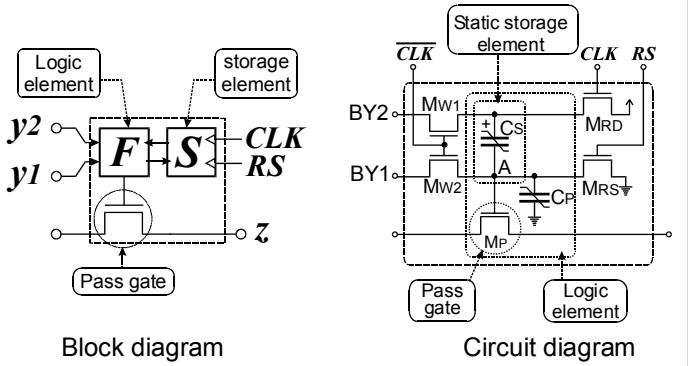


Figure 12.7.1: Design of a ferroelectric-based functional pass-gate.

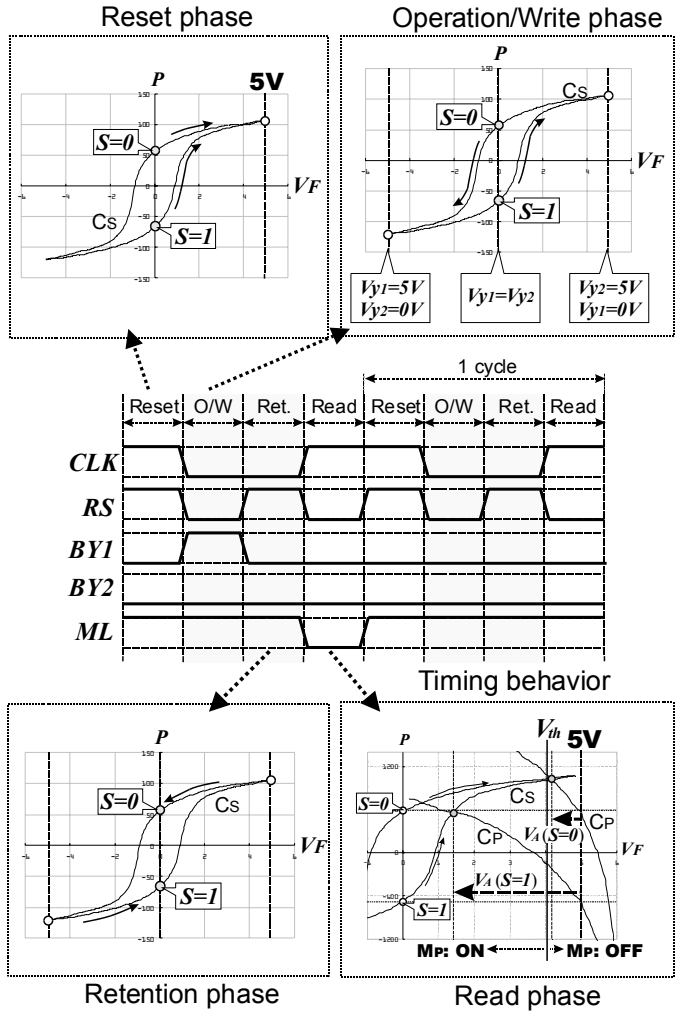


Figure 12.7.2: Basic behavior.

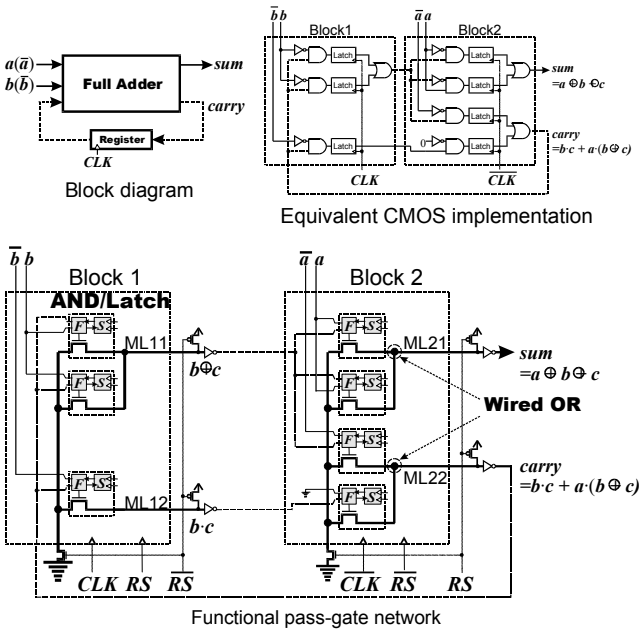


Figure 12.7.3: Design example.

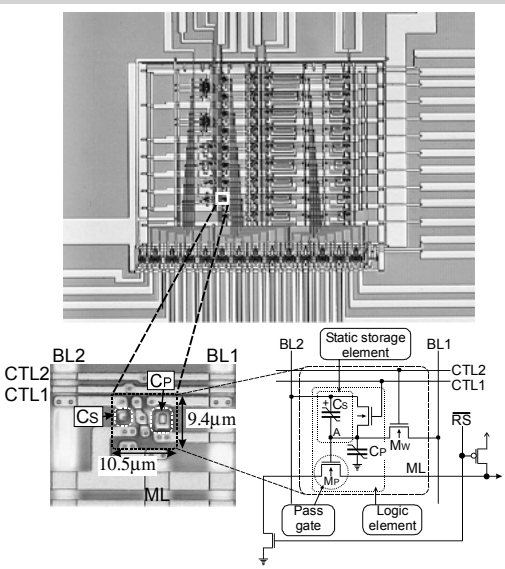


Figure 12.7.4: Test chip micrograph.

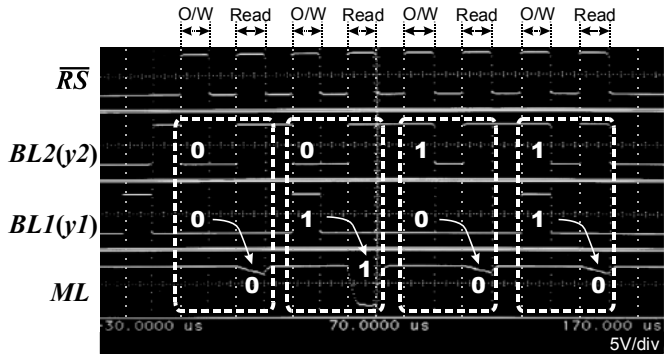


Figure 12.7.5: Measured waveforms of the test chip.

Power supply voltage: 4.0V

| | Static CMOS | Proposed |
|---|---|---|
| No. of pipeline stage | 16 | 16 |
| Delay / stage | 1.3ns | 1.8ns |
| Power dissipation | 5.07W | 2.50W |
| Area | 25.6mm$^2$ | 7.82mm$^2$ |

HSPICE simulation based on a 0.6μm ferroelectric/CMOS technology

Figure 12.7.7: Comparison of pipelined multipliers.

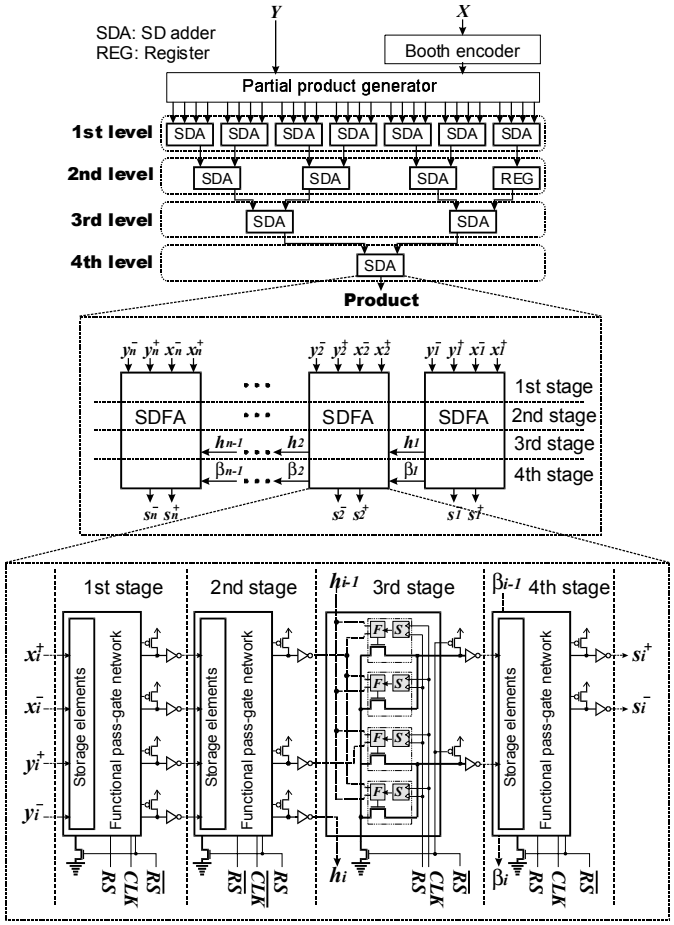


Figure 12.7.6: Overall structure of a pipelined 54x54b multiplier.