Challenge of a Multiple-Valued Technology in Recent Deep-Submicron VLSI

Takahiro Hanyu
Department of Computer and Mathematical Sciences,
Graduate School of Information Sciences, Tohoku University
Aoba-yama 05, Sendai 980-8579, Japan
Phone : +81-22-217-7153
Fax : +81-22-263-9401
E-mail : hanyu@kameyama.ecei.tohoku.ac.jp

Abstract

A logic-in-memory VLSI architecture based on multiple-valued floating-gate MOS pass-transistor logic is proposed to solve a communication bottleneck between modules in the recent deep-submicron VLSI. Moreover, a multiple-valued current-mode circuit based on dual-rail differential logic is also proposed as a candidate suitabe for self-checking and asynchronous VLSI systems. Finally, the advantage of the above multiple-valued circuit technologies is shown by using design examples.

1. Introduction

Communication bottleneck between memory and logic modules is one of the most serious problems in recent deep submicron VLSI systems, especially in the multimedia VLSI systems on a single chip [1],[2]. A logic-in-memory structure, in which storage functions are distributed over a logic-circuit plane, is a key technology to solve the above problem [3],[4]. However, the logic-in-memory VLSI architecture may be generally more complex to build than a normal one where a logic-circuit plane is separated from a memory module, because of the overhead involved in the storage and logic elements.

Moreover, an asynchronous-control technique and a fault-tolerance technique as well as high-performance system architectures and circuit design techniques, have become increasingly important in recent deep submicron VLSI chips. The self-checking circuit, that is an important fault-tolerance technique, has the capability to test for the occurrence of transient and permanent faults within the circuit by a normal input, as well as to detect errors at the input itself [5],[6]. And, the asynchronous-control circuit technique is a key to solve a clock-distribution problem due to interconnection complexity in the recent deep-submicron VLSI chips. However, the use of the present binary CMOS gates requires large number of transistors for realizing self-checking and asynchronous-control circuits [7]-[9].

This paper presents some multiple-valued (MV) circuit technologies to realize a high-performance or a highly reliable VLSI processor in the recent deep-submicron chip. First, a logic-in-memory VLSI using floating-gate-MOS pass-transistor logic [10]–[12] is proposed to merge storage and switching functions in a multiple-valued-input and binary-output combinational logic circuit. Multiple-valued stored data are represented by the threshold voltage of a floating-gate MOS transistor [13], so that both multiple-valued threshold-literal and pass-switch functions [14],[15] can be merged by using a single floating-gate MOS transistor.

In addition, a new multiple-valued current-mode (MVCM) circuit based on dual-rail differential logic is proposed to realize both a totally self-checking circuit [16] and an asynchronous-control circuit [17] with keeping a high-driving capability at a low supply voltage.

0-7695-1083-3/01 $10.00 © 2001 IEEE

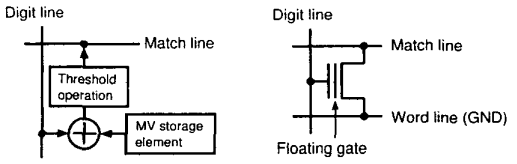

Figure 1: Multiple-valued CAM cell structure.

2. MV circuit technology for logic-in-memory VLSI architecture

Nonvolatile devices such as floating-gate MOS transistors and ferroelectric devices are generally used as memory cell devices [18]-[19]. Since a nonvolatile device can be utilized not only as a memory element but also as a switching one, a circuit design using nonvolatile devices has a potential advantage to realize a high-performance VLSI system with less communication bottleneck between storage and logic elements [20]-[22].

As a typical example, Figure 1 shows a multiple-valued CAM cell circuit where a multiple-valued threshold function and a pass-switch function are merged into a multiple-valued storage element by a single floating-gate MOS transistor. Using the principle of the above circuit structure, Figure 2 shows a layout of a highly parallel collision-detection VLSI processor for intelligent vehicles under a 0.8-μm CMOS technology. It includes two kinds of components: a multiple-valued CAM and eight processing elements (PEs) for high-speed coordinate transformations. Frequent communication between the PEs and the CAM is required for collision detection, so that they must be integrated on a single chip.

3. MV circuit technology for self checking and asynchronous control

It has been known that data representation based on dual-rail coding is useful as a code word in self-checking and asynchronous-control circuits. Since an MVCM circuit based on dual-rail differential logic has a potential advantage to realize a high-speed logic circuit at a low supply voltage, the MVCM circuit

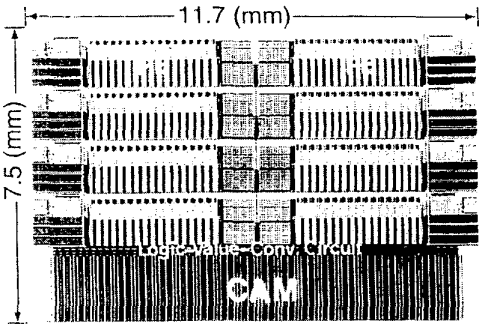

Figure 2: Layout of a collision-detection VLSI processor with a 4-valued CAM.

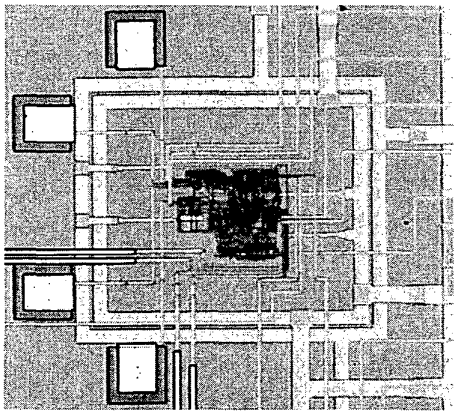

Figure 3: Totally self-checking circuit based on dual-rail MVCM differntial logic.

technology is compatible with the realization of self-checking and asynchronous-control circuits.

Figure 3 shows a chip photomicrogragh of a totally self-checking MVCM circuit. A non-self-checking (NSC) differential-pair circuit (DPC) is proposed and has a redundant function because one of the dual-rail outputs depends on only a single input in the NSC DPC. Accordingly, a self-checking DPC can be designed by the duplication of the proposed NSC DPC. As a result, a self-checking MVCM circuit can be easily designed by using the proposed NSC DPCs in replacement of the original NSC DPC, while other basic components such as comparators and wired-sum circuits still remain used to realize the self-checking circuit.

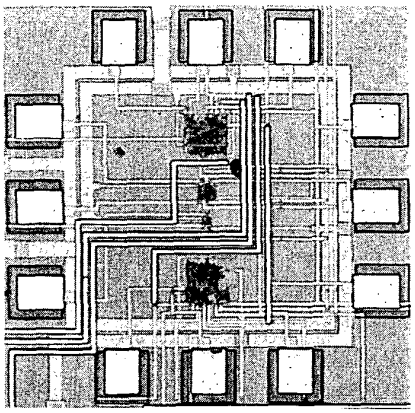

Figure 4: Asynchronous-control circuit based on dual-rail MVCM differntial logic.

Figure 4 show a chip photomicrograph of an MVCM circuit for asynchronous-control VLSI system. In the proposed two-color asynchronous communication, a four-valued data value is represented by a pair of seven-valued dual-rail complementary digits. In odd and even phases, the sums of dual-rail digit pairs becomes '3' and '9', respectively. Therefore, the use of this dual-rail coding makes it easy to detect three different states such as an odd-phase data-arrival state, an even-phase data-arrival state and a data-transition state in the two-color asynchronous communication. Moreover, the two-color dual-rail four-valued coding can be easily extended to any multiple-valued data representation. In the viewpoint of compact asynchronous circuit realization, the MVCM circuit technique is suitable because the signal-state detection for asynchronous data transfer is performed by using the sum of dual-rail digit pairs and its threshold operation whose basic operations are compactly realized by using the dual-rail MVCM circuit techniques.

4. Conclusion

Some multiple-valued circuit technologies have been introduced and their usefulness and easiness for chip fabrication are shown by using concrete examples. As a future prospect of the proposed multiple-valued circuit technologies, it is also important to combine voltage-mode circuit technologies into current-mode

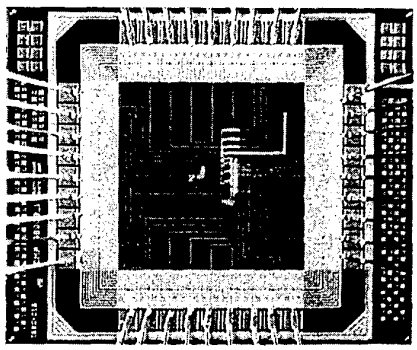

Figure 5: MV hybrid-mode circuit for 4-valued full addition with a 4-valued storage element.

ones, called a "hybrid-mode" circuit technology [23]. A multiple-valued current-mode logic circuit is suited to implement arithmetic VLSI systems. For example, Figure 5 shows a hybrid-mode multiple-valued circuit for the use of the hybrid-mode circuit technology will have a possibility to enhance the performance of muletiple-valued VLSI systems more and more in the recent deep-submicron era.

Acknowledgment

The author wishes to thank Michitaka Kameyama of Tohoku University for many helpful comments.

References

[1] J. Borel, "Technologies for Multimedia Systems on a Chip," Digest of Technical Papers, IEEE International Solid-State Circuits Conference, TA1.1, pp.18-21, Feb., 1997.

[2] H. Veendrick, "Deep-Submicron CMOS ICs," Kluwer BedrijfsInformatie, 1998.

[3] W. H. Kautz, "Cellular Logic-in-Memory Arrays," IEEE Trans. on Computer, Vol.C-18, No.8, pp.719–727, Aug., 1969.

[4] D. G. Elliott et al., "Computational RAM: Implemeting Processors in Memory," IEEE Design & Test of Computers, pp.32–41, Jan.–March, 1999.

[5] D. A. Anderson and G. Metze, "Design of totally self-checking check circuits for m-out-of-n codes," *IEEE Trans. Computers*, vol.C-22, no.3, pp.263–269, Mar. 1973.

[6] J. F. Wakerly, *Error Detecting Codes: Self-Checking Circuits and Applications*, Elsevier North-Holland, New York, 1978.

[7] A. K. Goel, *High-Speed VLSI Interconnections*, Wiley Interscience, 1994.

[8] G. Birtwistle and A. Davis, *Asynchronous Digital Circuit Design*, Springer, 1995.

[9] M. Afghahi and C. Svensson, "Performance of synchronous and asynchronous scheme for VLSI systems," *IEEE Trans. Computers*, vol.41, No.7, pp.858–872, July 1992.

[10] T. Hanyu, N. Kanagawa and M. Kameyama, "Design of a One-Transistor-Cell Multiple-Valued CAM," IEEE Journal of Solid-State Circuits, Vol. SC-31, No. 11, pp.1669–1674, Nov. 1996.

[11] T. Hanyu, K. Teranishi and M. Kameyama, "Multiple-Valued logic-in-Memory VLSI Based on a Floating-gate-MOS Pass-Transistor Network" IEEE International Solid-State Circuits Conference, FP12.5, pp. 194–195, Feb. 1998.

[12] T. Hanyu and M. Kameyama, "Multiple-Valued Logic-in-Memory VLSI Architecture Based on Floating-Gate-MOS Pass-Transistor Logic" IEICE Trans. Electronics, Vol.E82–C, No.9, pp. 1662–1668, Sep. 1999.

[13] T. Higuchi and M. Kameyama, "Multiple-Valued Digital Processing System," Shokodo Co. Ltd., Tokyo, 1989 (in Japanese).

[14] D. Radhakrishnan, S. R. Whitaker and G. K. Maki, "Formal Design Procedures for Pass Transistor Switching Circuits" IEEE Journal of Solid-State Circuits, Vol.SC-20, No.2, pp.531–536, April 1985.

[15] A. Parameswar, H. Hara and T. Sakurai, "A High Speed, Low Power, Swing Restored Pass-Transistor Logic Based Multiply and Accumulate Circuit for Multimedia Applications," IEEE 1994 Custom Integrated Circuits Conf., pp.278–281, May 1994.

[16] T. Hanyu, T. Ike and M. Kameyama, "Self-Checking Multiple-Valued Circuit Based on Dual-Rail Current-Mode Differential Logic," IEEE International Symposium on Multiple-Valued Logic, pp.275–279, May 1999.

[17] T. Hanyu, T. Ike and M. Kameyama, "Integration of Asynchronous and Self-Checking Multiple-Valued Circuits Based on Dual-Rail Differential Logic," IEEE 2000 Pacific Rim International Symposium on Dependable Computing, pp.27–33, Dec. 2000.

[18] C. Hu, "Nonvolatile Semiconductor Memories Technologies, Design and Applications" IEEE PRESS, 1991.

[19] W. D. Brown and J. E. Brewer, "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide to Understanding and Using NVSM Devices" IEEE PRESS, 1997.

[20] T. Miwa, "A 1Mb 2-Transistor/bit Non-Volatile CAM Based on Flash-Memory Technologies," Digest of Technical Papers, IEEE International Solid-State Circuits Conference, TP2.5, pp.40–41, Feb., 1996.

[21] A. Sheikholeslami, P. G. Gulak and T. Hanyu, "A Multiple-Valued Ferroelectric Content-Addressable Memory," IEEE International Symposium on Multiple-Valued Logic, pp.74–79, May 1996.

[22] T. Hanyu, H. Kimura and M. Kameyama, "Multiple-Valued Content-Addressable Memory Using Metal-Ferroelectric-Semiconductor FETs," IEEE International Symposium on Multiple-Valued Logic, pp.30–35, May 1999.

[23] T. Hanyu, S. Kaeriyama and M. Kameyama, "Arithmetic-Oriented Multiple-Valued Logic-in-Memory VLSI Based on Current-Mode Logic" IEEE International Symposium on Multiple-Valued Logic, pp. 438–443, May 2000.