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Efficient ZnO–SiO$_2$–Si Sezawa Wave Convolver

SHOICHI MINAGAWA, TAKESHI OKAMOTO, TERUO NIITSUMA, KAZUO TSUBOUCHI,
AND NOBUO MIKOSHIBA

Abstract—**A detailed design theory of the Sezawa wave convolver is developed, and the fabrication of a high-efficiency convolver using a ZnO-SiO$_2$-Si structure is discussed. The important points to improve the efficiency are 1) an optimum choice of SAW propagation direction on the Si substrate, 2) an optimum design of the resistivity of the Si epitaxial layer and ZnO film thickness, and 3) an improvement for lowering SAW propagation lsos and resistance of output circuit. The experiments were carried out for two specifications each with a 20-mm and 40-mm gate length. The highest efficiency (F_T) of −35 dBm was obtained in the gate length of 20 mm while the time-bandwidth product (*BT*) was 107. The highest *BT* product of 227 was obtained in the gate length of 40 mm, while F_T was −47.5 dBm. At the present time, the maximum available *BT* product is less than 320 due to the group velocity dispersion.**

I. Introduction

COMPARED WITH the other types of SAW convolvers, a ZnO–SiO$_2$–Si Sezawa wave convolver [1]–[3] has the following advantages 1) simple assembly because of monolithic structure, 2) high efficiency, and 3) wide bandwidth compared with a ZnO–SiO$_2$–Si Rayleigh wave convolver.

We have already reported on the Sezawa wave convolver [3] with the time-bandwidth (*BT*) product of 102 and F_T of −43.1 dBm. The value of F_T was the highest among the SAW convolvers with the same value of *BT* product, in which no amplifier was included.

On the other hand, a Sezawa wave convolver has a disadvantage that the available *BT* product is limited by the frequency dispersion of group velocity due to its layered structure.

In this paper we developed the detailed design theory of a Sezawa wave convolver and showed experimental results on the device performance. We also discuss the design capability of the Sezawa wave convolver.

II. Design Theory

A. Efficiency (F_T)

Two counter propagating acoustic waves interact with each other through the nonlinearity of space-charge layer capacitance [4] at the silicon surface in a ZnO–SiO$_2$–Si Sezawa wave convolver. Khuri-Yakub and Kino [5] defined the internal convolver efficiency (*M*-value) of a ZnO–SiO$_2$–Si Rayleigh wave convolver using the similar analysis to that of air gap convolver [6].

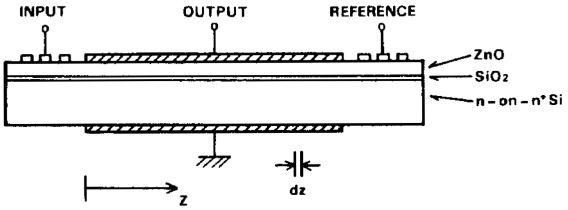

Fig. 1. Schematic configuration of a monolithic ZnO-SiO$_2$-Si Sezawa wave convolver.

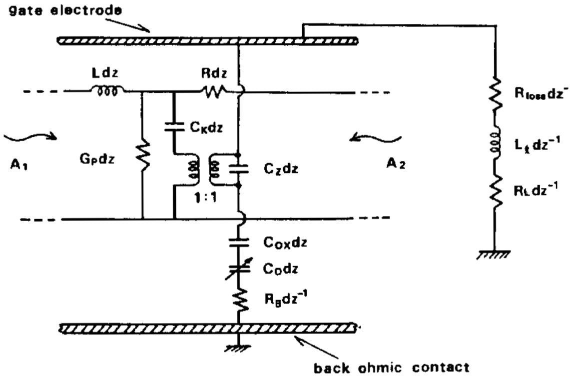

Fig. 2. Equivalent circuit for the interaction region at gate electrode.

In order to obtain the value of convolver efficiency more accurately, we have introduced an idea of conversion resistance between ω and 2ω circuits. We have directly obtained the terminal efficiency (F_T), taking account of the matching condition of the output circuit using the equivalent circuit model (Fig. 2). The calculated value of terminal efficiency F_T ($= P_3/P_1P_2$) (where P_1 and P_2 are the input power, and P_3 is the output power) is in good agreement with the experimental results [3].

According to our analysis, the expression of F_T under the small signal approximation is given by

$$F_T(\mathrm{dBm}) = 10 \log \left\{ \frac{2Be^{-\alpha_0 l}(1 - e^{-2\alpha_0 l})}{C_Z k^2 v \alpha_0} \right\} + 20 \log F_{\mathrm{in}} - 30 \qquad (1)$$

and

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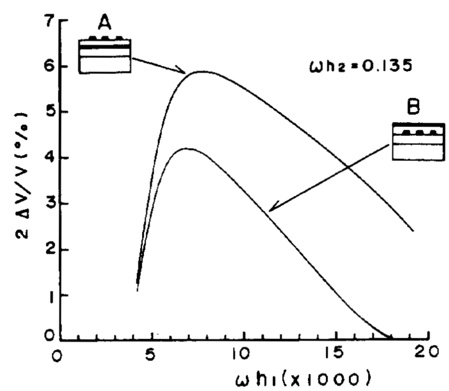

Fig. 3. Sezawa wave coupling coefficient $2\Delta V/V$ versus normalized ZnO film thickness for ZnO-SiO$_2$-(110) [001] Si structure, where h_1, h_2, and ω are the ZnO thickness, SiO$_2$ thickness, frequency, respectively.

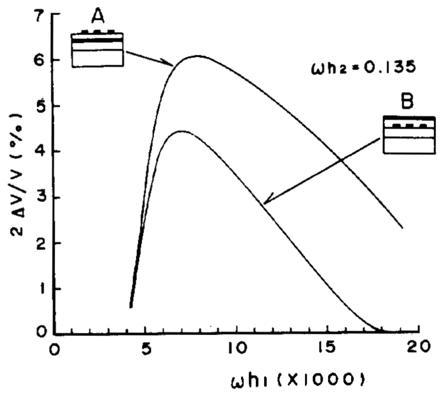

Fig. 4. Sezawa wave coupling coefficient $2\Delta V/V$ versus normalized ZnO film thickness for ZnO-SiO$_2$-(110) [001] Si structure.

$$B = \frac{3k^6\gamma_2^2C_1^4C_z^3}{16v(R_B + R_{\text{loss}})\,\{C_1^2 + C_z^2(1 + k^2)^2\,(1 + \omega^2C_1^2R_B^2)\} \times \{C_1^2 + 2C_1C_z(1 + k^2) + C_z^2(1 + k^2)^2\,(1 + \omega^2C_1^2R_B^2)\}} \tag{2}$$

where

α_0	SAW propagation attenuation coefficient
k	electro-mechanical coupling coefficient
R_B	Si bulk resistance
R_{loss}	2ω output circuit resistance
B	mode coupling coefficient
v	Sezawa wave phase velocity
l	gate length
C_1	series capacitance of SiO$_2$ and Si depletion layer
C_z	ZnO capacitance
ω	input angular frequency
F_{in}	input transduction efficiency of interdigital transducer (IDT).

The following ways for improving efficiency are obtained from this analysis.

1) Optimum Design of ZnO Film Thickness: The purpose of this design is to obtain large electromechanical coupling coefficient. We have reported that a larger value of k^2 could be obtained on a ZnO-Si structure by using (110) cut [001] propagation and (100) cut [011] propagation compared with that of (100) cut [001] propagation [3]. Furthermore, we have found that the analysis of ZnO-SiO$_2$-Si structure which was the actual structure showed a larger value of $k^2(\sim 2\Delta V/V)$ than ZnO-Si structure (Figs. 3 and 4). In Figs. 3 and 4, A and B correspond to the configurations at a transducer and a center gate, respectively. A surface acoustic wave can generate a large potential at the SiO$_2$ surface when the configuration B shows a large k^2; i.e., $\omega h = 5500 \sim 9500$. The efficient and wideband transducer can be obtained when the configuration A shows a large k^2; i.e., $\omega h = 5500 \sim 13\,000$. Thus the ZnO film thickness at the transducer and the center gate should have the same value; i.e., $\omega h = 5500 \sim 9500$.

2) Optimum Design of Resistivity of Si Epitaxial Layer: The purpose of this design is to obtain a large capacitance nonlinearity (γ_2). The capacitance nonlinearity γ_2 is defined by

$$\gamma_2 = \frac{1}{2}\left(\frac{\partial^2 V}{\partial Q^2}\right)_{Q_0} = \frac{1}{2C_1}\frac{\partial}{\partial V}\left(\frac{1}{C_1}\right)_{V_0} \tag{3}$$

where

V_0	dc voltage applied to SiO$_2$,
C_1	capacitance of SiO$_2$-Si system,
V, Q	voltage and charge of SiO$_2$-Si system, respectively.

It is noted that the less impurity density in the epitaxial layer results in the larger capacitance nonlinearity. It is also noted that the epitaxial layer thicker than the maximum depletion layer width (W_m) is required.

The value of γ_2 depends on an external bias voltage. The result of numerical calculation is shown in Fig. 5. A large value of γ_2 is obtained in a range from depletion region to inversion region (bias voltage: $-1.5 \sim -8$ V). However, at strong inversion region, F_T decreases because the propagation loss increases as minority carriers increase.

A more detailed analysis will be published in a forthcoming paper, where the effect of SAW propagation loss due to acousto-electric effect on ZnO-SiO$_2$-Si structure is taken into consideration.

3) Improvement for Lowering SAW Propagation Loss: The ZnO film made by sputtering usually shows fiber-grain structure. The propagation lsos in ZnO film is higher than that in ZnO single crystal and is influenced by sputtering techniques and deposition conditions [7]. In the case of our magnetron sputtering film, the propagation loss of 7.5 dB/cm is obtained at the frequency of 215 MHz in the ZnO-SiO$_2$-Si structure. Further improvement of the quality of sputtering ZnO film for lowering the propagation loss is desirable for a large BT device.

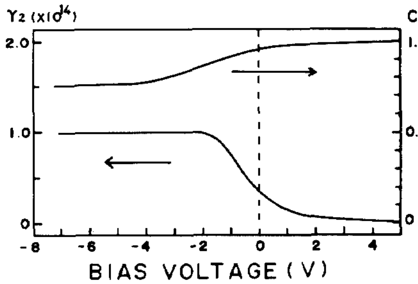

Fig. 5. Capacitance nonlinearity γ_2 and normalized gate capacitance C versus bias voltage on ZnO-SiO$_2$-Si structure. The donor impurity density in the epitaxial layer of silicon is 2.0×10^{14} cm^{-3}. The ZnO and SiO$_2$ film thickness are 4.96 μm and 0.1 μm, respectively.

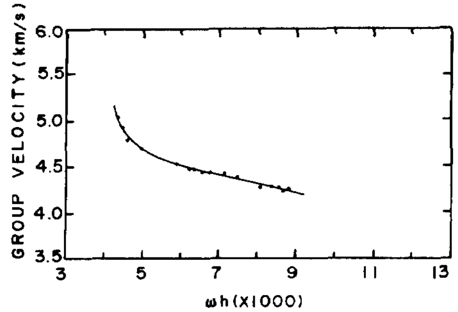

Fig. 6. Measured group velocity Vg versus normalized frequency ωh on ZnO-SiO$_2$-(110) [001] Si structure, where h is the ZnO film thickness. $\partial Vg/\partial\omega h = 0.0825$ at $\omega h = 6700$.

4) Improvement for Lowering Resistance of Output Circuit: The resistances in a 2ω output circuit are silicon bulk resistance and resistances in a 2ω electric circuit. The use of an epitaxial wafer is effective in order to reduce the silicon bulk resistance. The resistances in a 2ω electric circuit are resistance components of bonding wires and matching circuits. It is required to decrease all the resistance components as low as possible.

B. The Maximum BT Product

The disadvantage in a Sezawa wave convolver is that an available *BT* product is limited by the frequency dispersion of the group velocity. The measured dispersion characteristic of group velocity is shown in Fig. 6. The height of output correlation peak is degraded by the dispersion of group velocity.

Fig. 7 shows the calculated curves for an available *BT* product as a function of gate length by using Morgan's analysis [8] for the Sezawa wave convolver. The degradation of a correlation peak valve is taken as a parameter in Fig. 7. Assuming that the practical gate length is 5 cm, input center frequency is 300 MHz and allowable degradation of a correlation peak is 1.5 dB, the maximum *BT* product is 320 (B = 27.9 MHz and T = 11.5 μs) as shown in Fig. 7.

C. Dynamic Range

The dynamic range is defined as the power range in which an output power shows a bilinear characteristic for input powers. The lower and the upper boundaries are determined as a thermal noise level and 1-dB compression point of an output power, respectively. In a Sezawa wave convolver on ZnO-SiO$_2$-Si structure, the maximum output power is limited by the saturation of capacitance nonlinearity γ_2 due to a large potential induced at silicon surface by the SAW. The maximum output level of -15 dBm is experimentally obtained (l = 12 mm). The thermal noise level is a sum of the kTB and the noise figure of output circuits. It is easy to realize experimentally the thermal noise level of -90 dBm when the output bandwidth is less than 60 MHz. Furthermore, in an actual correlator, there are spurious signals due to 1) $\omega - 2\omega$ circuit isolation, and 2) reflection of the SAW.

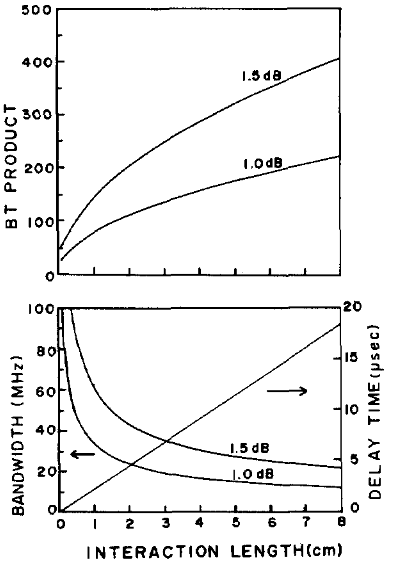

Fig. 7. Available *BT* product versus interaction length (upper), and delay time and available bandwidth versus interaction length (lower). The allowable value in degradation of correlation peak is taken as a parameter. Calculations are for Vg = 4350 m/s, $\partial Vg/\partial\omega h = 0.0825$, f_0 = 300 MHz and $\omega h = 6700$, where f_0 is center frequency.

The feedthrough noise of 2ω component from input signals and the spurious 2ω signal generated under the gate electrode are included in item 1). It is practically effective to use a low-pass filter at an input circuit and a shield electrode between the input transducer and the center gate for suppressing the spurious noise.

The spurious noise included in item 1) is mainly a self-convolution signal produced by the interaction between the input wave and the wave reflected within or outside the center gate. The reflection of SAW within the center gate can be reduced by improvement of the uniformity of ZnO film. The reflection level of SAW at the impedance-matched normal interdigital transducer is about -6 dB. Fig. 8 shows the calculated curves of self-convolution suppression versus gate length with the propagation loss as a parameter.

Various techniques such as dual-gate configuration [9] and unidirectional transducers [10] can be used in order to suppress the self-convolution more effectively in a low propagation loss medium and a short gate length.

III. Device Performances

We have fabricated two kinds of convolvers with different *BT* products using our design theory. Fig. 9 shows

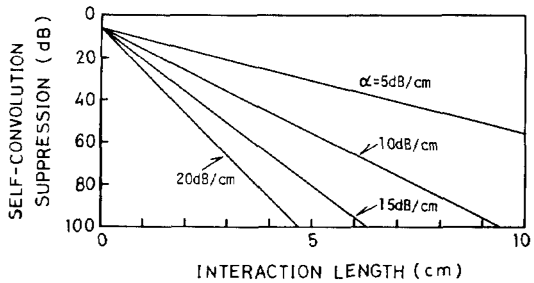

Fig. 8. Self-convolution suppression level versus interaction length with the propagation loss α as a parameter.

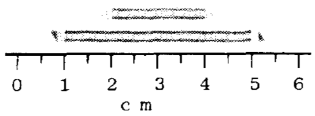

Fig. 9. Photograph of Sezawa wave convolver chips. The lower convolver chip is one for demodulating DPSK signals. The size of the upper and lower chip is 25× 2 mm and 45 × 2 mm, respectively.

TABLE I
DEVICE PARAMETERS

Gate length (mm)	20, 40
Acoustic beam width (mm)	0.5 ~ 1
ZnO thickness (μm)	4.96
Center frequency (MHz)	215
Donor impurity density in Si epi. layer	1 ~ 2 × 10^{14}
SiO$_2$ thickness (μm)	0.1
IDT finger pairs	6

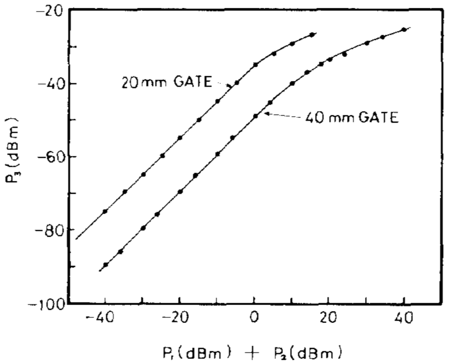

Fig. 10. Output power versus sum of two input powers. P_1 and P_2 are input power, and P_3 is the output power.

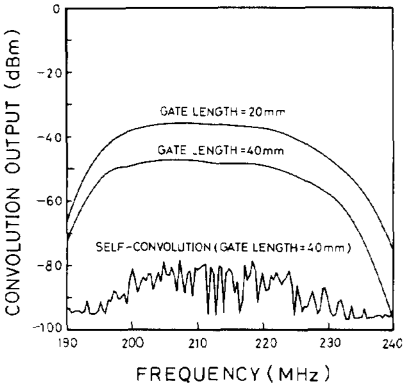

Fig. 11. Convolution and self-convolution output power versus input frequency. (P_1 = P_2 = 0 dBm).

TABLE II
CHARACTERISTICS OF THE SEZAWA WAVE CONVOLVER

Gate length (mm)	20	40
Delay time (μs)	4.6	9.2
Bandwidth (MHz)	23.2	24.7
BT product	107	227
Dynamic range (dB)	58	53
Terminal efficiency (dBm)	−35	−47.5
Spurious suppression (dB)	30	30

TABLE III
DESIGN CAPABILITY OF THE SEZAWA WAVE CONVOLVER[1]

	Present	Near Future
Bandwidth (MHz)	< 35	< 50
Delay time (μs)	< 16	< 18
BT product	< 320	< 520
Center frequency (MHz)	< 300	< 500
Dynamic range (dB)	< 80	< 80
Spurious suppression (dB)	< 40	< 50
Terminal efficiency (dBm)	< −35	< −30

[1] It is noted that there are various trade-offs among these characteristics.

ZnO-SiO$_2$-Si Sezawa wave convolver chips. The device parameters are shown in Table I. In the device with 40-mm gate, the gate is separated at the center for demodulating DPSK (differential phase shift keying) signals. The experimental characteristics of output power versus input power at the center frequency is shown in Fig. 10. Fig. 11 shows the output power versus frequency (input power = 0 dBm). The device performances are listed in Table II. The highest efficiency of −35 dBm was obtained in the gate length of 20 mm, where BT = 107 and the dynamic range is 58 dB. On the other hand, the highest BT product of 227 was obtained in the gate length of 40 mm, where F_T = −47.5 dBm and the dynamic range is 53 dB. Due to the SAW reflection at the discontinuity of the center gate electrode, the spurious suppression in the 40-mm gate length device was smaller than the expected value of about 40 dB.

IV. DESIGN CAPABILITY

Table III gives the design capability of a Sezawa wave convolver on ZnO-SiO$_2$-Si structure. This design capability is determined by overall estimation from theoretical and experimental results. The SAW convolver with f_0 = 300 MHz and BT = 320 can be fabricated on ZnO-SiO$_2$-Si structure.

V. CONCLUSION

We have developed a new detailed design theory of a ZnO-SiO$_2$-Si Sezawa wave convolver. Based on our design theory, we fabricated a monolithic SAW convolver with high performance. The terminal convolver efficiency F_T = −35 dBm was obtained in the gate length of 20 mm, while time bandwidth was 107. The time–bandwidth product of 227 was obtained in the gate length of 40 mm, while F_T was −47.5 dBm.

We also discussed the limit of the device performance of a Sezawa wave convolver. The Sezawa wave convolver has various practical advantages such as high efficiency and a wide dynamic range for the systems, where the required time-bandwidth product is less than 320.

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Kazuo Tsubouchi, for a photograph and biography see page 644 of the September 1985 issue of this TRANSACTIONS.

Nobuo Mikoshiba, for a photograph and biography see page 644 of the September 1985 issue of this TRANSACTIONS.