

# A novel clock recovery circuit for fully monolithic integration

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# A Novel Clock Recovery Circuit for Fully Monolithic Integration

Koichi Murata, *Member, IEEE*, and Taiichi Otsuji, *Member, IEEE*

**Abstract**—This paper presents a novel clock recovery circuit that offers fully monolithic integration. The circuit consists of just the transistor gates of an exclusive OR for an edge-detector and a free-running T-type flip-flop for a high- $Q$  oscillator. As the first proof of the concept, we assemble a circuit using discrete integrated circuits and confirm half-rate clock extraction from an nonreturn to zero data stream input. In order to examine feasibility of the circuit in practical use, we assemble a clock and data recovery circuit. The circuit exhibits stable operation with the bit-error rate of less than  $1 \times 10^{-12}$ .

**Index Terms**—Clock and data recovery circuit, clock recovery circuit, fully monolithic integration, injection locking, and optical transmission systems.

## I. INTRODUCTION

**D**UE TO THE rapid growth in multimedia services, backbone networks must offer much larger transmission capacity. Up to now, 40 Gbit/s time division multiplexing (TDM) transmission experiments in the research stage have been successfully carried out [1]. A clock and data recovery (CDR) circuit is a key component of optical transmission receivers. The CDR generally consists of a decision circuit for realizing regeneration, and a clock recovery circuit (CRC) for realizing retiming. CDR research is emphasizing not only the operating speed but also fully monolithic integration because the monolithic circuit is superior to the multichip configuration in terms of size, cost of assembly, and reliability.

Monolithic integration of the CRC is the key to achieve the goal of the one-chip CDR. There are two CRC configurations. The first realizes a nonlinear extraction technique using a differentiator, rectifier, limiting amplifier, and high- $Q$  filter such as a resonator filter or tank filter. Such CRC's have simple circuit configuration, but the filter is difficult to integrate with other electrical circuits. The second configuration uses the phase-locked loop (PLL) technique. Recently, several types of 40-Gbit/s-class monolithic CRC's based on the PLL technique have been demonstrated [2]–[4]. However, these CRC's are not truly monolithic because they need external components such as voltage-controlled oscillators (VCO's), filters, and/or resonator filters. Monolithic integration of this type of CRC

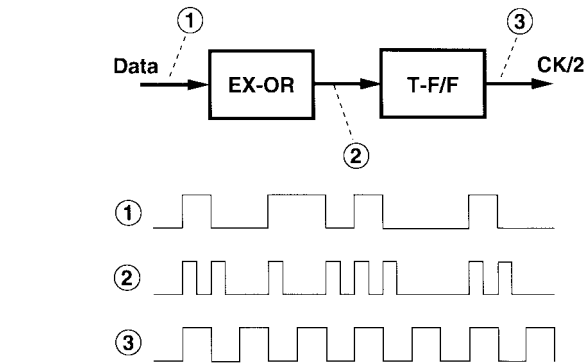


Fig. 1. Conceptual schematic of the CRC.

is prevented mainly by the high-frequency analog VCO's and large capacitors used in the low-pass filters.

This paper describes the configuration of a novel CRC that can be fully and monolithically integrated. The circuit consists of just an exclusive OR (EX-OR) and a free-running T-type flip-flop (T-F/F), and its operation is based on the injection-locking principle. As the proof of the concept, two types of CRC's are assembled using discrete integrated circuits (IC's). The first CRC consists of a 40-Gbit/s-class InP high electron-mobility transistor (HEMT) EX-OR IC [5] and a 10-Gbit/s-class GaAs MESFET T-F/F IC [6]. The second CRC, which consists of the EX-OR IC and a 40-Gbit/s-class InP HEMT T-F/F IC [7], is examined for higher bit-rate operation. Both CRC's successfully extract a half-rate clock signal from nonreturn-to-zero (NRZ) data streams. In order to examine the feasibility of the design in practical use, we assembled a CDR using the first CRC. The CDR exhibited stable operation with the bit-error rate of less than  $1 \times 10^{-12}$  at the bit-rate of 9.799 Gbit/s. In Section II, we describe the proposed CRC configuration. The experimental results of the CRC and CDR are presented and discussed in Section III.

## II. CIRCUIT CONFIGURATION

### A. CRC Configuration

Fig. 1 shows a conceptual schematic and time chart of the proposed CRC. The circuit consists of an EX-OR gate as an edge detector and a free-running T-F/F as a high- $Q$  oscillator. Here, the edge detector is indispensable for an NRZ data signal because it does not include a frequency component of the clock signal. An NRZ data signal is input to the EX-OR gate. The clock signal component is generated from the input NRZ

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data stream by the differentiation and full-wave rectification operation of the EX-OR gate. The signal is then input to the T-F/F operating in the self-oscillating state. When the input signal has a carrier component equal or close to the self-oscillation frequency, the T-F/F oscillation is injection locked to the carrier frequency, which results in half-rate clock signal extraction from the NRZ input data stream. Here, it should be noted that the T-F/F operates as a logic circuit, when the input power is sufficiently large, which disturbs the self-oscillation state. Therefore, the input power must be so small as to block the normal logic operation in order to ensure injection-locking operation. The proposed CRC is categorized as a nonlinear clock-extraction circuit while the injection-locking principle is used for clock extraction. This is because the nonlinear clock frequency component extraction process is common to both the proposed CRC and the conventional nonlinear CRC that consists of a differentiator, rectifier, limiting amplifier, and high- $Q$  filter. The difference between them is the circuit configuration realizing the filtering function and amplification. In the proposed CRC, the T-F/F realizes these functions simultaneously.

The characteristics of the T-F/F are important in this CRC configuration. This is because the self-oscillation frequency determines the extracted clock signal frequency that corresponds to the system bit-rate, and the tunable range of the self-oscillation frequency determines the operating margin of the CRC. The  $Q$ -factor and gain of the T-F/F are key parameters for determining the CRC's tolerance to consecutive identical digits on the analogy of the theory of the conventional nonlinear CRC. These T-F/F parameters tightly depend on the circuit configuration of the T-F/F. In order to clarify how the T-F/F characteristics affect the CRC characteristics, we assembled two CRC's that had the same configuration except for the T-F/F. The first CRC used a 10-Gbit/s class commercial GaAs MESFET IC based on a master-slave-type T-F/F (MS T-F/F). The second CRC used a 40-Gbit/s-class InP HEMT T-F/F IC based on a high-speed latching-operation flip-flop (HLO T-F/F) [8].

The proposed CRC configuration possesses the following merits for fully monolithic integration.

- 1) The circuit offers monolithic fabrication without any external component because only transistor gates are used.
- 2) As shown later, the self-oscillation frequency of these T-F/F's can be tuned over quite a wide range. These features are attractive for use in practical systems.
- 3) The EX-OR gate does not require high-conversion gain because the input power to the T-F/F oscillator must be so small as to block normal logic operation.

As described in Section, II-B, the input power of the T-F/F in a CRC is expected to be much lower than  $-20$  dBm, which also means that the CRC operates with low input power. This feature is important in realizing practical monolithic CDR's.

### B. T-F/F Circuit Configuration and Characteristics

Fig. 2(a) and (b) shows the circuit diagram of the MS T-F/F and HLO T-F/F, respectively. Here, the circuit diagrams

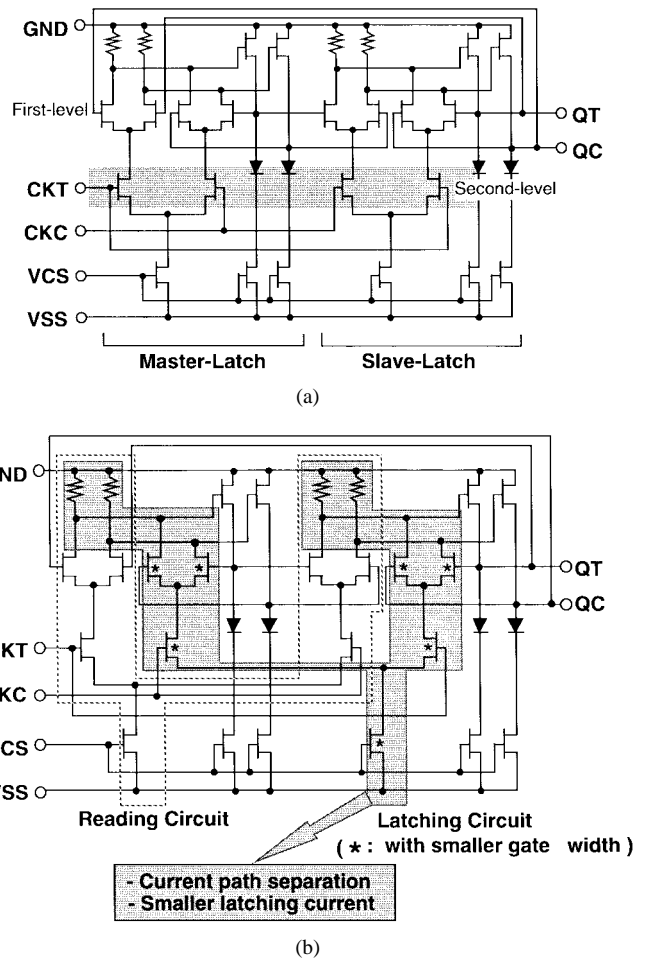
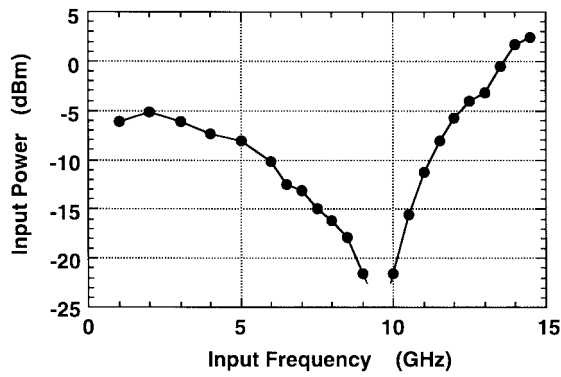


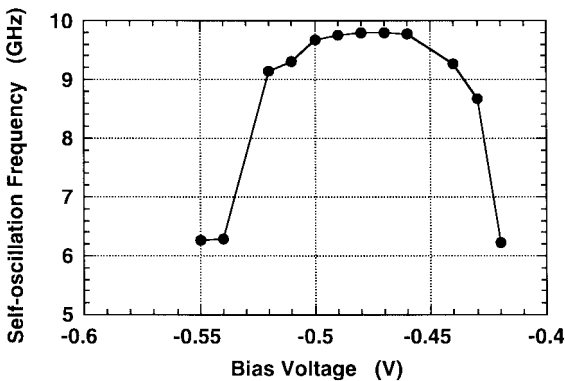
Fig. 2. Circuit diagram of T-F/F's. (a) MS T-F/F. (b) HLO T-F/F.

are drawn, assuming the use of enhancement-type FET's. Both T-F/F's are basically configured as two-level series-gate circuits. The two most important differences between the MS T-F/F and HLO T-F/F are the combination of second-level FET's in the series gate circuits and the smaller operating current of the latching circuit. The series-gate connection in the HLO T-F/F separates the current paths of the reading and latching circuits, and the operating current of the latching circuit is designed to be smaller than that of the reading circuit. This configuration ensures reduced voltage swing in the latching operation, which offers a shorter transition time in latching. As a result, the circuit has higher maximum operating speed than the conventional MS T-F/F that has the same operating current in both reading and latching circuits. On the other hand, lowering the voltage swing in the latching operation degrades the operating margin in the low-frequency region, which sometimes results in restricting the normal circuit operation in the low frequency. In the GaAs MESFET T-F/F IC [6], the reading and latching elements have the same gatewidths. The widths of the reading and latching gates of the InP HEMT T-F/F IC [7] are set to 20 and 10  $\mu\text{m}$ , respectively.

When the input power to the clock signal input terminals (CKT and CKC) is extremely small, the T-F/F falls into the self-oscillation state, the frequency of which is determined by the propagation delay time of the first-level circuits [8]. The



(a)



(b)

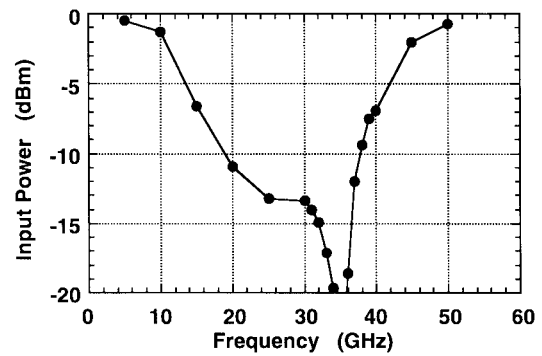
Fig. 3. Characteristics of the GaAs MESFET T-F/F IC. (a) Input sensitivity and (b) tunable range of the self-oscillation frequency.

operating currents of the first-level circuit can be varied by the input bias voltage levels of the second-level FET's, which results in changing the propagation delay time. Consequently, the oscillation frequency can be easily tuned by the bias voltages. Fig. 3(a) shows the measured input sensitivity of the GaAs MESFET T-F/F IC. The IC operates as a static frequency divider, which means the IC operates from dc up to 14.5 GHz. The self-oscillation frequency was 9.799 GHz. The frequency can be widely tuned by adjusting the reference bias voltage level; the measured tuning range of the IC was over 800 MHz, as shown in Fig. 3(b). Fig. 4(a) and (b) shows the input sensitivity and tuning range of the self-oscillation frequency, respectively, of the InP HEMT T-F/F IC. The IC operates over 50 GHz as a quasi-static frequency divider, which means that the IC has a minimum operating frequency of 5 GHz for normal operation. The self-oscillation frequency was 17.55 GHz with the wide tuning range of 800 MHz.

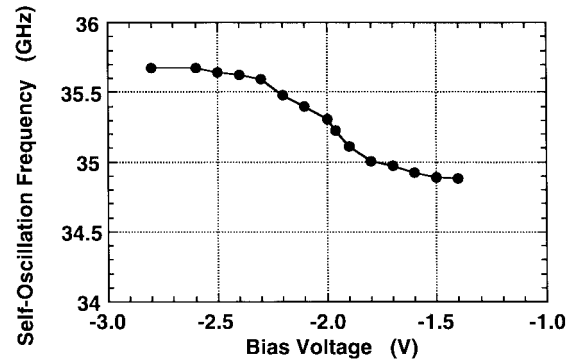
### III. EXPERIMENTAL RESULTS

#### A. CRC

The experimental setup used to confirm CRC operation is shown in Fig. 5. The input data bit-rates were set to the self-oscillation frequencies. For the first CRC, the data signal was generated by a 10-Gbit/s pulse pattern generator (PPG). The data signal was divided into two streams, which were then phase shifted against each other by a half-bit in order to ensure



(a)



(b)

Fig. 4. Characteristics of the InP HEMT T-F/F IC. (a) Input sensitivity and (b) tunable range of self-oscillation frequency.

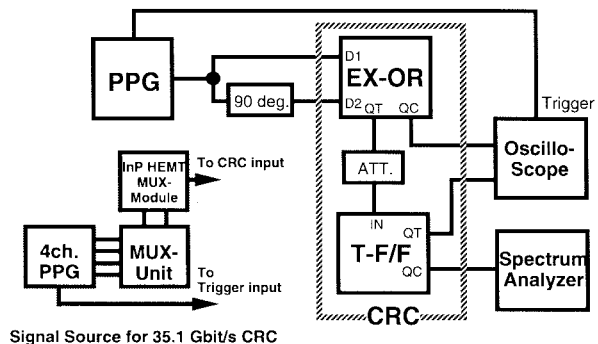
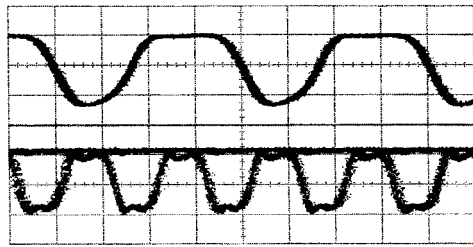


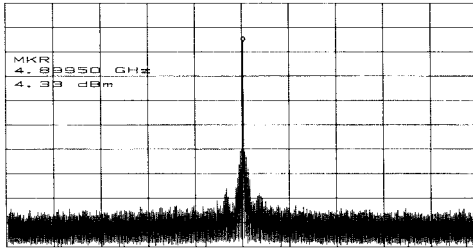
Fig. 5. Experimental setup.

the differentiation and full-wave rectification operation in the EX-OR IC. They were then input to the EX-OR IC. The output signal of the IC was attenuated, and was input to the T-F/F IC. Synchronization was confirmed by means of a spectrum analyzer and by a digitizing sampling oscilloscope triggered by the PPG. The experimental setup for the second CRC was the same as that for the first CRC, except for data signal generation, as indicated by the grayed rectangle in Fig. 5. A 10-Gbit/s four-channel PPG and a 20-Gbit/s MUX unit (Anritsu MP1778, MP1779) and 40-Gbit/s-class InP HEMT module [9] were used for 35.1-Gbit/s data signal generation. The 4-channel PPG generates four parallel pseudorandom bit-sequences (PRBS's) maintaining a delay of a quarter data period relative to each other. Therefore, the multiplexed data signal is truly a PRBS.



Upper: Extracted clock signal (4.8995 GHz)  
Lower: EX-OR IC Output ( $2^{31}$ -1 PRBS input)

(a)



RL: 20.0 dBm, 10 dB/div.  
Center: 4.8995 GHz, Span: 10 MHz  
RBW: 1 kHz, VBW: 1 kHz

(b)

Fig. 6. Operating waveforms of the first CRC. (a) Operating waveforms of the first CRC. (b) Spectrum of the extracted clock signal.

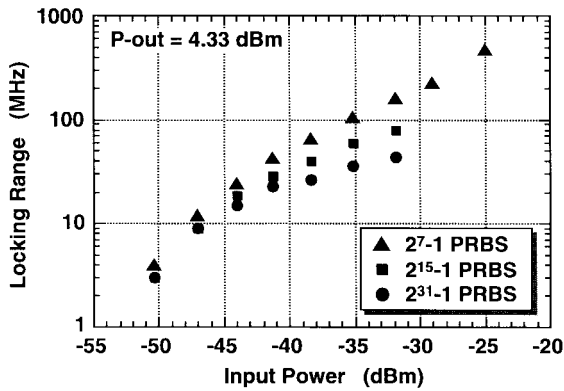


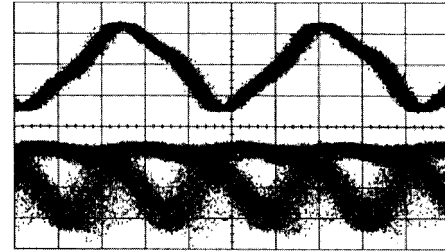
Fig. 7. Locking range of the first CRC.

Fig. 6(a) and (b) shows the operating waveforms of the first CRC and a spectrum of the extracted clock signal, respectively, when the input bit-rate was set at 9.799 Gbit/s (the self-oscillation frequency of the T-F/F IC). Fig. 7 shows the relationship between the input power of the T-F/F and locking range. Clock extraction was confirmed for the input power range from  $-50.3$  to  $-25$  dBm for the  $2^7 - 1$  PRBS data stream, and that from  $-50.3$  to  $-31.8$  dBm for both the  $2^{15} - 1$  PRBS and the  $2^{31} - 1$  PRBS data streams. The output power was approximately constant at 4.33 dBm in these input power ranges. When the input power had exceeded the input power range, clock-extraction operation was not obtained because the T-F/F IC exhibited logic operation. The CRC even handled a  $2^{31} - 1$  PRBS data input signal that has 31 consecutive identical digits. The obtained locking range is

TABLE I  
FIRST CRC'S CHARACTERISTICS

Input Data Rate	9.799 Gbit/s	$2^{31}$ -1 PRBS NRZ
Center Frequency	4.8995 GHz	
Output Power	4.33 dBm	
Locking Range*	23 MHz	
RMS Jitter*	2.23 ps (3.96 deg.)	
Phase Noise*	-100 dBc/Hz	@100 kHz Offset

\* Input power of T-F/F oscillator : -41 dBm



Upper: Extracted clock signal (17.55 GHz)  
Lower: EX-OR IC Output ( $2^{15}$ -1 PRBS input)

Fig. 8. Operating waveforms of the second CRC.

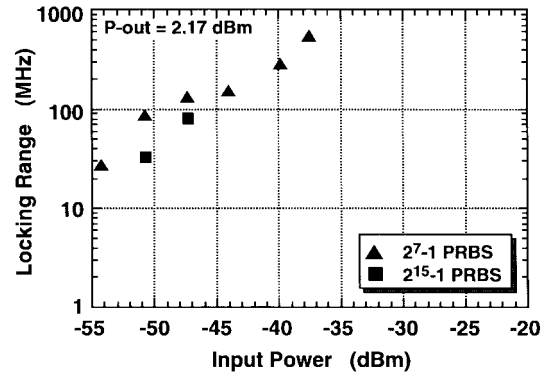


Fig. 9. Locking range of the second CRC.

approximately proportional to the square-root of the injection power, as described in [10]. A 23-MHz locking range was obtained at a typical input power of  $-41$  dBm for the  $2^{31} - 1$  PRBS data input. The rms jitter was 2.23 ps, as calculated from the measured single-sideband phase noise at the input power examined. The CRC characteristics are summarized in Table I.

Figs. 8 and 9 show the operating waveforms of the second CRC at the input bit-rate of 35.1 Gbit/s and the locking range of the CRC, respectively. Clock extraction was confirmed for the input power range of  $-54.2$  to  $-37.5$  dBm for the  $2^7 - 1$  PRBS data stream, and  $-50.7$  to  $-47.3$  dBm for the  $2^{15} - 1$  PRBS data stream. The output power was approximately constant at 2.17 dBm over the input power range. Clock extraction failed if the input power exceeded these ranges. Moreover, clock extraction could not be confirmed when the PRBS contained over 15 consecutive identical digits. A 131-MHz locking range and 0.22-ps rms jitter were obtained at a typical input power of  $-47.3$  dBm when  $2^7 - 1$  PRBS data was input. The second CRC characteristics are summarized in Table II.

TABLE II  
SECOND CRC'S CHARACTERISTICS

Input Data Rate	35.1 Gbit/s	$2^7-1$ PRBS NRZ
Center Frequency	17.55 GHz	
Output Power	2.17 dBm	
Locking Range*	131 MHz	
RMS Jitter*	0.22 ps	
Phase Noise*	-96 dBc/Hz	@100 kHz Offset

\* Input Power of the T-F/F oscillator : -47.3 dBm

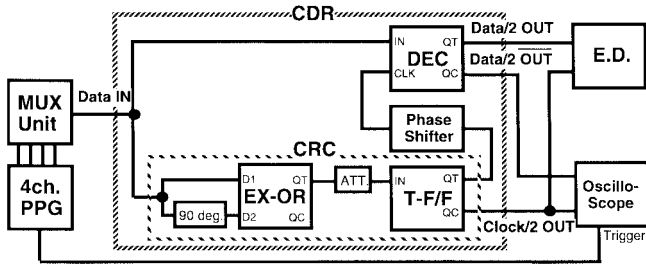


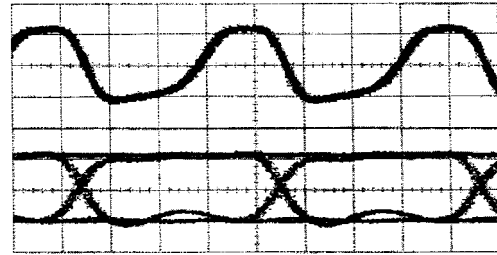
Fig. 10. Circuit configuration of the CDR and its experimental setup.

### B. Clock and Data Recovery Circuit

In order to examine the stability and feasibility of using the CRC in a practical CDR, we assembled a CDR using discrete IC's. The experimental setup, which includes the CDR configuration, is shown in Fig. 10. The circuit consists of an Si-bipolar decision IC (DEC) [11] and the first CRC. The input data signal is divided into two streams that are then input to the DEC and the CRC. The extracted half-rate clock signal is input to the DEC, via a discrete phase shifter, in order to ensure precise phase alignment of the clock and data signals. As a result, the DEC demultiplexes the input data signal into a half-rate data signal. The CDR has a demultiplexing function besides the regeneration and retiming function. Setting two DEC's in parallel yields a CDR with full-demultiplexing function, which means that the two channel half-rate data signals are output simultaneously.

The bit-error-rate of the demultiplexed data signal was measured using, as the input, a data signal generated by a 10-Gbit/s 4-channel PPG and a 20-Gbit/s MUX unit (Anritsu MP1778, MP1779). As described above, this signal generator configuration assures a PRBS for the multiplexed data signal. The bit-error rate was measured using a 10-Gbit/s error detector (E.D.). The voltage swing and bit-rate of the input data signal were set to  $1 V_{P-P}$  and 9.799 Gbit/s, respectively. The attenuation value was set to 38 dB (typical), which corresponds to the T-F/F input power of -44 dBm. The operating waveforms of the CDR are shown in Fig. 11 for the input of a  $2^{31} - 1$  PRBS data signal. The extracted half-rate clock signal and the demultiplexed data signal were clearly observed, and the bit-error rate was confirmed to be less than  $1 \times 10^{-12}$ . This indicates that the stable CDR operation was achieved. The measured phase margin of the decision circuit for the  $2^{31} - 1$  PRBS data signal was 15 ps, and that for the  $2^7 - 1$  PRBS data signal was larger at 68 ps.

All of these experiments were executed under the condition of relatively high CRC input power, thus, the EX-OR operated in the saturation region. Actually, since the EX-OR IC has high



Upper: Extracted clock signal  
480 mV/div., 50 ps/div.  
Lower: Regenerated data signal  
500 mV/div., 50 ps/div.  
( $2^{31}-1$  PRBS input)

Fig. 11. Operating waveforms of the CDR.

conversion gain [12], an attenuator was inserted between the EX-OR IC and T-F/F IC in order to adjust the power injected into the T-F/F IC. As shown in Figs. 7 and 9, both CRC's operate even at T-F/F input power to less than -40 dBm. The measured EX-OR input powers that yielded the output power of -40 dBm at carrier frequencies of 9.799 and 40 GHz were -14 and -6 dBm, respectively [12]. Therefore, it is expected that the input power to the CRC, which corresponds to the input power to the EX-OR IC, can be further reduced. This high input sensitivity characteristic is important for realizing monolithic 40-Gbit/s-class high-speed CDR's. For example, the highest reported input sensitivity at 40 Gbit/s was over  $150 mV_{P-P}$  for  $2^{15} - 1$  PRBS input even for the fastest DEC [13]. From the viewpoint of increasing the input power margin of the decision circuit, the CRC is suitable for high-speed monolithic CDR's.

### IV. CONCLUSION

We presented a simple CRC configuration that uses only a free-running T-F/F and the transistor gates of an EX-OR and, thus, realizes fully monolithic CDR integration. Circuit operation is based on the injection-locking principle and is categorized as a nonlinear clock-extraction circuit. As the proof of the concept, two CRC's were assembled with discrete IC's to evaluate the circuit characteristics. Both were found to offer half-rate clock signal extraction from an input NRZ data signal with good CRC characteristics. In the proposed CRC, the T-F/F circuit configuration is the key to achieving high tolerance to consecutive identical digits. We experimentally confirmed that MS T-F/F is superior to HLO T-F/F in terms of increased tolerance. A CRC using an MS T-F/F IC was found to accept a  $2^{31} - 1$  PRBS input signal that has 31 consecutive identical digits. The CRC configuration has attractive features for monolithic CDR integration such as inherently high input sensitivity. A discrete CDR consisting of a DEC and the first CRC exhibited stable operation with the bit-error ratio of less than  $1 \times 10^{-12}$ . We believe that the proposed CRC is a promising candidate for realizing high-speed fully monolithic CDR's.

### ACKNOWLEDGMENT

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