Optical repeater circuit design based on InAlAs/InGaAs HEMT digital IC technology

doi: 10.1109/22.643831

Optical Repeater Circuit Design Based on InAlAs/InGaAs HEMT Digital IC Technology

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***Abstract*— This paper describes an optical repeater circuit that uses an InAlAs/InGaAs HEMT digital integrated circuit (IC) chip set. The chip set includes a 64-Gb/s 2:1 multiplexer (MUX), a 40-Gb/s demultiplexer (DEMUX), a 46-Gb/s decision circuit (DEC), and a 48-GHz frequency divider (DIV). Electrically multiplexed and demultiplexed 40-Gb/s 300-km transmission is successfully demonstrated.**

***Index Terms*—HEMT, optical communication, optical repeaters.**

I. Introduction

MUCH effort is being devoted to expand the transmission bit rates of backbone networks to realize multimedia communication systems. We have developed a 10-Gb/s time division multiplexing (TDM) system and brought it into commercial use [1]. TDM systems based on fully digital technology are the most practical and most mature in terms of accurate phase matching, reliability, and cost. On the other hand, optical TDM (OTDM) and wavelength division multiplexing (WDM) techniques have been reported as potential candidates to increase the performance. OTDM techniques can increase the transmission bit rate to 400 Gb/s [2], [3] and WDM techniques yield throughputs beyond 1 Tb/s [4], [5]. However, it is true that the drastic increase in transmission capability are based on high-speed electronic integrated circuit (IC) technology, and some breakthroughs are needed to realize practical systems. OTDM systems have difficulty in phase matching, and WDM systems require significant advances in photonic devices. Therefore, it is very useful to increase the single-channel bit rate with progress in TDM techniques. One of the major issues in implementing an ultra-high-speed TDM system is ultra-high-speed electronic IC's.

This paper describes a 40-Gb/s optical repeater that uses an InP-based HEMT digital IC chip set. First, we describe device and circuit design technologies to achieve operation beyond 40 Gb/s. A novel dynamic D-type flip-flop (D-F/F), and a circuit configuration using wide-band data and clock buffers are proposed. Second, we describe IC performance beyond 40 Gb/s. Third, an optical repeater that uses the HEMT IC chip set is detailed. Electrically multiplexed and demultiplexed 40-Gb/s 300-km transmission is successfully demonstrated.

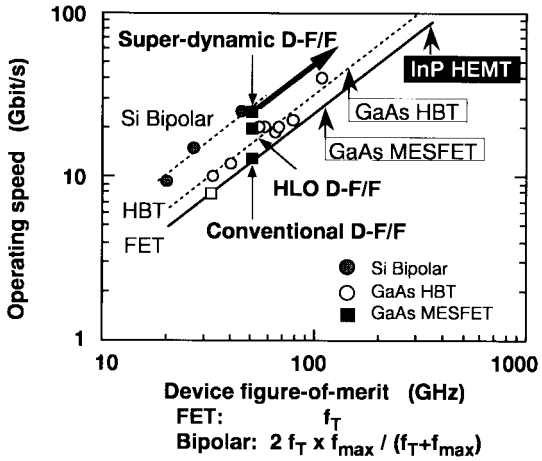

Fig. 1. Relationship between operating speed of D-F/F's and device figure of merit.

II. InP HEMT for Digital IC's

Many electrical IC's reported for over 10-Gb/s transmission systems are Si-bipolar [6], GaAs MESFET [7], heterojunction bipolar transistor (HBT) [8], or high electron-mobility transistor (HEMT) devices. D-F/F is one of the most useful circuits and is used in digital IC's frequently. However, D-F/F speed is a bottleneck in speed performance of digital IC's. Fig. 1 shows the empirical relationship between the maximum operating speed of D-F/F's or decision circuits (DEC's) and the device figure of merit [9]. Roughly speaking, a f_T of 200 GHz is needed to achieve 40-Gb/s operation by a conventional master–slave D-F/F using FET's. Therefore, faster devices are the key to achieving a higher bit rate. InP HEMT offers the highest cutoff frequency (f_T) and maximum frequency of oscillation $(f_{\max})$ of all semiconductor devices [10], [11], and is a good candidate to achieve digital IC's that can operate over 40 Gb/s. It should be noted that due to interconnection parasitic loss, the influence of gate-to-drain

Manuscript received March 31, 1997; revised August 15, 1997.

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Publisher Item Identifier S 0018-9480(97)08328-2.

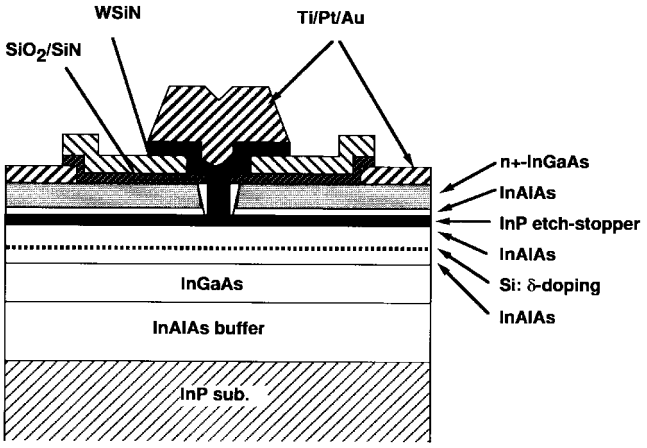


Fig. 2. Schematic cross section of 0.1-μm gate InAlAs/InGaAs HEMT.

capacitance $C_{\rm gd}$ and feedback delay, the operating speed of D-F/F's is not directly proportional to transistor performance. InP HEMT has another advantage in terms of integration with photonic devices such as photodetectors. The integration can reduce connection parasitic loss between electronic IC's and photonic devices, and is suitable for high-speed operation.

Novel circuit-design technology is another key. As shown in Fig. 1, the high-speed latching operation (HLO) [12] and super-dynamic-type D-F/F [13] can achieve bit rates 1.5 times and two times faster than the conventional one, respectively. The combination of the InP HEMT process and advanced circuit design technology promises ultrafast digital IC's for 40 Gb/s and beyond optical repeater circuits. In fact, our first trial IC's, a 2:1 multiplexer (MUX) and a 1:2 demultiplexer (DEMUX), operate at over 40-Gb/s [14] and have successfully achieved 40-Gb/s 300-km transmission [15], [16] even though they represent a preliminary HEMT design.

III. Device Technology

The device we employed is a 0.1-μm gate-length InAlAs/InGaAs HEMT [17], [18]. The schematic cross section of the HEMT is shown in Fig. 2. A novel recess-etch stopper reduces the standard deviation of the threshold voltage $(V_{\rm th})$ to around 30 mV in a 2-in wafer and enables the use of HEMT's in digital IC's. Schottky diodes using the additional InAlAs/n-InAlAs layers on the HEMT layers were used as level shift diodes because of their small size and low resistance. The measured f_T and transconductance (g_m) values are 174 GHz and 950 mS/mm, respectively. $F_{\rm max}$ was estimated to be 400–500 GHz from the equivalent circuit parameters.

IV. Circuit Design

We designed a digital IC chip set including 2:1 MUX, 1:2 DEMUX, DEC, and 1/2 frequency divider (DIV). To achieve a bit rate of 40 Gb/s and beyond, we need: 1) a faster D-F/F; 2) a wide-band data buffer with high voltage gain; and 3) a wide-band clock buffer operating at over 40 GHz. Therefore, we introduce the super-dynamic D-F/F. To cover the D-F/F operating range, we introduce wide-band buffers employing peaking and feedback techniques.

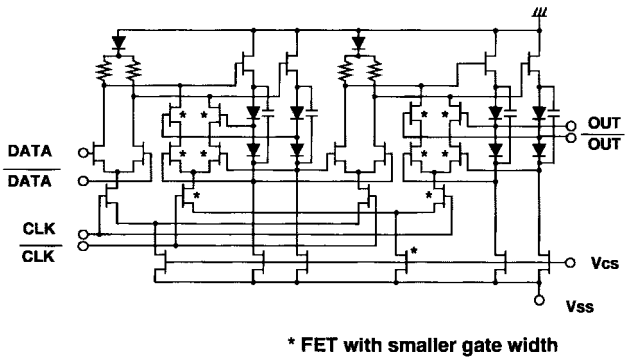
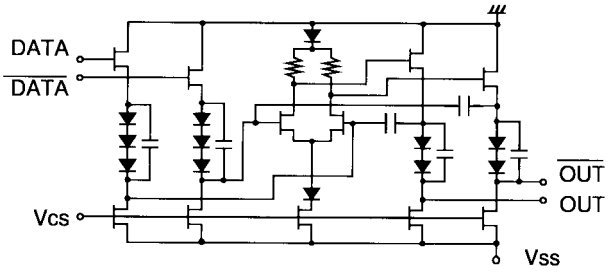
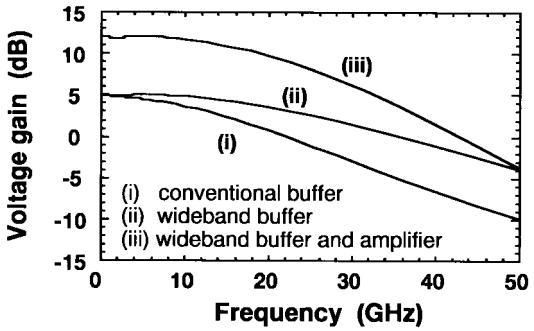


Fig. 3. Circuit configuration of super-dynamic D-F/F.



(a)



(b)

Fig. 4. Wide-band data buffer. (a) Circuit configuration. (b) Simulated gain–bandwidth characteristics.

A. Super-Dynamic D-F/F

The super-dynamic D-F/F is shown in Fig. 3. The circuit features are: 1) a series–gate connection to separate the current paths of the reading and latching circuits; 2) a smaller latching current $(I_{\rm latch})$ than the reading current $(I_{\rm read})$; and 3) a source-coupled negative feedback pair (SCNFP) inserted in the first-level latching differential pair in a cascode manner. The SCNFP's drastically reduce the effective logic swing from $R_L I_{\rm read}$ to $R_L/2(I_{\rm read}$-$I_{\rm latch})$ without any degradation in the signal transition slew rate; R_L is the load resistance. This is the key to increasing F/F speed. To compensate source follower loss in the high-frequency region, capacitive peaking was used in the source followers.

B. Wide-Band Data Buffer and Amplifier

The wide-band data buffer we use consists of a two-stage differential buffer. Fig. 4(a) shows the first stage of the data buffers. The data buffers employ capacitive feedback

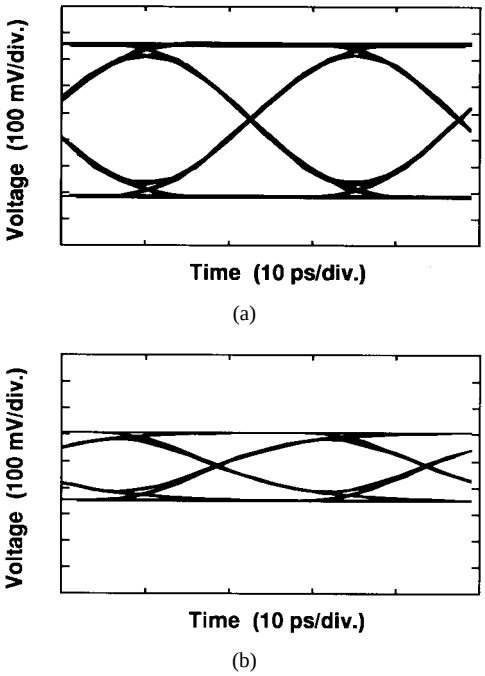


Fig. 5. Simulated eye patterns. (a) Wide-band data buffer and amplifier. (b) Conventional data buffer.

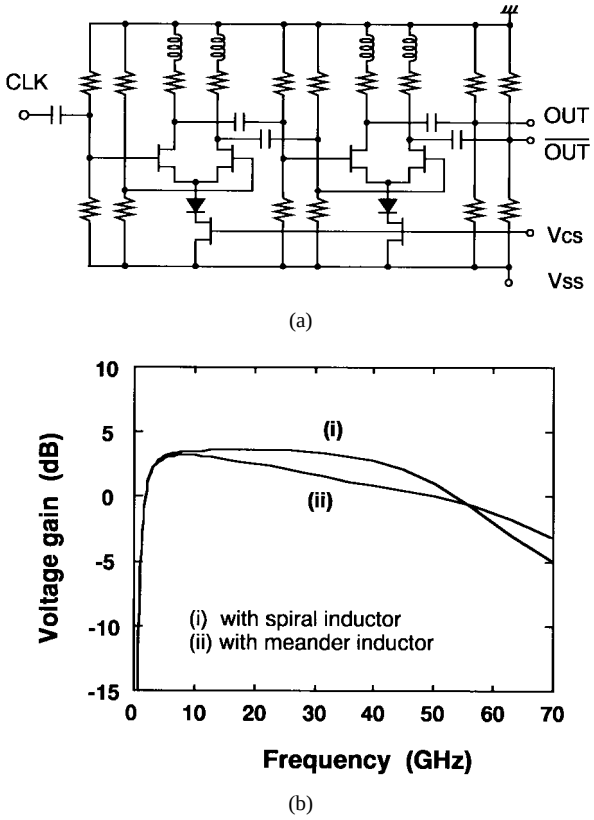


Fig. 6. Wide-band clock buffer. (a) Circuit configuration. (b) Simulated gain–bandwidth characteristics.

at the differential buffer [19] and capacitive peaking at the source follower. Capacitive feedback cancels the influence of the gate-to-drain capacitance $C_{\rm gd}$, and capacitive peaking compensates the source follower loss in the high-frequency region. As the feedback capacitor, gate-to-drain and gate-to-source capacitance in a HEMT was used. The wide-band data amplifier used also employs the same configuration except for the source follower at the input stage. A performance comparison of this wide-band buffer and a conventional buffer is shown in Fig. 4(b). The bandwidth of the conventional buffer is insufficient for 40-Gb/s operation and its voltage gain is not so high. On the other hand, the wide-band buffer offers adequate bandwidth and the gain is still not so high. The data buffer with wide-band amplifiers increases the gain to 12 dB, and its bandwidth is 40% wider than the conventional one. Output eye patterns of the buffers were simulated and are shown in Fig. 5. A 40-Gb/s (2^7-1) pseudorandom bit stream (PRBS) with an amplitude of 150 $\rm mV_{pp}$ was used as the input data. The eye opening is still clear at 40 Gb/s and a large output amplitude, 2.3 times that of a conventional one, is obtained.

C. Wide-Band Clock Buffers

The circuit configuration of the clock buffer is shown in Fig. 6(a). The clock buffer consists of a two-stage inductor peaking differential buffer. A capacitively coupled resistive DIV was introduced as a low-loss passive RF level shifter instead of source followers. The inductors have meander and spiral structures. The equivalent circuits of the inductors were fitted by using an electromagnetic-field simulator and a microwave-circuit simulator. The simulation results predict that the inductors act as inductive elements up to around 60 GHz. The simulated frequency characteristics of the clock buffers are shown in Fig. 6(b). The clock buffer using the meander inductor has a wider bandwidth and is suitable for higher bit-rate operation. Another buffer using the spiral inductor has a higher voltage gain and is expected to achieve shorter rise and fall times at the buffer output around 40 GHz. The meander inductors were used in the DEC and DIV for a high-speed operation, and the spiral inductors were used in the MUX and DEMUX for a better retiming performance. Due to the capacitive coupling, the minimum clock frequency offering adequate amplitude is approximately 1 GHz.

D. Circuit Configuration for High Bit-Rate Operation

The block diagram of the DEC and other IC's, 2:1 MUX, 1:2 DEMUX, and DIV are shown in Fig. 7. All the inputs and outputs employ an SCFL interface. The interfacing requirements for the clock inputs are relaxed because of the capacitive coupling of the clock buffer. All the data and clock inputs are single-ended. To confirm the effect of the wide-band buffer and amplifier, the input data sensitivity of the DEC was simulated by HSPICE. In this simulation, a repeated "1000" pulse was used as the input data. We defined the input data sensitivity as the minimum data amplitude at which the DEC could achieve output amplitude larger than 700 $\rm mV_{pp}$. For comparison, the following three types of DEC's were simulated: a DEC with a conventional data buffer, a DEC with a wide-band data buffer and an amplifier, and a DEC with a wide-band data buffer, an amplifier, and an output amplifier [shown in Fig. 7(a)]. All of them employ the wide-band clock buffer shown in Fig. 5. The simulation results (Fig. 8) show that the sensitivity of the

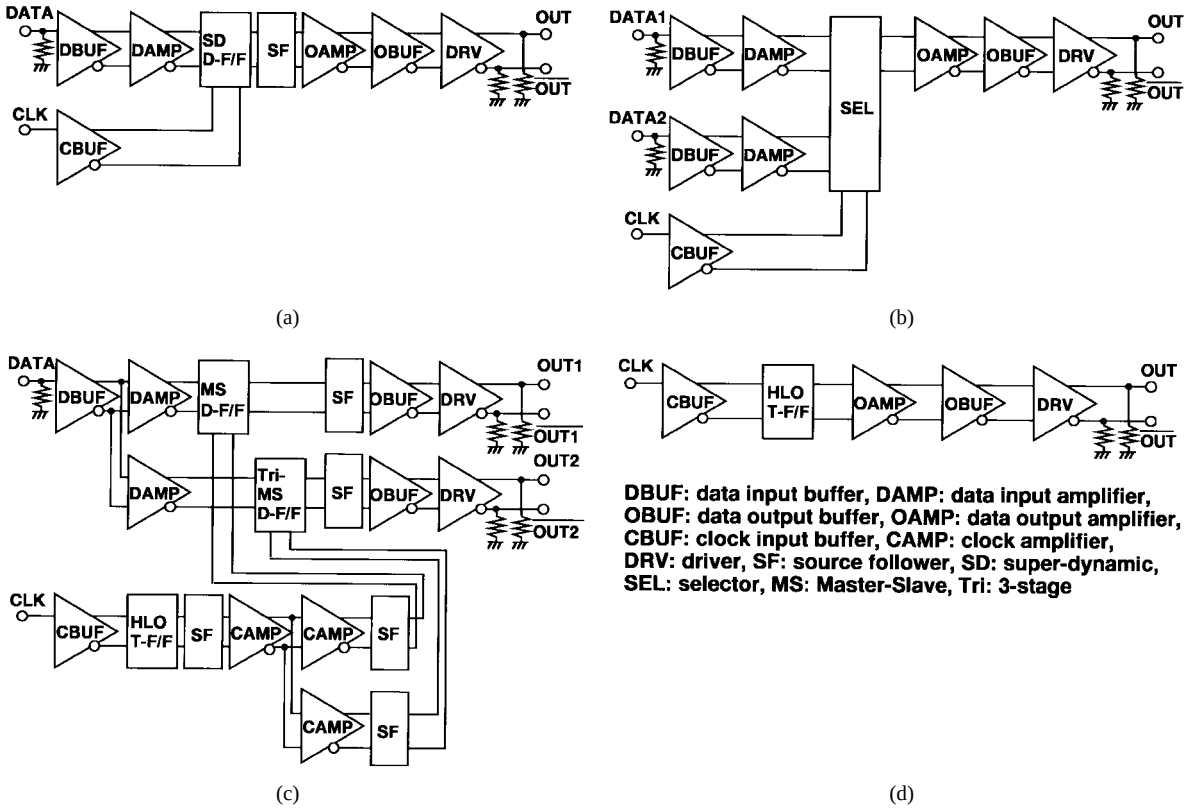


Fig. 7. Block diagram of InP HEMT IC chip set. (a) DEC. (b) 2:1 MUX. (c) 1:2 DEMUX. (d) DIV.

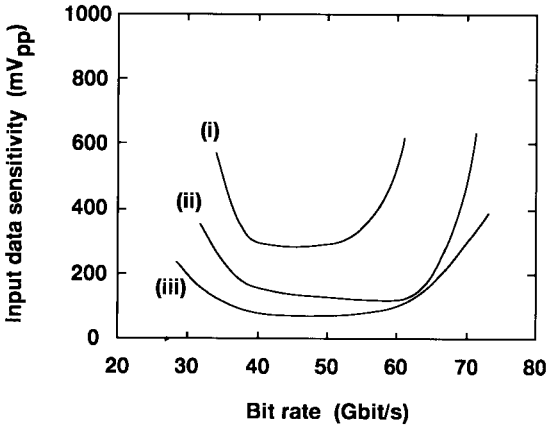


Fig. 8. Simulated input data sensitivity of DEC (i) with conventional data buffer, (ii) with wide-band data buffer and amplifier, and (iii) with wide-band data buffer and amplifier, and wide-band output amplifier.

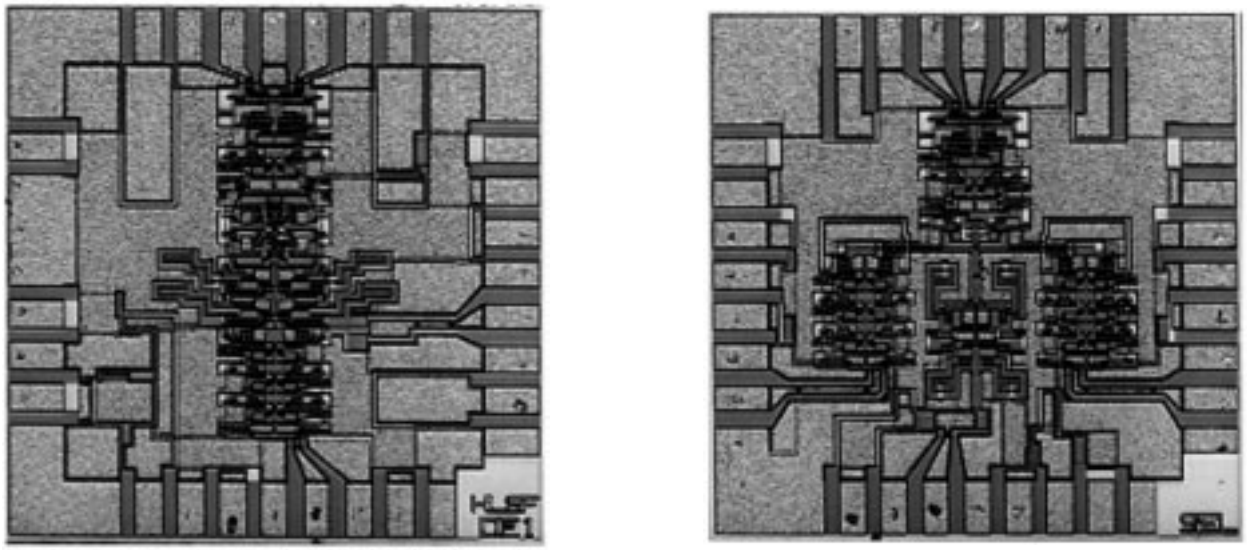
conventional data buffer is relatively low due to the poor voltage gain of the buffer. The degradation of the sensitivity in the low-frequency region is due to the logic swing reduction caused by the SCNFP's in the super-dynamic D-F/F. The conventional data and output buffer cannot compensate for the reduction so its output amplitude falls under 700 mV_{pp} even though the DEC accurately generates the "1000" output. The wide-band data buffer and amplifier achieve higher sensitivity and keep it in the higher bit-rate region. The wide-band output amplifier also compensates for the logic swing reduction and keeps the sensitivity high from the lower to higher bit-rate region. These simulations confirmed that the wide-band buffer and amplifier are very effective for high-speed operation. The same effect was also confirmed in other IC's. The chip sizes were 2×2 mm^2 for the DEC, MUX, DIV, and 3×2 mm^2 for the DEMUX. The power supply voltage (V_{SS}) is -5.2 V. The fabricated IC chip set was embedded in a package that can accommodate up to six RF ports with V-band connectors [20]. The package minimizes the inner cavity in order to shift the cavity resonance outside the transmission bandwidth. The IC's were mounted on a thin-film multilayer interconnection substrate using ribbon wire. Photographs of the fabricated IC's are shown in Fig. 9.

TABLE I
OPERATING SPEED AND POWER DISSIPATION OF IC CHIP SET

IC	on wafer	module	power dissipation
DEC	15 - >40 Gbit/s	15- 46 Gbit/s	1.7 W
2:1 MUX	1 - ~ 64 Gbit/s	1 - 52 Gbit/s	2.2 W
1:2 DEMUX	2 - 40 Gbit/s	2 - 40 Gbit/s	3.8 W
DIV	2 - 46 GHz	2 - 45 GHz	1.1 W

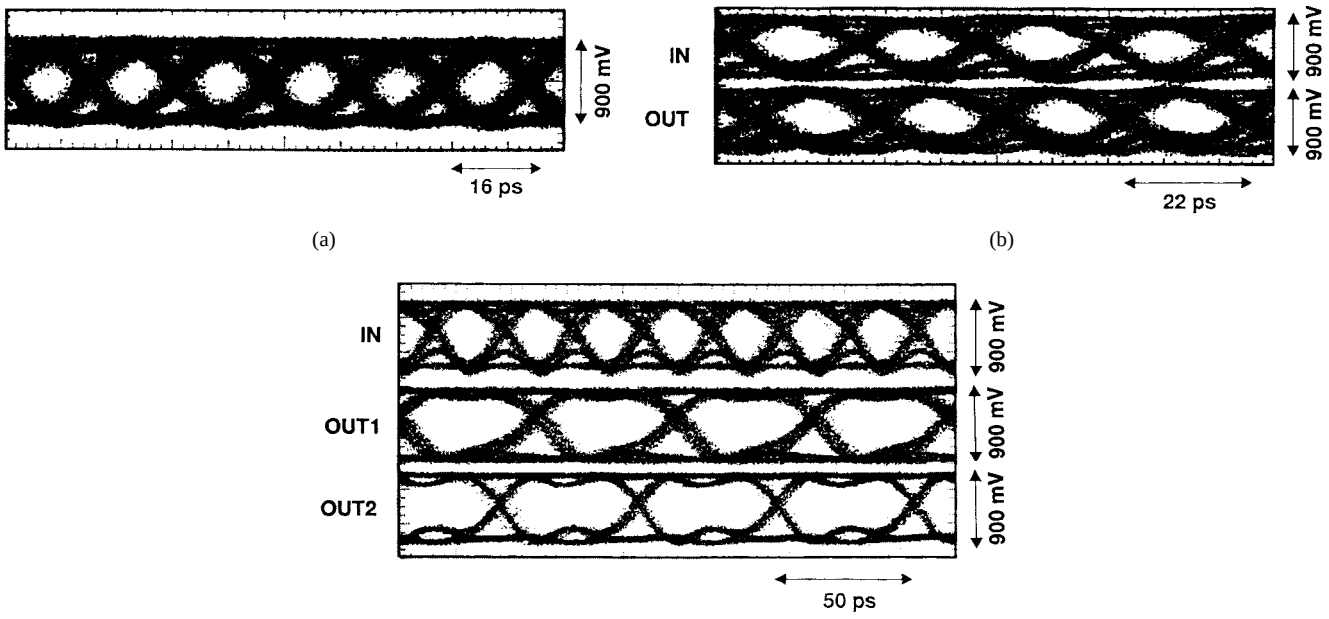
V. IC PERFORMANCE

The performance was measured for devices on the wafer and after packaging. Initially, we measured the maximum operating speed of the IC's. For the signal source, complementary PRBS's from a pulse-pattern generator (PPG), one of which was delayed, were multiplexed by a GaAs MESFET MUX and two HEMT MUX modules. Fig. 10 shows the eye



(a) (b)

Fig. 9. Photograph of (a) DEC chip and (b) 2:1 MUX chip.



(a) (b)

(c)

Fig. 10. Observed eye patterns at the maximum operating bit rate. (a) 2:1 MUX (on wafer), 64 Gb/s, $(2^{31}-1)$ PRBS. (b) DEC module, 46 Gb/s, $(2^{15}-1)$ PRBS. (c) 1:2 DEMUX module, 40 Gb/s $(2^{23}-1)$ PRBS input.

patterns observed by a sampling oscilloscope. The maximum operating speeds and power dissipation are shown in Table I. We confirmed a clear eye opening of the MUX output up to 64 Gb/s (on wafer). For the DEC module, we confirmed an error-free operation up to 46 Gb/s. For wafer measurements, we confirmed clear eye opening up to 40 Gb/s; however, the maximum bit rate is not yet confirmed due to the limitations of the experimental setup. We think the maximum operating speed of the DEC is higher than 46 Gb/s. For the DEMUX, error-free operation was confirmed up to 40 Gb/s. To our knowledge, the eye opening of the MUX at 64 Gb/s, and the error-free operation of the DEC at 46 Gb/s are the fastest data ever reported.

We measured the input data sensitivity and clock-phase margin of the DEC module for PRBS's having lengths of (2^7-1) and $(2^{15}-1)$. The experimental setup is shown in Fig. 11(a). Four-channel PRBS, delayed by a quarter data period against each other, were generated from a PPG. They were multiplexed by two GaAs MESFET MUX's, and further multiplexed using the HEMT MUX module. A part of the generated 40-Gb/s (2^7-1) PRBS observed by a sampling oscilloscope is shown in Fig. 11(b). It is confirmed that the PRBS has a series of seven "1" bits. The $(2^{15}-1)$ PRBS is too long to confirm the series of fifteen "1" bits is in the data by the sampling oscilloscope. However, the 15 "1" bits must be in the data stream because the four PRBS channels

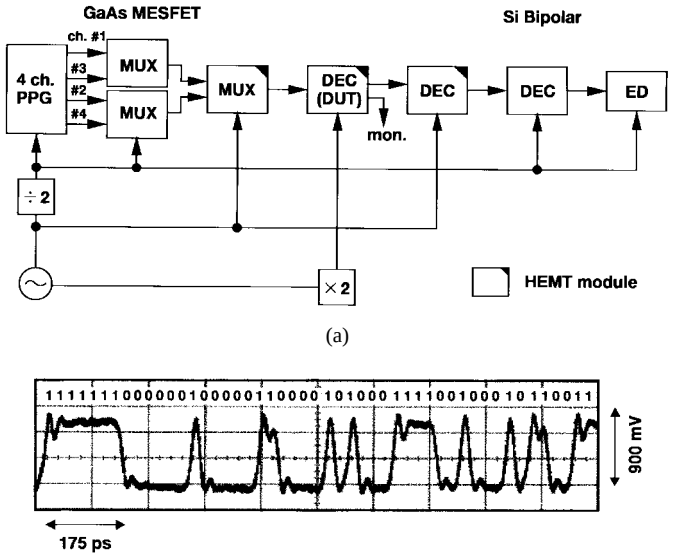


Fig. 11. (a) Experimental setup to measure input data sensitivity and clock phase margin and (b) a part of a 40-Gb/s $(2^7 - 1)$ PRBS (input for DUT).

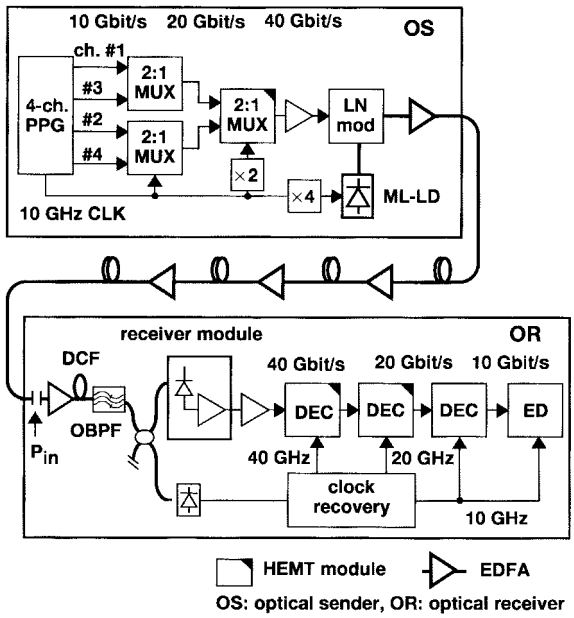


Fig. 13. 40-Gb/s optical repeater.

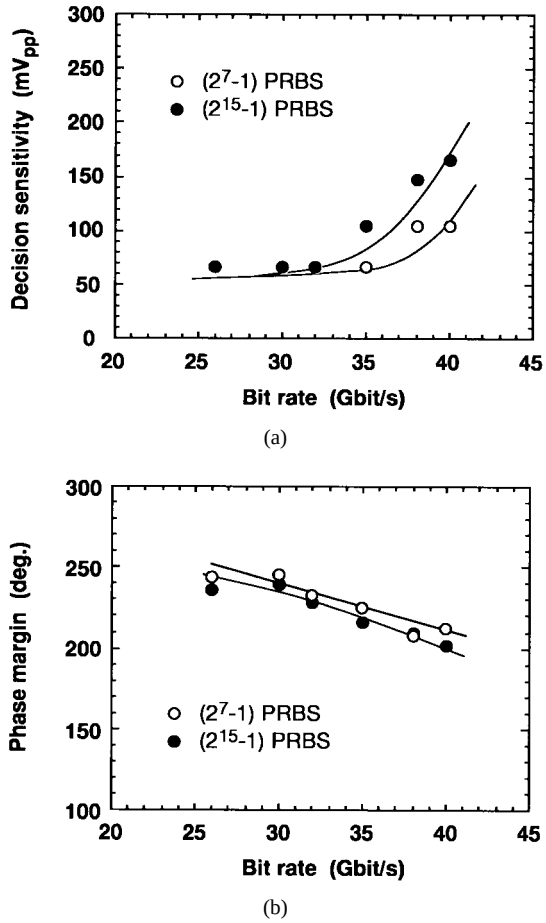


Fig. 12. Measured input data sensitivity and clock-phase margin of DEC module.

maintain a delay of a quarter data period, relative to each other. The generated PRBS was fed into the device under test (DUT) HEMT DEC module as the input data. To measure the sensitivity, the amplitude of the PRBS was attenuated by combinations of 3-, 6-, 10-, and 20-dB attenuators. A bias network (HP11612B; 0.045-50-GHz bandwidth) was used to provide an optimum operating voltage level for an input amplitude of less than about 100 mV_{pp}. The output of the DUT was demultiplexed by another HEMT DEC module to half the rate, and then further demultiplexed to a quarter of the rate to measure the bit error rate (BER) with an error detector (ED). We defined the input data sensitivity as the difference between the centers of data "Hi" and "Low" levels for a BER of better than 1×10^{-11}. For the clock phase margin, we measured the edge drift of the output eye pattern of the DUT for a BER of better than 1×10^{-9} when the clock timing was shifted by a phase shifter. Measured sensitivity and clock-phase margin are shown in Fig. 12. For PRBS length of $(2^7 - 1)$, high input sensitivities of less than 66 mV_{pp} up to around 35 Gb/s and 104 mV_{pp} at 40 Gb/s, and a wide phase margin of 246° at 30 Gb/s and 212° at 40 Gb/s were obtained. The difference between measured sensitivity and the simulation result (Fig. 8) may be for the following reasons. In the simulation, we used a very simple repeated "1000" pattern with ideal rise and fall times as input data. We could not estimate interconnection and structure-dependent parasitic impedance accurately. The package performance had limitations. The degradation of the sensitivity and phase margin for PRBS length of $(2^{15} - 1)$ may be caused by the bandwidth limitation and/or unflat frequency characteristics of the input buffers. The bias network we used seems to be another degradation factor because it does not have enough bandwidth in the low-frequency region.

VI. 40-Gb/s 300-km Transmission

We fabricated an optical repeater using the HEMT IC modules and performed 40-Gb/s 300-km transmission. The experimental setup is shown in Fig. 13. Four-channel 10-Gb/s

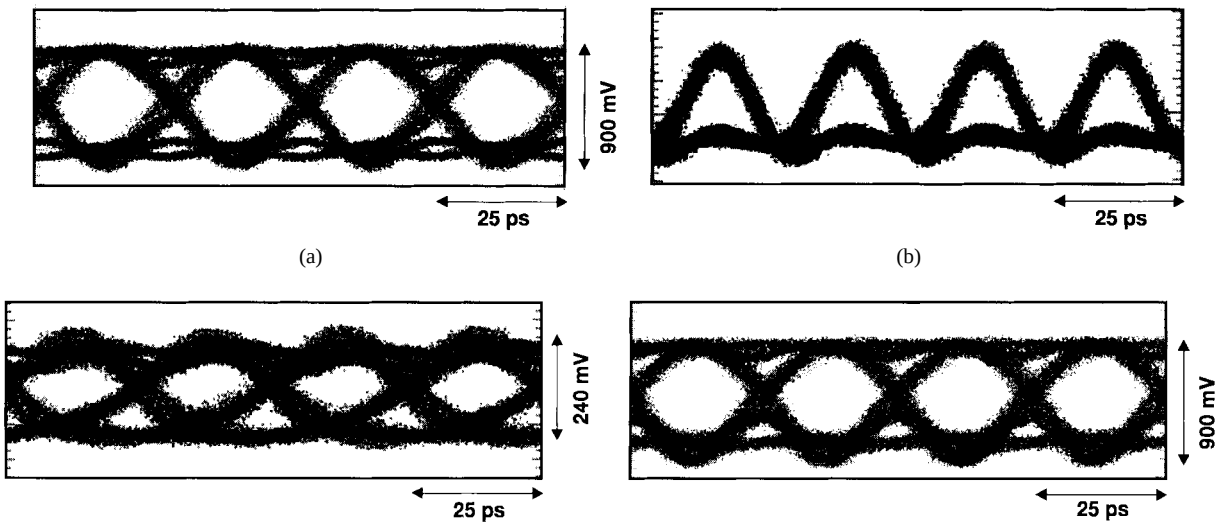


Fig. 14. 40-Gb/s eye patterns of (a) 2:1 MUX, (b) OS, (c) receiver module, and (d) DEC.

PRBS $(2^7 - 1)$ signals from a PPG were multiplexed to 40 Gb/s using two GaAs MESFET MUX's and the HEMT MUX module. The 40-GHz optical pulse train was directly generated by a monolithic mode-locked laser diode (ML-LD) module [21] and was encoded by a Mach–Zehnder modulator [22]. The modulated 40-Gb/s return-to-zero (RZ) optical signal was amplified by an erbium-doped fiber amplifier (EDFA) and injected into the transmission line. The transmission line was comprised of four 75-km-long dispersion shifted fibers (DSF's) connected by three EDFA's. Each EDFA accommodated a dispersion compensator to cancel the dispersion in each section. The transmitted signal was amplified by another EDFA, followed by a dispersion equalizer module [23]. The signal was received by the newly developed optical receiver module comprised of a waveguide-type pin-photodiode and a GaAs MESFET distributed amplifier [24]. The received signal was fed into the HEMT DEC module, then demultiplexed to 10 Gb/s by another HEMT DEC module and an Si-bipolar DEC. The observed 40-Gb/s eye patterns are shown in Fig. 14. The HEMT DEC module generated a clear eye pattern even though intersymbol interference (ISI) was observed in the receiver output. The BER performance of the four 10-Gb/s channels in the 40-Gb/s data stream was measured by adjusting the clock timing of the DEC's, as shown in Fig. 15. The average receiver sensitivities at the BER of 10^{-9} before and after transmission were -24.8 dBm ($d = 0.2$ dB) and -24.3 dBm ($d = 0.6$ dB), respectively. To improve the sensitivity, reducing the ISI of the receiver module is important.

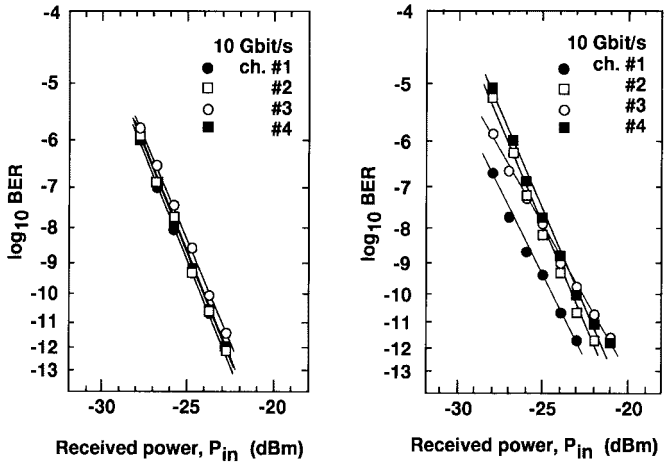


Fig. 15. BER performance at 40 Gb/s. (a) Back-to-back. (b) After 300-km transmission.

VII. Conclusion

We have developed a 0.1-μm gate InAlAs/InGaAs HEMT's digital IC chip set for a 40-Gb/s optical repeater. We have proposed a novel dynamic D-F/F with wide-band buffers, and fabricated a 64-Gb/s 2:1 MUX, a 40-Gb/s DEMUX, a 46-Gb/s DEC, and a 48-GHz frequency DIV. The eye opening of the MUX at 64 Gb/s and the error-free operation of the DEC module at 46 Gb/s are the fastest data rates ever reported. The DEC has shown a high input data sensitivity of 104 mV_{PP} and wide clock-phase margin of 212° for a 40-Gb/s $(2^7 - 1)$ PRBS. The optical repeater using the HEMT IC modules has successfully demonstrated an electrically multiplexed and demultiplexed 40-Gb/s, 300-km transmission. These results show that InP-based HEMT is a potential candidate for 40-Gb/s digital IC's. It is also verified that the super-dynamic D-F/F and wide-band buffer using peaking and feedback techniques are usable for bit rates of 40 Gb/s and beyond, and provide high input data sensitivity and wide clock-phase margin. At the same time, these results indicate that time-division multiplexed 40-Gb/s transmission systems are feasible. However, we cannot conclude that the process and circuit design techniques are sufficient. Larger scale integration is needed to reduce the number of modules. The integration with electronic and photonic devices will

also be needed to reduce the packaging process as well as interconnection paths via RF connectors and cables. Higher input data sensitivity and a wider clock-phase margin will be needed to implement the IC's into practical systems. For this, further work is required to improve and optimize the circuit design and packaging technologies.

ACKNOWLEDGMENT

The authors would like to thank I. Kobayashi, S. Horiguchi, H. Yoshimura, Y. Ishii, and Y. Akazawa for their encouragement and suggestions throughout this work. They also thank Y. Umeda, O. Mitomi, K. Noguchi, H. Miyazawa, K. Sato, T. Kataoka, A. Hirano, and Y. Miyamoto for their support.

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