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A Novel MOS PROM Using a Highly Resistive Poly-Si Resistor

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***Abstract*—A novel MOS electrically programmable read-only memory (PROM) using a highly resistive polycrystalline silicon (poly-Si) resistor as a memory element is proposed.**

In a highly resistive poly-Si, a new memory effect of an irreversible resistivity transition, from an initial highly resistive value to a low-resistive one, is observed. The dependencies of the transition voltage and current, which cause the transition, on the poly-Si deposition conditions, are studied, and the deposition conditions suitable for MOS PROM fabrication are obtained. The transition voltage V_t can be reduced down to 10 V by decreasing the poly-Si film thickness to 0.4 μm. The transition current is less than 10 mA.

A 36-bit MOS PROM, using the poly-Si resistor as a memory element, is fabricated. The programming voltage used in this work is 25 V and the programming time per bit is less than 10 μs. The read access time is less than 300 ns. The programming voltage, however, can be reduced down to 15 V by decreasing the poly-Si film thickness and the series resistance in the circuit. The novel PROM has another advantage in that the poly-Si resistor is compatible with a conventional silicon-gate process.

I. INTRODUCTION

A READ-ONLY MEMORY (ROM) is an important device for code conversion, character generation, and microprogramming. Various types of ROM's have been developed [1]-[7]. Among these ROM's, an electrically programmable ROM (PROM) is remarkably superior to a mask ROM in a small-volume memory system. Moreover, MOS PROM's have an advantage over bipolar PROM's in chip cost.

There are two types of MOS PROM's. One is an alterable PROM. Since alterable PROM's can be erased by applying voltage or by exposing to ultraviolet light, they can be programmed over and over again. They require, however, a high programming voltage, and some of them, such as MNOS, require a very thin gate oxide which is not used in MOS random-access memory. The other is a fusable-link PROM. The programmed state of the fusable-link PROM is stabler than that of the alterable PROM because the programming is carried out by blowing a fusable-link instead of storing charges into a floating gate or a trapping state. However, this PROM also requires a high programming voltage to flow a large programming current.

In this paper, a novel MOS PROM using a polycrystalline silicon (poly-Si) resistor as a memory element is proposed. A poly-Si resistor is composed of highly resistive poly-Si whose resistivity is above $10^3\ \Omega \cdot$cm. An irreversible resistivity transition in highly resistive poly-Si is used for programming the PROM. This PROM is a kind of the fusable-link PROM. The voltage and current required for this transition can be reduced down to 10 V and less than 10 mA, respectively. Therefore, the programming voltage and current of the PROM are small, compared with those of other MOS PROM's. The fabrication process of the PROM requires no special technology because the poly-Si resistor is fabricated by a conventional silicon-gate process.

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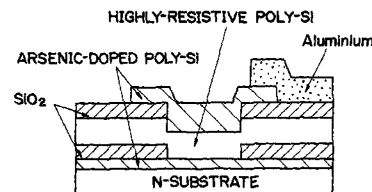

Fig. 1. Cross-sectional view of the highly resistive poly-Si resistor.

Section II describes some experimental results for the irreversible resistivity transition in poly-Si. The deposition condition of poly-Si, which is applicable to a memory element of MOS PROM, is also given. Section III covers the PROM fabrication and experimental results obtained from the PROM. Section IV summarizes the results of this work.

II. MEMORY EFFECT IN HIGHLY RESISTIVE POLY-SI

A. Sample Preparation

The fabrication process of the poly-Si resistor, shown in Fig. 1, is as follows. First, a highly arsenic-doped poly-Si, whose resistivity is below $2 \times 10^{-2}\ \Omega \cdot$cm, is deposited on n-type, (100), 1.5-$\Omega \cdot$cm substrate as a lower electrode. Then, a highly resistive poly-Si, whose resistivity is higher than $1 \times 10^3\ \Omega \cdot$cm, is deposited, by pyrolysis of SiH_4-H_2-AsH_3 system, in an RF-heated horizontal reactor at temperatures between 650 and 750°C. An upper electrode is composed of highly arsenic-doped poly-Si, whose resistivity is about $2 \times 10^{-2}\ \Omega \cdot$cm, and aluminum metallization on top of the poly-Si electrode. CVD SiO_2 is used to insulate the highly resistive poly-Si from each electrode, except for the active region, and the current path is constructed perpendicular to the substrate, as shown in Fig. 1.

B. Current-Voltage Characteristics

Typical current-voltage characteristics of the poly-Si resistor are shown in Fig. 2. In the initial highly resistive state, the current is proportional to the voltage in a low applied voltage region. Though the current becomes unproportional to the

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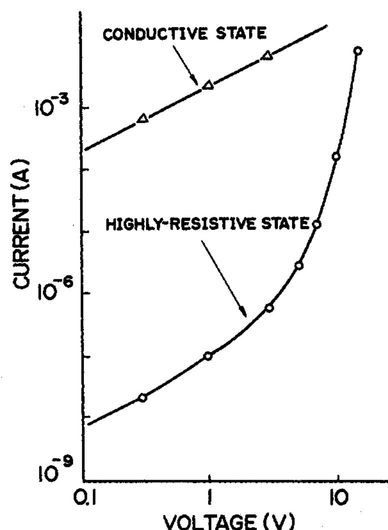

Fig. 2. Current–voltage characteristics of the poly-Si resistor.

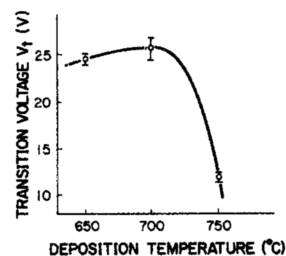

Fig. 3. Deposition temperature dependence of transition voltage V_t.

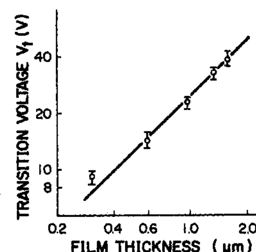

Fig. 4. Film thickness dependence of transition voltage V_t.

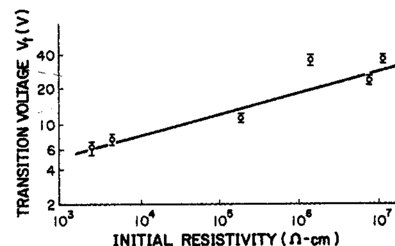

Fig. 5. Initial resistivity dependence of transition voltage V_t.

voltage in a high applied voltage region, the current–voltage characteristic is reversible. When the applied voltage exceeds the transition voltage V_t, the highly resistive poly-Si resistor is changed irreversibly into a low-resistive one. In this low-resistive state, the current–voltage characteristic of the poly-Si resistor is linear over all the voltage region even when a reverse bias is applied.

The current path in this low-resistive poly-Si is observed by the following procedure. An aluminum metallization layer, an upper poly-Si electrode, and an upper SiO_2 film are removed by chemical etching. The highly resistive poly-Si film is Sirtl etched slightly. A selective etched area of about 1-μm diameter is observed. This means that the structure of poly-Si is changed locally. Therefore, it is suggested that 1) the current concentrates in a small area in the low-resistive poly-Si, and 2) the irreversible resistivity transition of the poly-Si resistor is caused by the structural change of highly resistive poly-Si.

A similar memory effect is obtained for a variety of sample structures. For example, it is obtained with a sample in which the lower and upper electrodes are made of an n^+-diffused layer and an aluminum (or molybdenum) metallization layer, respectively. It is also obtained with a sample in which the positions of the upper and lower electrodes are separated in parallel to the substrate, and the current path is constructed obliquely to the substrate.

In this work, arsenic-doped poly-Si is chosen as an upper electrode and the distance between the electrodes is controlled by the film thickness in order to obtain the uniformity of the transition voltage within a lot and for different lots. This memory element using the poly-Si resistor is expected to be compatible with a conventional MOS process.

C. Dependence of Transition Voltage V_t on Deposition Condition

To realize a memory device with the poly-Si resistor, it is indispensable to lower the transition voltage V_t. The relationships between the transition voltage and deposition conditions, such as deposition temperature, film thickness, and partial pressure of AsH_3, are studied.

Fig. 3 shows the deposition temperature dependence of the transition voltage for an undoped poly-Si of 1.0-μm thickness. The transition voltage decreases abruptly above 700°C. The preferred orientation of the poly-Si film changes from the random orientation to the ⟨110⟩ orientation when the deposition temperature is above 700°C. It is considered that the transition voltage depends on the structure of the poly-Si film. To make the transition voltage variation small with the deposition temperature, the deposition temperature should be below 700°C.

Fig. 4 shows the film thickness dependence of the transition voltage for an undoped poly-Si deposited at 700°C. The transition voltage is proportional to the film thickness. The electric field in the film is approximately 2×10^5 V/cm. It is possible to obtain a transition voltage of less than 10 V by decreasing the film thickness down to 0.4 μm, as shown in Fig. 4.

Fig. 5 shows the initial resistivity dependence of the transition voltage for the highly resistive poly-Si with a 1.0-μm thickness, deposited at 700°C. The initial resistivity is varied from 1×10^3 to 1×10^7 Ω · cm by varying the AsH_3 partial pressure during deposition of the poly-Si. The transition voltage tends to increase with the initial resistivity. The transi-

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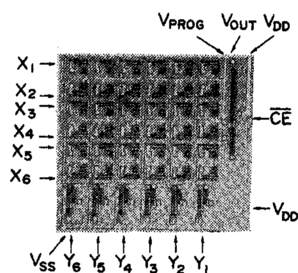


Fig. 6. Microphotograph of the MOS PROM. Effective area is 0.7 mm × 0.7 mm.

tion voltage can be made less than 10 V by lowering the initial resistivity down to $1 \times 10^4\ \Omega \cdot$cm, even for a 1.0-$\mu$m film thickness. Undoped poly-Si, however, is preferable because it is difficult to control the initial resistivity by varying the AsH_3 partial pressure.

D. Application to Memory Element in PROM

As described above, the poly-Si resistor has a memory effect and its transition voltage is low. The pulsewidth dependence of the transition voltage V_t is small; for example, V_t's at 0.1-μs pulsewidth and at 1.0 μs are larger than that under dc condition by only 15 and 5 percent, respectively. The current required for the irreversible transition (transition current I_t) depends on deposition conditions, electrode area, and film thickness. The transition current is from 1 to 10 mA, when the transition voltage is from 25 to 10 V and the electrode area is below 100 μm^2. The total deviations from the average value of the transition voltage V_t and current I_t for different lots are 10 percent for V_t and 30 percent for I_t.

The stability of the poly-Si resistor in low- and highly resistive state is tested at 100°C with an applied voltage of 10 V. The resistance of the poly-Si resistor does not change under these conditions.

The ratio of the resistance in a highly resistive state to that in a low-resistive state is larger than 10^4 in a low applied voltage region at temperatures below 70°C. The temperature dependence of the transition voltage V_t is small; for example, V_t at 70°C is only 10 percent smaller than V_t at room temperature.

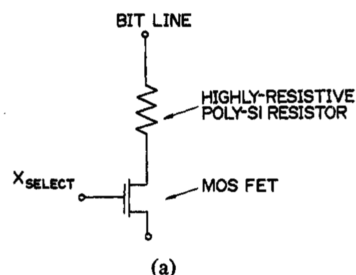
From these results, it is confirmed that the poly-Si resistor will become an excellent memory element of an MOS PROM.

III. MOS PROM

A. Fabrication

A 36-bit MOS PROM using the poly-Si resistor is fabricated. Its microphotograph is shown in Fig. 6. The PROM is constructed with a 6 × 6 bit memory cell array, address selecting MOSFET's, and an output amplifier. Fig. 7(a) and (b) shows an equivalent circuit and a cross-sectional view of a memory cell, respectively. The cell consists of a poly-Si resistor and a selecting MOSFET, which are connected in series.

A conventional n-channel silicon-gate process is used to fabricate this device on a p-type, (100), 1.5-$\Omega \cdot$cm substrate. The MOSFET has a gate oxide thickness of 1000 Å and an



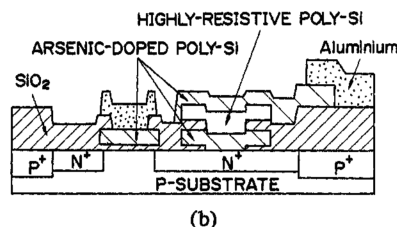


Fig. 7. Memory cell. (a) Circuit diagram. (b) Cross-sectional view.

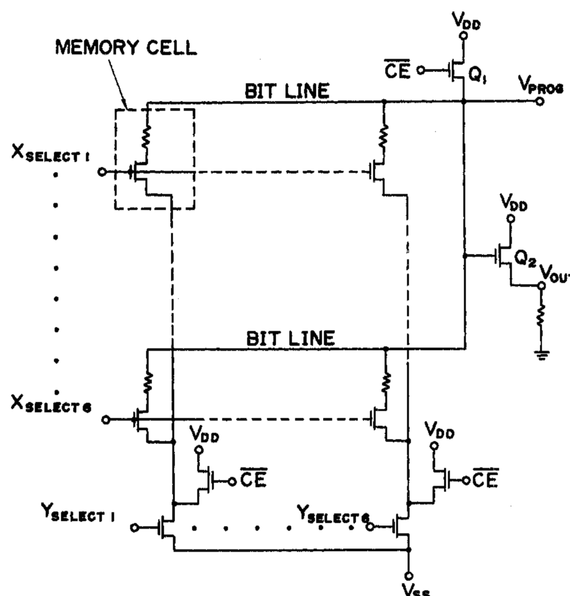


Fig. 8. Circuit diagram of the MOS PROM.

effective channel length of 5 μm. The threshold voltage of the MOSFET is 1.1 V when the substrate bias voltage is −2 V. The poly-Si resistor, as shown in Fig. 1, is constructed with undoped poly-Si on the n^+-diffused drain region of the FET. Undoped poly-Si is deposited at 700°C. The film thickness of poly-Si is selected as 0.6 μm because the transition voltage should be larger than the power supply voltage V_{DD} of the PROM. The transition voltage of this film is expected to be 15 V, while V_{DD} is 10 V.

B. Device Operation

A circuit diagram of the PROM is shown in Fig. 8. The programming operation can be performed as follows. A cell (X_i, Y_j) is selected by raising the $X_{SELECT\,i}$ and $Y_{SELECT\,j}$ line

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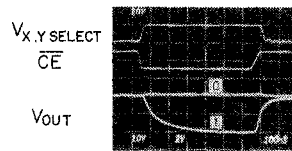

Fig. 9. Operation waveforms.

potentials and a voltage larger than the transition voltage is applied to the V_{PROG}. The resistance of a highly resistive poly-Si resistor is lowered and the programming operation is accomplished at this particular address location. Read operation can be performed in the following manner. The bit line is precharged through a transistor Q_1 by the $\overline{CE}$ signal. A cell (X_i, Y_j) is selected by raising the $X_{SELECT\,i}$ and $Y_{SELECT\,j}$ line potentials. As a result, the potential of the precharged bit line decreases. The time constant of this transient response is determined by the resistance of a highly resistive poly-Si resistor, g_m of the MOSFET, and parasitic capacitance. Since the ratio of the resistance for the poly-Si resistor in a highly resistive state to that in a low-resistive state is about 10^4, the time constant difference between "1" and "0" written in a cell is very large. Therefore, the information in a selected cell can be read by monitoring the bit-line voltage by the source-follower transistor Q_2.

The programming and read operations of the fabricated PROM are successfully verified. The programming voltage is 25 V and time required for programming is less than 10 μs per bit. Read access is less then 300 ns. Output waveforms of this PROM, when stored information "1" and "0" are read, are shown in Fig. 9. The resistor of 5 kΩ is connected to the V_{OUT}. The following voltages are used to operate this PROM:

PROGRAMMING: $V_{X,Y\,SELECT} = 20$ V $V_{PROG} = 25$ V

READ: $V_{X,Y\,SELECT} = 10$ V $\overline{CE} = 10$ V.

In the programming mode, $V_{X,Y\,SELECT}$ is chosen to be 20 V to provide the current required for the programming. On the other hand, $V_{X,Y\,SELECT}$ is chosen to be 10 V in the read mode. A dc bias voltage of 10 V is applied as V_{DD} and that of −2 V as the substrate bias V_{BB}.

In this fabricated PROM using 0.6-μm-thick poly-Si, the programming voltage is expected to be 20 V, taking into account the potential drops in the address selecting transistors. However, the programming voltage V_{PROG} used in this work is 25 V, because of potential drops in the upper poly-Si electrode and common line which is connected in series to the highly resistive poly-Si resistor. The resistance of an upper electrode is more than 500 Ω because it is composed of an arsenic-doped poly-Si whose resistivity is about 2×10^{-2} $\Omega \cdot$ cm as described in Section II-A. The common line, connecting memory cell and Y-select transistor, is composed of a diffused layer whose sheet resistance is about 15 $\Omega/\square$. The total resistance of the common line is, for example, about 1 kΩ for memory cell (X_1, Y_1). The potential drops in the upper poly-Si electrode and the common line can be reduced by optimizing cell structure and physical layout. Therefore, V_{PROG} can be lowered to 20 V. Moreover, V_{PROG} can be reduced down to 15 V since the transition voltage is expected to be 10 V by decreasing the poly-Si film thickness to 0.4 μm.

IV. Conclusions

A memory effect in a highly resistive poly-Si and a novel MOS PROM using this memory effect are described.

An irreversible transition from a highly resistive state to a low-resistive state is observed in a highly resistive poly-Si. The transition voltage V_t at which the highly resistive poly-Si resistor is changed to a low-resistive one can be reduced down to 10 V by increasing the deposition temperature and by decreasing the film thickness and the initial resistivity. The current necessary for this transition is less than 10 mA.

A 36-bit MOS PROM, using the poly-Si resistor as a memory element, is fabricated. This novel PROM has an advantage in that it can be programmed with a low voltage and a small current. In addition, its fabrication process requires no special technology, because the poly-Si resistor is fabricated by a conventional silicon-gate process.

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