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著者	室田　淳一
journal or publication title	IEEE Journal of Solid-State Circuits
volume	17
number	1
page range	62-68
year	1982
URL	http://hdl.handle.net/10097/47723

A Novel 14 V Programmable 4 kbit MOS PROM Using a Poly-Si Resistor Applicable to On-Chip Programmable Devices

MASAFUMI TANIMOTO, JUNICHI MUROTA, MASATO WADA, TAKASHI WATANABE, KENJI MIURA, AND NOBUAKI IEDA

Abstract—A novel fusible-link-type 4 kbit MOS programmable read-only memory (PROM) has been developed with n-channel silicon-gate technology. The programmable element is a poly-Si resistor which makes an irreversible resistivity transition. A low programming voltage of 10 V and a small programming current of 4 mA is obtained by optimizing the undoped polycrystalline silicon (poly-Si) deposition conditions and reducing the electrode area of a poly-Si resistor. The fabrication is compatible with conventional silicon-gate processing. New clock generator and clamping circuits result in low-voltage and high-speed programming. High-speed reading is achieved by adopting a dual X-line layout. The fabricated 4 kbit PROM can be programmed within 5 μs by applying a voltage of less than 14 V. Measured access time is less than 130 ns and active power dissipation is 125 mW at 300 ns cycle time with a single 5 V supply.

I. Introduction

With the rapid progress of LSI technology, the software of digital systems has been replaced by hardware such as LSI devices. Moreover, LSI devices have been customized to realize various functions in digital systems. In order to meet the requirements for customization, they must be composed of programmable devices. Programmable devices such as alterable MOS programmable read-only memories (PROM's) [1]-[7] and fusible-link PROM's [8]-[10] have been used as the instruction memory and the data memory in digital systems for making prototype software codes and data of the systems. PROM's have become more and more important, being used as on-chip programmable devices in VLSI's such as single-chip computers [11], [12] and fault-tolerant random access memories (RAM's) [13]-[15].

Recently, short-channel MOSFET's have been used to enhance device performance in PROM's as well as RAM's. Since the breakdown voltage of these FET's is low, the programming voltage of PROM's should be reduced. Moreover, taking account of the PROM application to on-chip devices, the fabrication process of a PROM must be compatible with that of other components on the same chip. Continuous efforts to reduce the programming voltage of alterable MOS PROM's have been made, but reduction has been carried out only at the sacrifice of the simplicity of the fabrication process. Although a fusible-link PROM using polycrystalline silicon (poly-Si) fuses has been adopted as an on-chip programmable device [15], it is difficult to control the programming using MOSFET's because a large programming current is required to blow the fuse.

As a candidate for a low-voltage PROM for on-chip programmable devices, we proposed a novel MOS PROM using a highly resistive poly-Si resistor as a memory element. This PROM is a kind of fusible-link PROM. The poly-Si resistor makes an irreversible resistivity transition from an initial highly resistive state to a low resistive one [16]. Since the transition voltage is as low as 10 V and the transition current is less than 10 mA, the programming is easily controlled by MOSFET's. Moreover, its fabrication process requires no special technology because the poly-Si resistor is made by a conventional silicon-gate process.

This paper describes the further study of this PROM fabrication technology and the design of a 4 kbit MOS PROM fabricated by the novel MOS PROM technology. Section II describes fabrication technology of the MOS PROM and poly-Si resistor. Section III describes the design of the 4 kbit MOS PROM. Section IV presents the 4 kbit PROM device characteristics. Section V summarizes the results of this work.

II. PROM Fabrication Technology

A. Fabrication Process

A schematic diagram of the PROM fabrication process is shown in Fig. 1. The cell consists of a highly resistive poly-Si resistor and a cell MOSFET which are connected in series [Fig. 1(d)]. MOSFET's are formed by conventional n-channel silicon gate technology [Fig. 1(a) and (b)], and subsequently poly-Si resistors are made on drain regions [Fig. 1(c)]. The highly resistive layer is composed of undoped poly-Si. Arsenic-doped poly-Si is used for both the upper and lower electrodes of the poly-Si resistor. The current path is limited by the area of the through-hole made in the phosphosilicate glass (PSG) layer between the gate and interconnection metal. The PSG is adopted as an intermediate layer to improve surface smoothness [17], instead of SiO_2 used in our previous work [16]. Then the interconnection layer is formed [Fig. 1(d)]. In this process, the undoped poly-Si is deposited after the FET fabrication process, which requires high temperatures. Therefore, the fluctuation in the FET process and/or modification of the FET process do/does not affect the characteristics of

Manuscript received May 26, 1981; revised August 24, 1981.
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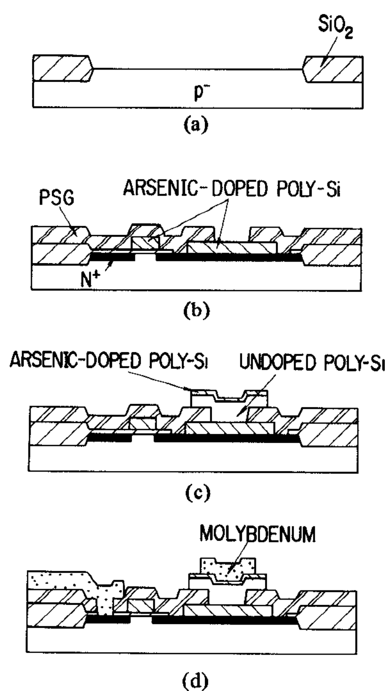

Fig. 1. Schematic diagram of the PROM process. (a) LOCOS oxidation. (b) MOSFET formation. (c) Poly-Si resistor formation. (d) Metallization.

the poly-Si resistor, and stable transition characteristics are obtained.

The PROM fabrication process is simplified by the fact that 1) both the lower electrode of the poly-Si resistor and the gate poly-Si are formed at the same time, 2) arsenic-doped poly-Si for the upper electrode is deposited sequentially after undoped poly-Si deposition, and 3) the undoped poly-Si and the sequentially deposited arsenic-doped poly-Si are patterned at the same time by dry etching technology. Consequently, the number of masks used in the PROM process is only two greater than that in the conventional MOS RAM process.

B. Poly-Si Resistor Fabrication Conditions

It is necessary to reduce the transition voltage and current of the poly-Si resistor and to improve the uniformity of these transition characteristics in order to realize large capacity PROM's. The deposition conditions of undoped poly-Si and the device-size effect on the transition characteristics of a poly-Si resistor were investigated using low-pressure CVD technology. This technology is an excellent deposition technology; for example, deviation of the deposition temperature as small as ±1°C results in a variation of the undoped poly-Si film thickness of ±2 percent. The deposition temperature of undoped poly-Si should be set as low as possible since the transition characteristics are influenced by phosphorus autodoping into undoped poly-Si from PSG during undoped poly-Si deposition.

The temperature dependences of the transition voltage and current of a 0.4 μm thick, 8 μm^2 electrode area, poly-Si resistor are shown in Fig. 2. Both PSG and SiO_2 are used as an intermediate layer to study the influence of phosphorus autodoping. At a deposition temperature of 650°C, the transition current of a poly-Si resistor using PSG is three times larger

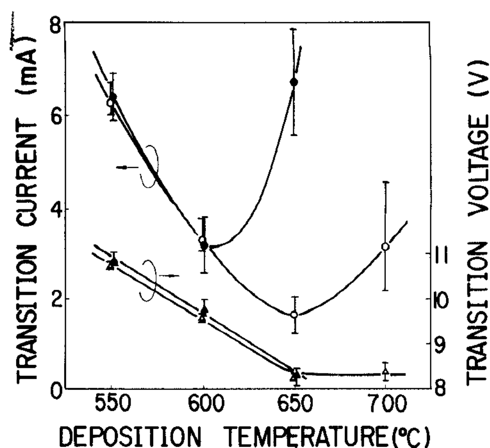

Fig. 2. Deposition temperature dependence of transition voltage and current. (●▲PSG intermediate layer, ○△SiO_2 intermediate layer.)

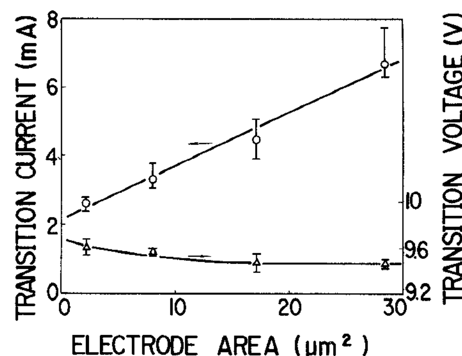

Fig. 3. Electrode area dependence of transition voltage and current.

than that using SiO_2, although the transition voltage is the same for both types of resistors. This means that phosphorus autodoping cannot be neglected above 650°C because the resistivity of poly-Si decreases greatly even with a small amount of impurity [16]. Taking account of this result and the fact that the deposition rate at 550°C is very small, a deposition temperature of 600°C was chosen.

The electrode-area dependence of the transition voltage and current of undoped poly-Si with 0.4 μm thickness, deposited at 600°C, is shown in Fig. 3. The transition current increases with the electrode area but the transition voltage scarcely depends on it. The transition current can be reduced by decreasing the electrode area, while the transition voltage remains constant. However, an electrode area of 8 μm^2 was used, to take into account controllability of the electrode area.

The transition voltage and the reciprocal of the transition current increase with the film thickness, as described in our previous work [16]. When the film thickness of undoped poly-Si is varied from 0.2 to 0.6 μm, the transition voltage increases from 6 to 15 V and the transition current decreases from 6 to 1.5 mA. Since the maximum voltage used in the 4 kbit MOS PROM is 14 V and the voltage applied between the two electrodes of the poly-Si resistor is designed to be less than 10 V, a film thickness of 0.4 μm was chosen.

The uniformity of the transition characteristics is determined mostly by the electrode-area accuracy because the deviations of deposition temperature and film thickness are very small. The deviation of the electrode area is 20 percent of

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8 μm^2, and this gives rise to less than a 5 percent fluctuation of the transition voltage and less than a 20 percent fluctuation of the transition current. These values are small enough to realize MOS PROM's.

C. 4 kbit MOS PROM Fabrication Conditions

The 4 kbit MOS PROM is fabricated on a p-type, (100), 10 $\Omega \cdot$ cm substrate. The MOSFET has a 500 Å thick gate oxide and a 2 μm effective channel length. The diffusion depth of the source and drain is 0.25 μm. The threshold voltage of the MOSFET is 0.45 V when the substrate voltage is 0 V and the drain voltage is 1 V. The film thickness of the arsenic-doped poly-Si used for a lower electrode is 0.45 μm and that for an upper electrode is less than 0.1 μm. The undoped poly-Si for the poly-Si resistor is deposited using an SiH_4-He gas system at 600°C with low-pressure CVD technology, and its film thickness is 0.4 μm. The electrode area (the area of the through-hole in PSG) is 8 μm^2. The transition voltage and current of the poly-Si resistor ranges from 9.5–10 V and 2.5–4 mA, respectively. For interconnection, an evaporated 0.7 μm thick molybdenum film is used. Its sheet resistance is 1 $\Omega/\square$. Ultraviolet photolithography is used with a positive photoresist.

III. Design

A. Dual X-Line Layout

A circuit diagram of the memory cell array and peripheral circuits of a 4 kbit MOS PROM is shown in Fig. 4. Each memory cell is connected to three lines, which are the X-line, V_{PP} line, and bit line. The V_{PP} and bit lines are perpendicular to the X-line. Although only ac current flows in the X-line, a relatively large dc current flows in both the V_{PP} and bit lines during programming. Since two layers of metal are not used in the PROM fabrication process, V_{PP} and bit lines should be metal to minimize the potential drop in them, while the X-line should be poly-Si.

The resistance of the X-line is large owing to the high poly-Si sheet resistance of 50 $\Omega/\square$. Moreover, the X-line capacitance, mainly determined by the gate capacitance of the cell FET's, is also large since a cell FET with large channel width is needed in order to force the programming current. Therefore, the propagation delay along the X-line, determined by X-line resistance and capacitance, becomes large. To realize high-speed read operation, the propagation delay along the X-line formed with poly-Si must be minimized. This problem is circumvented by making the X-line dual and putting a MOSFET on both sides of the poly-Si resistor.

The schematic memory cell layouts for a single and a dual X-line, and their equivalent circuits, are shown in Fig. 5. By adopting a dual X-line, both the resistance and the capacitance of each X-line are reduced to one half because the channel width of each MOSFET for a dual X-line layout is one half of that for a single X-line layout and the length of the X-line is reduced to one half. Therefore, the propagation delay is reduced to a quarter of that along the single X-line. Moreover, dividing a memory cell array into two blocks in the 4 kbit MOS PROM, the propagation delay along the X-line is reduced to 25 ns, and a high-speed read operation is acheived without impairing the PROM programming characteristics.

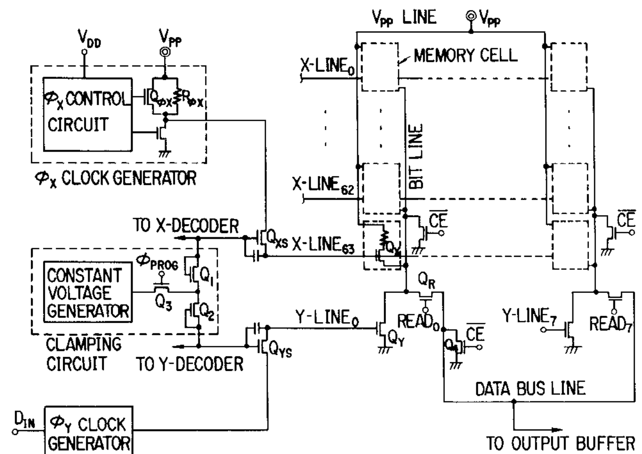

Fig. 4. Memory cell array and peripheral circuits of 4 kbit MOS PROM. (This PROM is organized as 512 words × 8 bits. This figure shows the memory cell array for one bit.)

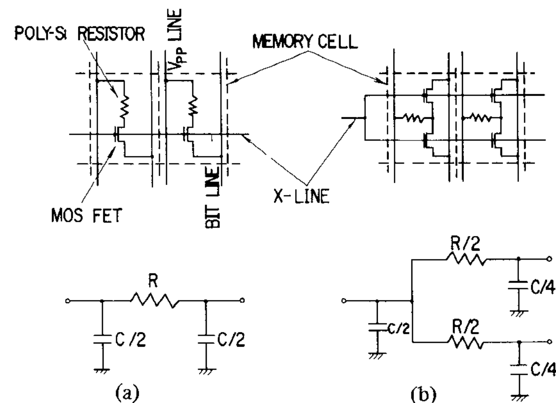

Fig. 5. Memory cell layouts and their equivalent circuits for (a) single X-line, and (b) dual X-line.

This dual X-line layout also results in the reduction of cell size. The cell size is reduced to about 75 percent of that for a single line layout, for the length along the bit line increases 50 percent while the length along the X-line is reduced to about one half.

B. Program Operation

In the programming mode, the potential of the selected X-line rises regardless of the input data, but the potential of the selected Y-line, which is controlled by input data, rises only when the input data is "1." Thus, a cell is selected and the current path from the V_{PP} terminal to ground through the poly-Si resistor Q_X and Q_Y is made. Applying programming voltage to the V_{PP} terminal and forcing a programming current which is larger than the transition current, the resistance of the poly-Si resistor is lowered and an information "1" is programmed in the cell. On the other hand, when the input data is "0," the potential of the selected Y-line is kept at ground level and programming is inhibited. Therefore, the poly-Si resistor remains at the initial highly resistive state.

C. Read Operation

The read operation is performed in the following manner. The potential level of the programming voltage V_{PP} is reduced to that of the supply voltage V_{DD}. A cell is selected by raising

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its X-line and read-line potentials. (The Y-line potential level is kept at ground level in read mode.) Then the potential level of the data bus line, which is initially discharged to ground by MOSFET Q_4, becomes "high" in the rise time determined by the resistance of the poly-Si resistor, g_m's of the MOSFET's (Q_X and Q_R), and the parasitic capacitance of the bit line and the data bus line.

When the "1" information stored in a cell is read out, fast access time can be obtained since the resistance of the poly-Si resistor is as small as 500 Ω and the data bus line potential rises in a short time. When the "0" information is read out, the rise time is much larger than the read cycle time since the resistance of the poly-Si resistor is as high as 10^8 Ω and the data bus line potential remains at ground level.

D. Peripheral Circuits

To realize high-performance PROM's, both low programming voltage and high-speed read operation are required. For this purpose, in the programming mode two high-level internal programming clocks, which drive the X-line and Y-line separately, are required to give high X- and Y-line potentials and to reduce the channel width of a cell MOSFET, or the cell size. In the read mode, a high-speed internal read clock which drives only the X-line is required. Moreover, it is preferable that these programming and read clocks for the X-line are generated by a single circuit. Furthermore, it is also required that the highest voltage level used in the PROM should not exceed the breakdown voltage of the MOSFET's. To meet these requirements, ϕ_X and ϕ_Y clock generators and a clamping circuit have been designed, as shown in Fig. 4.

The ϕ_X clock generator driving the X-line consists of a control circuit and a buffer circuit. The supply voltages for the control and buffer circuits are V_{DD} and V_{PP}, respectively. The load element of the buffer circuit consists of a resistor $R_{\phi X}(= 20\ k\Omega)$ and a MOSFET $Q_{\phi X}$ connected in parallel. The ϕ_Y clock generator driving the Y-line is similar to the ϕ_X clock generator. In the programming mode, the ϕ_X level is raised to the V_{PP} through resistor $R_{\phi X}$. The rise time, which is determined by the resistance of the $R_{\phi X}$ and the capacitance of the X-line, is about 200 ns and is sufficiently small compared with the programming cycle time. In the read mode, a high-speed read clock is obtained through a MOSFET $Q_{\phi X}$, since the gate potential of $Q_{\phi X}$ is raised to a much higher level than V_{DD} by the control circuit.

A clamping circuit, which prevents the internal node potentials from exceeding the breakdown voltage of MOSFET's, is connected to the gate of MOSFET's Q_{XS} and Q_{YS}, which drive the X- and Y-lines, respectively. This circuit consists of MOSFET diodes (Q_1 and Q_2), a switching MOSFET (Q_3), and a constant voltage generator. The output voltage of the constant voltage generator is designed to be $V_{PP} - V_{TH}$. Here, V_{TH} is the threshold voltage of a MOSFET. The internal control signal ϕ_{PROG} is generated by detecting the voltage difference between V_{PP} and V_{DD} as described below.

In the programming mode, V_{PP} is set much higher than V_{DD} and the clamping circuit becomes ready to work. When the bootstrapped gate potential of Q_{XS} begins to exceed V_{PP}, Q_1 turns on and the gate potential is kept at the V_{PP} level. Finally, the potentials of the selected X- and Y-lines increase

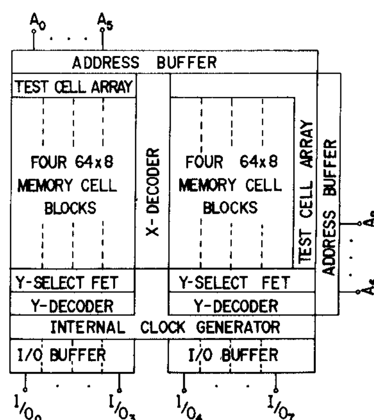

Fig. 6. Block diagram of 4 kbit MOS PROM.

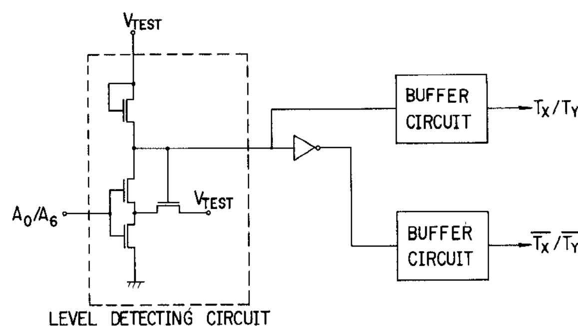

Fig. 7. Test signal generator.

to the level of $V_{PP} - V_{TH}$. In the read mode, V_{PP} is set equal to V_{DD} and ϕ_{PROG} becomes 0 V. MOSFET Q_3 turns off and the constant voltage generator is separated from Q_{XS} and Q_{YS}. Therefore, the clamping circuit ceases to work and the potential of the selected X-line rises freely up to the V_{DD} level.

E. Test Bits

The designed 4 kbit MOS PROM has test cells for testing peripheral circuits and programming characteristics. Fig. 6 shows a block diagram of the 4 kbit MOS PROM. The 260 test cells (two row and two column lines) are located outside of each memory cell array. The test cells of one row and one column line consist of the regular memory cells shown in Fig. 5(b) and memory cells without poly-Si resistors. These two types of test cells are arranged according to a parity-bit pattern, which is useful for detecting multiselecting errors of X- and Y-lines. All the test bits of the other row and column lines consist of regular memory cells for testing the programming characteristics.

The test cell is selected by decoder using either output signal of the two test signal (T_X and T_Y) generators. The test cells along the X- and Y-lines are distinguished from regular cells by T_X and T_Y, respectively. The test signal generator is composed of a level detecting circuit [18], an inverter, and buffer circuits, as shown in Fig. 7. A test signal (V_{TEST}) is adopted and supplied to the level detecting circuit. Address input signals A_0 and A_6 are used as the input signals of the T_X and T_Y generators, respectively. When the functional test of PROM's, using the test cells, is carried out on the wafer, either voltage level of A_0 and A_6 is set at V_{TEST}. When the PROM's are packaged, V_{TEST} is connected to the GND. Therefore, the output

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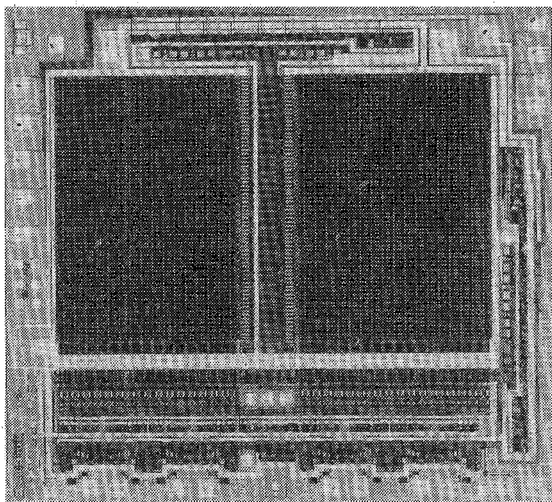


Fig. 8. 4 kbit MOS PROM photomicrograph.

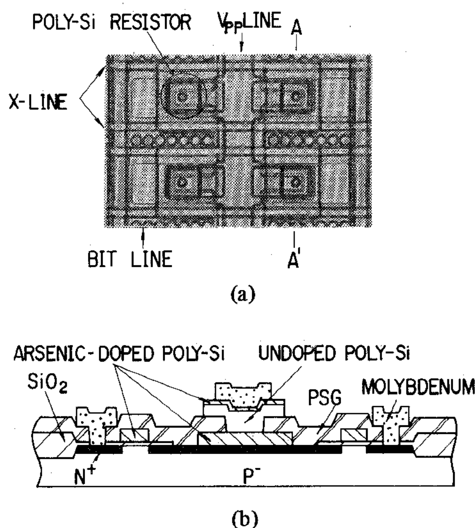


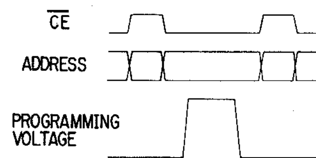
Fig. 9. Memory cell. (a) Photomicrograph (memory cells for 4 bits). (b) Cross-sectional view along A-A' shown in (a) (memory cell for 1 bit).

signals of T_X and T_Y are fixed, and regular cells are always selected.

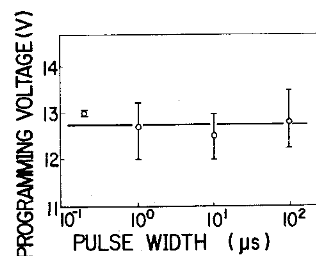
IV. 4 kbit MOS PROM Device Characteristics

A photomicrograph of the fabricated 4 kbit MOS PROM is shown in Fig. 8. The PROM is organized as 512 words × 8 bits. Its chip size is 4.1 × 3.75 mm^2. The top view and the cross-sectional view of the memory cell are shown in Fig. 9. The memory cell size is 29 × 40.75 μm^2.

In the programming mode, a supply voltage V_{DD} of 8 V is used to ensure stable circuit operation, and a substrate voltage V_{BB} of −2 V is used to increase the threshold voltage of parasitic MOSFET's. The PROM is programmed using a programming pulse whose waveform is shown in Fig. 10(a). The programming voltage V_{PP} is independent of the pulse width and is less than 14 V over the wide range of the pulse width, as shown in Fig. 10(b). Using a 1 μm width pulse, this programming operation can be accomplished within 5 μs. This



(a)



(b)

Fig. 10. Programming characteristics. (a) Waveforms. (b) Pulse width dependence of programming voltage.

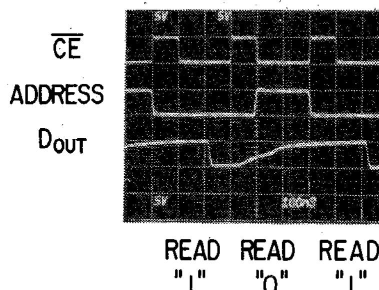


Fig. 11. Operating waveforms.

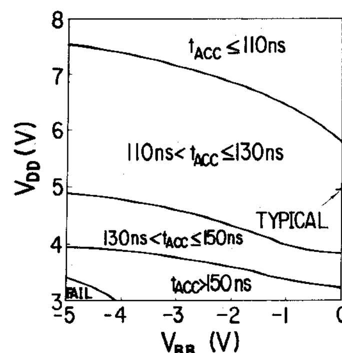


Fig. 12. $V_{DD} - V_{BB}$ shmoo plots.

is 10^3 times shorter than that of the conventional PROM's [1]-[10].

Fig. 11 shows the operating waveforms when the stored information "1" and "0" is sequentially read. Measured access time is less than 130 ns and active power dissipation is 125 mW at 300 ns cycle time under typical dc supply voltage conditions, i.e., $V_{DD} = V_{PP} = 5$ V and $V_{BB} = 0$ V. Standby power is 60 mW. Fig. 12 shows $V_{DD} - V_{BB}$ shmoo plots at 300 ns cycle time. The PROM has a broad operating margin. The temperature dependence of the access time is small; for example, the access time increases only 10 percent when the temperature is raised from 25 to 75°C. The key device characteristics of the fabricated 4 kbit MOS PROM are summarized in Table I.

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TABLE I
4 kbit MOS PROM DEVICE CHARACTERISTICS

Organization	512word x 8bit
Access time	130ns
Cycle time	300ns
Supply voltage	Read : Single 5V
	Program : 8V,-2V
Programming voltage	$<$ 14V
Programming time	$<$ 5μs
Active power	125mW
Standby power	60mW
I/O interface	TTL compatible

V. SUMMARY

A novel fusible-link-type 4 kbit MOS PROM, using a poly-Si resistor as a memory element, has been developed with n-channel silicon-gate technology.

The PROM fabrication process is simplified and the process is compatible with conventional silicon-gate processing. A low-voltage and small-current programmable poly-Si resistor is obtained by optimizing the undoped poly-Si deposition conditions and reducing the electrode area of the poly-Si resistor. Since the transition voltage and current are as small as 10 V and 4 mA, respectively, the programming is easily controlled by MOSFET's. In addition to the development of an excellent memory element, by the use of newly designed circuits, such as a resistor-FET-load clock generator and a voltage-suppressing circuit, a low programming voltage of 14 V is obtained. Moreover, a high-speed read operation is achieved without impairing the PROM programming characteristics by adopting the dual X-line layout. This PROM has 260 test cells, which are selected by applying an address signal larger than the TTL level and a test signal, to test the peripheral circuits and the programming characteristics.

The fabricated 4 kbit PROM can be programmed within 5 μs by applying a voltage less than 14 V. Measured access time is less than 130 ns and active power dissipation is 125 mW at 300 ns cycle time under single 5 V supply condition.

This PROM is a high-performance MOS PROM itself, and the programmable resistor is an excellent candidate for on-chip programmable devices in VLSI's for logic and fault-tolerant RAM's.

ACKNOWLEDGMENT

The authors wish to thank Dr. S. Ōhara, Dr. H. Yoshimura, Dr. T. Asaoka, M. Kondo, and Dr. H. Katsuraki for supporting this work. They also wish to thank H. Asakawa and the staffs of the Semiconductor Memory Technology Section and Mask Pattern Generation Section at the Musashino Electrical Communication Laboratory for their support with the device fabrication. They are also grateful to the staff of the Semiconductor Memory Design Section for their useful discussions.

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