An 80-Gb/s optoelectronic delayed flip-flop IC using resonant tunneling diodes and uni-traveling-carrier photodiode

doi: 10.1109/4.902769

An 80-Gb/s Optoelectronic Delayed Flip-Flop IC Using Resonant Tunneling Diodes and Uni-Traveling-Carrier Photodiode

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***Abstract*—This paper describes an 80-Gb/s optoelectronic delayed flip-flop (D-FF) IC that uses resonant tunneling diodes (RTDs) and a uni-traveling-carrier photodiode (UTC-PD). A circuit design that considers the ac currents passing through RTDs and UTC-PD is key to boosting circuit operation speed. A monolithically fabricated IC operated at 80 Gb/s with a low power dissipation of 7.68 mW. The operation speed of 80 Gb/s is the highest among all reported flip-flops. To clarify the maximum operation speed, we analyze the factors limiting circuit speed. Although the bandwidth of UTC-PD limits the maximum speed of operation to 80 Gb/s at present, the circuit has the potential to offer 100-Gb/s-class operation.**

***Index Terms*—Flip-flop, optical communications, optoelectronic integrated circuit (OEIC), resonant tunneling diode, uni-traveling-carrier photodiode.**

I. Introduction

LARGE-capacity optical network systems are required to provide various multimedia services. 10-Gb/s electrical time-division multiplexing (ETDM) systems have already been commercialized [1], and 40-Gb/s ETDM systems are being developed [2]. In ETDM systems, an electrical delayed flip-flop (D-FF) is a key component for realizing regenerative function. Up to now, 40-Gb/s D-FFs that use AlGaAs/GaAs heterojunction bipolar transistors (HBTs) [3], InP high electron mobility transistors (HEMTs) [4], [5], GaAs metal-semiconductor field-effect transistors (MESFETs) [6], and InP/InGaAs HBTs [7] have been reported. To significantly increase D-FF operation speed, there are several problems we have to overcome. The first is transistor speed limit. It is empirically known that a master–slave-type D-FF operates at 25% of the current gain cut-off frequency (f_T) in the case of FETs [8]. This implies that 100-Gb/s-class D-FFs need transistors with 400-GHz f_T which seems to be challenging. The second is the D-FF feedback circuit configuration. Since the feedback transmission delay becomes dominant in ultrafast operation [9], shortening the intrinsic gate delay is less effective in improving operation speed. The third problem is the bandwidth in the electrical interconnection. Power loss at over 40 GHz is severe for the interconnection between chips. The fourth is the large power consumption of D-FFs, reaching into hundreds of milliwatts. This is a severe handicap when developing more integrated functional circuits such as one-chip clock and data recovery circuits.

To realize an over-40-Gb/s D-FF IC, we proposed a novel optoelectronic D-FF IC that uses only two resonant tunneling diodes (RTDs) and a uni-traveling-carrier photodiode (UTC-PD) [10]. Since RTDs can switch in a few picoseconds [11], [12] and form a no-feedback D-FF with only two RTDs, they are suitable for realizing an ultrafast D-FF with low power consumption. The UTC-PD converts optical signals into electrical signals with fast response and sufficient power even at low bias voltages [13]. As a result, it can offer an optical interface for the IC without an electrical wide-bandwidth amplifier. A fabricated IC exhibited not only 40-Gb/s D-FF operation, but also 80-to-40-Gb/s demultiplexing operation with less than 10-mW power consumption [14]. High-speed D-FF operation at more than 40-Gb/s, however, was not achieved by the IC.

This paper describes an 80-Gb/s optoelectronic D-FF IC using RTDs and a UTC-PD. The IC design takes account of the ac currents passing through the RTDs and the UTC-PD. We reveal that this circuit design improves circuit speed performance. A new IC was fabricated using the same process used for the previous IC [10], [14], and it was confirmed to operate at 80 Gb/s with 7.68-mW dissipation. In order to clarify the factors restricting circuit operation speed, we analytically investigate circuit performance. Although the speed limit of the fabricated IC seems to be 80 Gb/s due to the bandwidth of the fabricated UTC-PD, it is shown that the IC has the potential for 100-Gb/s-class operation.

The next section describes the circuit configuration, operation principle, and design for ultrafast operation. Section III introduces a process technology that integrates RTD and UTC-PD monolithically, the measurement setup for assessing 80-Gb/s D-FF operation, and the performance of the fabricated IC. Section IV discusses the maximum operation speed by analyzing the factors limiting speed.

II. Circuit Design

A. Circuit Configuration and Operation Principle

Fig. 1 shows a circuit diagram of the optoelectronic delayed flip-flop IC. The IC consists of just two RTDs (the lower one is the driver and the upper one is the load) and one UTC-PD.

Manuscript received March 3, 2000; revised September 5, 2000.

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Publisher Item Identifier S 0018-9200(01)00934-9.

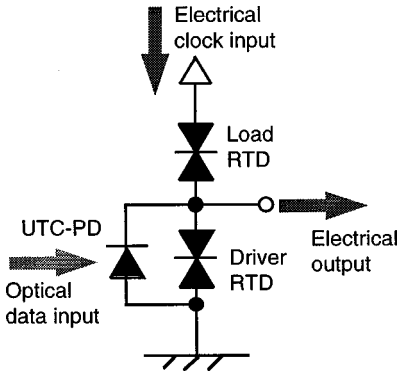

Fig. 1. Circuit diagram of the optoelectronic delayed flip-flop IC.

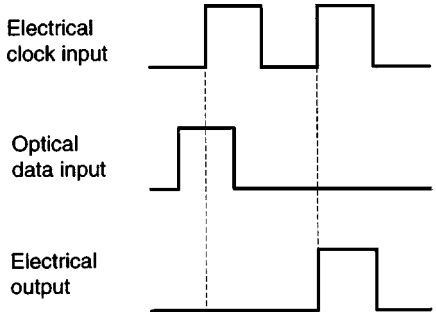

Fig. 2. Time chart of the input/output signals for the D-FF IC.

A circuit consisting of an RTD pair and one current modulator is known as a monostable-bistable transition logic element (MOBILE) [15]. To realize an optical interface, we employ the UTC-PD as the current modulator. The UTC-PD is connected in parallel to the driver RTD in order to obtain sufficient logic swing [10].

Fig. 2 shows a time chart of the input/output signals for the IC. Here, the high level (low level) in the optical signal means illumination (no illumination) of the optical signal. When the clock signal is at a low level, the IC is in the monostable state, where there is only one stable point, as shown in Fig. 3(a) and (b). Thus, no matter which optical signal is present, the output voltage level is low corresponding to the stable point. When the clock switches to a high level, the IC moves from the monostable to the bistable state which has two possible stable points [Fig. 3(c) and (d)]. The stable point is determined by the relationship between the magnitude of the peak current of the driver RTD ($I_{\rm DP}$) and that of the load RTD ($I_{\rm LP}$) at the rising edge of the clock. Here, the photocurrent through UTC-PD ($I_{\rm photo}$) can effectively control the relationship between $I_{\rm DP}$ and $I_{\rm LP}$. If $I_{\rm DP} < I_{\rm LP}(I_{\rm DP} + I_{\rm photo} > I_{\rm LP})$, the stable point becomes S2 (S1) of the high-(low-)voltage output. Therefore, the no-illumination and illumination conditions at the rising edge of the clock lead to high- and low-level output voltages, respectively. The output voltage is held until the clock returns to a low level [15]. These operations are regarded as those of a D-FF that outputs a return-to-zero (RZ) signal.

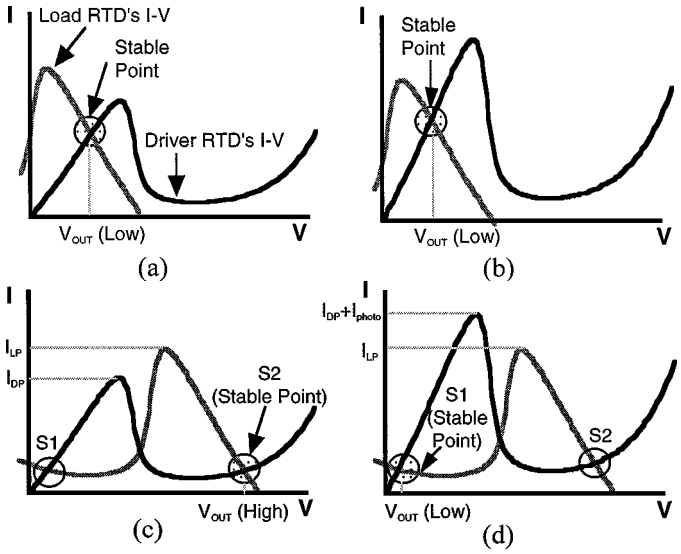

Fig. 3. Operation principle of the D-FF IC. (a) Unilluminated and low-level clock (monostable state). (b) Illuminated and low-level clock (monostable state). (c) Unilluminated and high-level clock (bistable state). (d) Illuminated and high-level clock (bistable state).

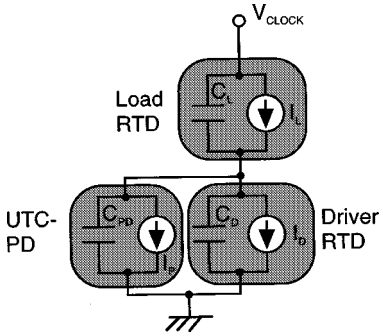

Fig. 4. Simplified equivalent circuit of the D-FF IC.

B. Design for Ultrafast Operation

The RTDs' peak-current relationship is very important for IC operation. The IC must be designed to emulate the following equation for correct circuit operation.

$$I_{\rm DP} < I_{LP} \tag{1}$$

$$I_{\rm DP} + I_{\rm photo} > I_{\rm LP}. \tag{2}$$

In the high-frequency region, we need to consider the ac currents through the capacitance of RTD and UTC-PD because they are as large as $I_{\rm DP}$, $I_{\rm LP}$, and $I_{\rm photo}$. Fig. 4 shows the simplified equivalent circuit of the IC. Since the load RTDs capacitance $C_{\rm L}$ is in parallel to the current source, which represents the load RTDs dc current–voltage characteristics, the ac current $dC_{\rm L}V_{\rm L}/dt$ should be added to $I_{\rm LP}$ in (1) and (2), where $V_{\rm L}$ is the voltage applied to $C_{\rm L}$. Similarly, $d(C_{\rm D}+C_{\rm PD})V_{\rm D}/dt$ must be added to $I_{\rm DP}$, where $V_{\rm D}$ is the voltage applied to $C_{\rm D}$ and $C_{\rm PD}$. The current relationships considering the ac current are rewritten as

$$I_{\rm DP}+d(C_{\rm D}+C_{\rm PD})V_{\rm D}/dt < I_{LP}+dC_{\rm L}V_{\rm L}/dt \tag{3}$$

$$I_{\rm DP}+d(C_{\rm D}+C_{\rm PD})V_{\rm D}/dt + I_{\rm photo} > I_{LP}+dC_{\rm L}V_{\rm L}/dt. \tag{4}$$

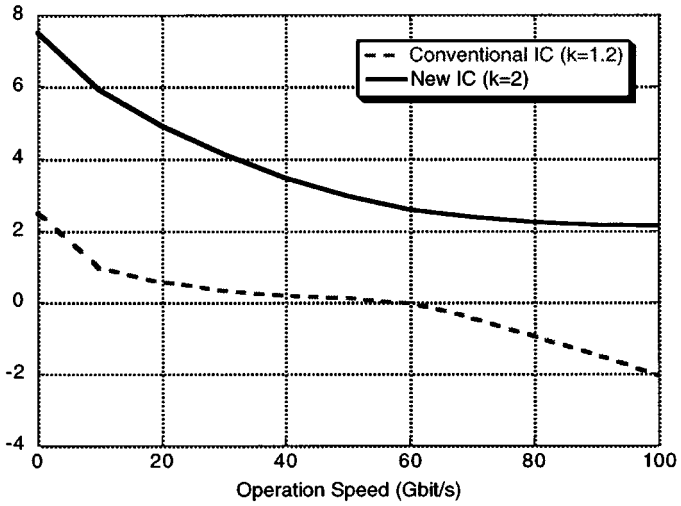

Fig. 5. Simulated dependency of $\Delta I_{\rm P}$ on the operation speed.

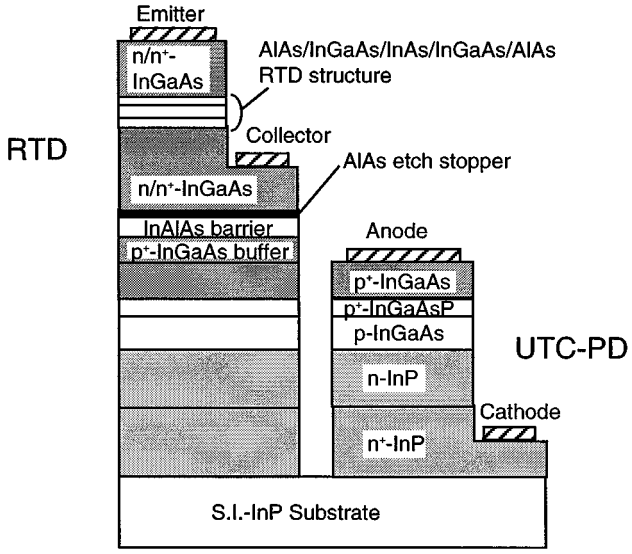

Fig. 6. Schematic cross-sectional view of the monolithically integrated RTD and UTC-PD.

Here, we define a factor k, which is the ratio of the load RTD's emitter area to the driver RTDs emitter area, and $\Delta I_{\rm P} \equiv (I_{LP} + dC_{\rm L}V_{\rm L}/dt) - (I_{\rm DP} + d(C_{\rm D} + C_{\rm PD})V_{\rm D}/dt) = (k-1)I_{\rm DP} + kdC_{\rm D}V_{\rm L}/dt - d(C_{\rm D} + C_{\rm PD})V_{\rm D}/dt$. Equations (3) and (4) can be rewritten as

$$0 < \Delta I_{\rm P} < I_{\rm photo}. \tag{5}$$

$\Delta I_{\rm P}$ varies with the operation speed because it includes time differential terms. Fig. 5 shows the dependency of $\Delta I_{\rm P}$ on the operation speed as simulated by SPICE. In the simulation, the bandwidth of the current source in the UTC-PD is assumed to be infinite. The dashed line plots $\Delta I_{\rm P}$ for the previous IC [14], and the solid line is for the newly designed IC of this paper. For the previous IC, which was designed with $k = 1.2$, $\Delta I_{\rm P}$ becomes negative at over 60 Gb/s due to the ac current through the capacitance of the driver RTD and UTC-PD. This ac current effect seems to be the main reason why we could not achieve an over-40-Gb/s D-FF. For the new IC, in order to satisfy (5) at more than 60 Gb/s, we set $k = 2.0$ by reducing the size of the driver RTD. As a result, $\Delta I_{\rm P}$ is more than 0 and satisfies (5) even at 100 Gb/s.

III. Experiment

A. Process Technology

The new IC was fabricated using the same process used for the previous IC [16]. Fig. 6 shows a schematic cross-sectional view of the monolithically integrated RTD and UTC-PD. The UTC-PD layers were grown on an InP substrate by the MOCVD method. The p^+-InGaAs buffer layer, the InAlAs barrier layer, the AlAs etch-stopper layer, and the RTD layer were regrown on the UTC-PD layers by the molecular-beam etching (MBE) method [17]. In the device and electrode formation, conventional wet-etching and lift-off processes were used. The chip size was 0.43 mm $\times$ 0.37 mm. Fig. 7 shows a microphotograph of the chip. The device parameters are summarized in Table I.

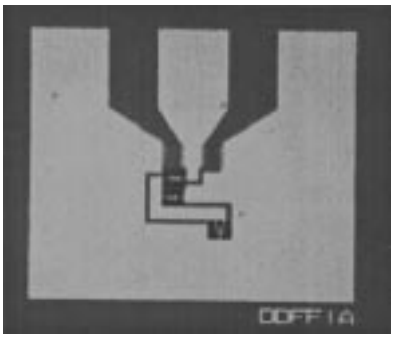

Fig. 7. Microphotograph of the chip.

TABLE I
RTD and UTC-PD Parameters Obtained in the Process for the IC

RTD		UTC-PD	
Parameters	Values	Parameters	Values
V_P	350 mV	C_{PD}	0.91 x size(μm²) fF
V_V	700 mV		
I_{DP}	1.25 x size(μm²) mA	dark resistance	>1 MΩ
I_{DV}	0.12 x size(μm²) mA		
R_{D6}	4530 / size(μm²) Ω	sensitivity	0.26 A/W
C_D	6.77 x size(μm²) fF	3-dB bandwidth	80 GHz

For the fabricated IC
RTD size : 6 μm²
UTC-PD size: 24.6 μm²

B. Measurement Setup

Fig. 8 shows the measurement setup used to assess the 80-Gb/s D-FF operation. Because of the lack of a more than 80-GHz clock source, 80 Gb/s is the upper limit of the setup at present. The IC was tested on a wafer. Electro-optic sampling (EOS) [18] was used to monitor the input and output signals. An 80-GHz clock signal was generated from a 20-GHz signal by using a frequency quadruplexer and then fed to the IC

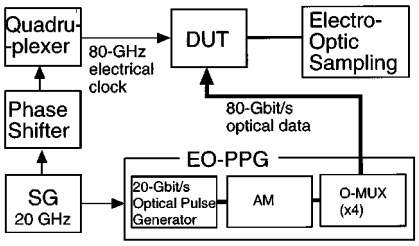

Fig. 8. Measurement setup for 80-Gb/s D-FF operation.

through a waveguide tube and a waveguide-type RF probe. To allow measurement of the phase margin of the D-FF IC, a phase shifter was inserted between the signal source (SG) and the quadruplexer in order to shift the phase of the clock. The clock signal has the voltage amplitude of 1 V_{p-p} with +0.5-V offset. An 80-Gb/s optical data signal was generated by an electro-optic pulse pattern generator (EO-PPG) [19]. A repetition of the pattern "10 110 100" (1 : mark, 0 : space) was used since EOS systems cannot measure eye patterns. The optical signal, which had an RZ shape with about 5-ps pulsewidth, illuminated the UTC-PD from the backside of the wafer. The optical input signal was monitored at the output node of the IC by biasing the clock-input node to ground level.

C. Circuit Performance

Fig. 9 shows the observed waveforms of the 80-Gb/s input signal and the output signal of the D-FF IC. The 80-Gb/s optical input signal "10110100," in which the peak intensity of each bit "1" differed, was successfully inverted and regenerated. The power dissipation was extremely low at 7.68 mW, which was as small as that of the 40-Gb/s D-FF operation (7.00 mW) [10]. The peak photocurrent estimated from the measured average photocurrent was 4.65 mA. Although this value is smaller than $\Delta I_{\rm P}$ at dc (7.2 mA, Fig. 5, new IC), it is sufficiently larger than $\Delta I_{\rm P}$ at 80 Gb/s (about 2 mA, Fig. 5, new IC), which includes the ac currents passing through the RTDs and UTC-PD. This indicates that the circuit design must consider the ac current not only for ultrafast operation, but also for estimating the minimum photocurrent for D-FF operation. In order to confirm retiming capability, we observed the output waveforms while shifting the phase of the clock signal (Fig. 10). As the phase of the clock was delayed, the output waveform gradually collapsed, and then returned to correct D-FF operation at 360°. This indicates that the circuit is not simply passing through the input data but is indeed realizing retiming. The phase margin of this IC at 80 Gb/s seems to be less than 120°.

IV. Discussion

We achieved 80-Gb/s D-FF operation by adopting a circuit design that considered ac current. The upper limit of the operation speed remains unclear because of the lack of an over-80-Gb/s measurement system. In this section, we discuss the upper speed of the IC by independently analyzing the factors restricting the speed, the ac current effect, the switching delay time, and the bandwidth of the UTC-PD.

A. AC Current Effect

The ac current effect described in Section II-B was the major reason why the previous IC could not achieve over-40-Gb/s D-FF operation. In this section, we analytically introduce the speed limit due to the ac current effect. Here, the equivalent circuit shown in Fig. 11(a) is assumed. Definitions of the variables used are as follows:

- k ratio of the load RTD's emitter area to the driver RTD's emitter area;
- $V_{\rm clock}$ voltage of clock signal;
- $V_{\rm L}$ bias voltage for the load RTD;
- $V_{\rm D}$ bias voltage for the driver RTD and the UTC-PD;
- $V_{\rm P}$ driver/load RTD's peak voltage;
- $I_{\rm DP}$ driver RTD's peak current;
- $C_{\rm D}$ driver RTD's capacitance;
- $C_{\rm PD}$ UTC-PD's capacitance.

The following conditions are assumed in the derivation of the analytical expression.

1) The bias voltages for the RTDs are inversely proportional to their sizes, that is, $V_{\rm L}$ and $V_{\rm D}$ are given by $V_{\rm clock} \times 1/(k+1)$ and $V_{\rm clock} \times k/(k+1)$, respectively.
2) $V_{\rm clock}(t)$ is assumed to be a sinusoidal waveform with 1-V_{p-p} amplitude and offset of +0.5 V, as shown in Fig. 11(b). Therefore
$$V_{\rm clock} = 0.5 \sin\left(2\pi f t - \frac{\pi}{2}\right) + 0.5. \tag{6}$$
Here, f is the frequency of the clock, which is equal to the operation speed.
3) With regard to the operation principle, (5) in Section II-B must be kept at the time when $V_{\rm D} = V_{\rm P}$.

With these assumptions, we calculated $\Delta I_{\rm P} = (k-1)I_{\rm DP} + kdC_{\rm D}V_{\rm L}/dt - d(C_{\rm D} + C_{\rm PD})V_{\rm D}/dt$ in (5) at the time when $V_{\rm D} = V_{\rm P}$.

The time when $V_{\rm D} = V_{\rm P}$, t_o, is given by

$$t_0 = \frac{1}{2\pi f} \sin^{-1}\left(\frac{k+1}{0.5k} V_{\rm P} - 1\right) + \frac{1}{4f}. \tag{7}$$

Derivatives of $V_{\rm D}$ and $V_{\rm L}$ at t_o are

$$\frac{dV_{\rm D}}{dt}_{t=to} = \frac{k\pi f}{k+1} \cos\left\{\sin^{-1}\left(\frac{k+1}{0.5k} V_{\rm P} - 1\right)\right\} \tag{8}$$

$$\frac{dV_{\rm L}}{dt}_{t=to} = \frac{\pi f}{k+1} \cos\left\{\sin^{-1}\left(\frac{k+1}{0.5k} V_{\rm P} - 1\right)\right\}. \tag{9}$$

Using (7)–(9), $\Delta I_{\rm P}$ at t_o becomes

$$\Delta I_{\rm P} = (k-1)I_{\rm DP} - C_{\rm PD}\frac{k\pi f}{k+1} \cdot \cos\left\{\sin^{-1}\left(\frac{k+1}{0.5k} V_{\rm P} - 1\right)\right\}. \tag{10}$$

The maximum operating speed ($f_1^{\rm limit}$) is defined by $\Delta I_{\rm P} = 0$, and is given by

$$f_1^{\rm limit} = \frac{(k+1)(k-1)I_{\rm DP}}{k\pi \cos\left\{\sin^{-1}\left(\frac{k+1}{0.5k} V_{\rm P} - 1\right)\right\} \cdot C_{\rm PD}}. \tag{11}$$

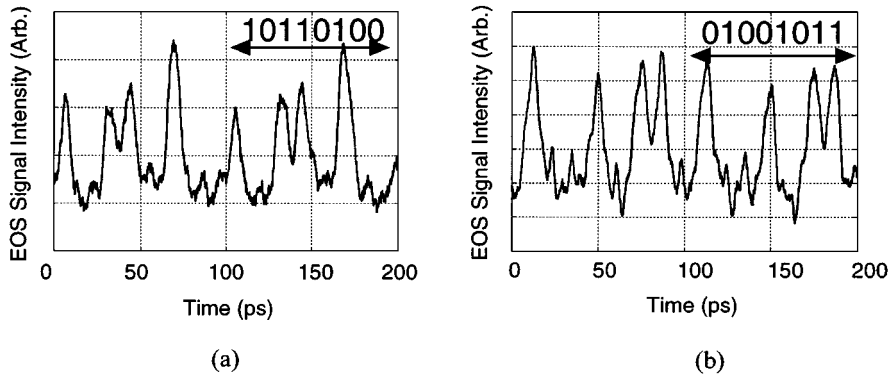

Fig. 9. Observed waveforms of the 80 Gb/s input/output signals of the D-FF IC. (a) Input. (b) Output.

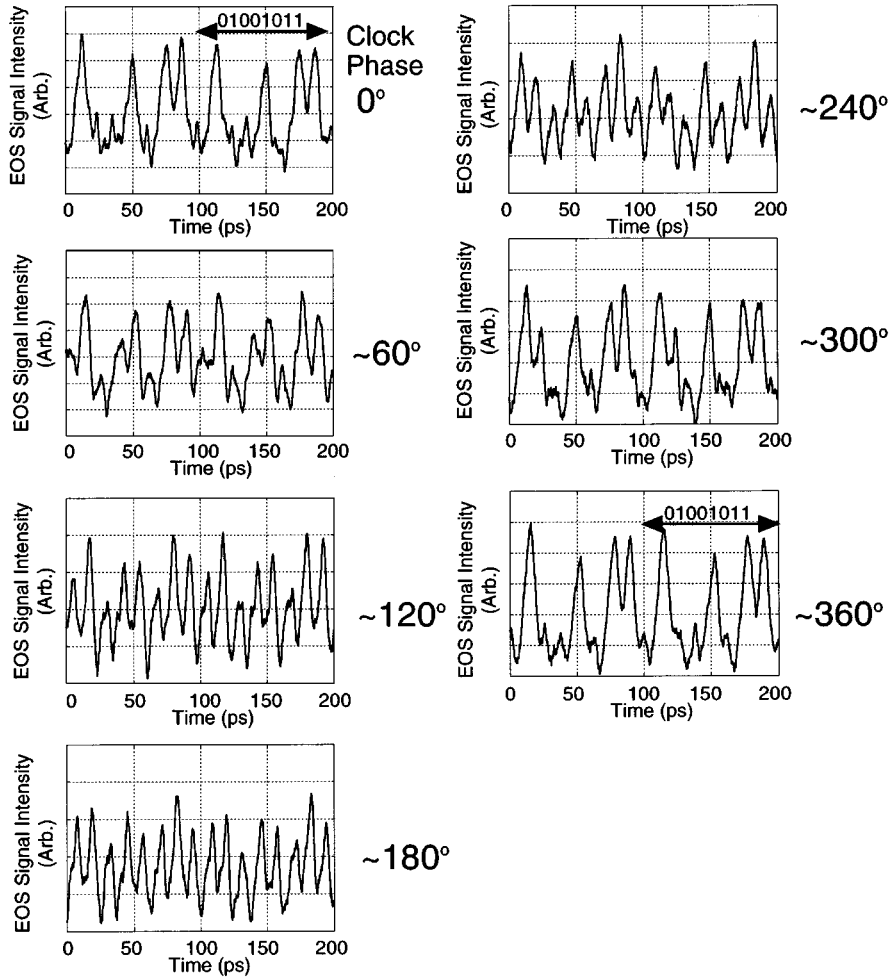

Fig. 10. Output waveform variation with clock phase shifting.

B. Switching Delay Time

The switching delay time is a crucial factor restricting operation speed in any digital circuit. Here, we analyze the delay time in switching from a low level (0 V) to a high level ($V_{\rm H}$), and derive the limit speed by this delay time.

The equivalent circuit shown in Fig. 11(a) is also assumed in this analysis. Voltage-current characteristics in RTD current sources are approximated as piecewise-linear RTD I–V curves, as shown in Fig. 12(a). Here, the following parameters are defined:

$V_{\rm v}$ driver/Load RTD's valley voltage;
$I_{\rm DV}$ driver RTD's valley current;
$R_{\rm Db}$ driver RTD's resistance at over valley voltage ($V>V_{\rm v}$).

Input clock voltage $V_{\rm clock}$ is equal to $V_{\rm v}+V_{\rm P}$. The delay time is analyzed by dividing the voltage region into 1) $0 \sim V_{\rm P}$ (RTD's peak voltage) and 2) $V_{\rm P} \sim V_{\rm H}$.

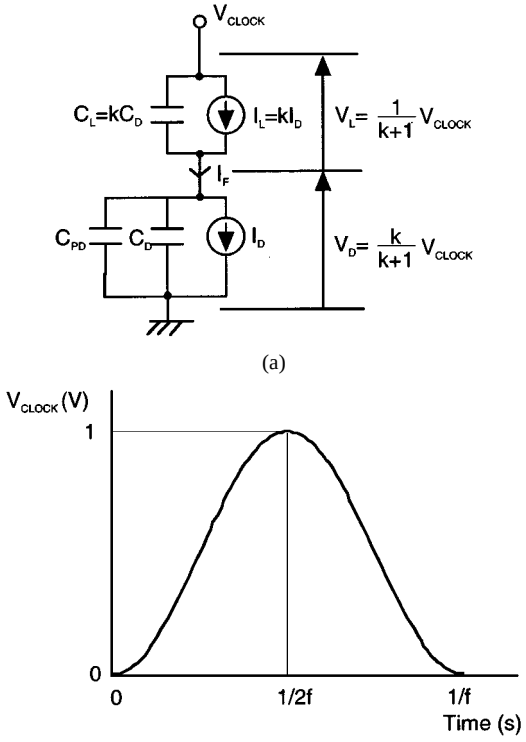

Fig. 11. Figures for calculating the speed limited by the ac current effect. (a) Equivalent circuit. (b) Clock signal waveform.

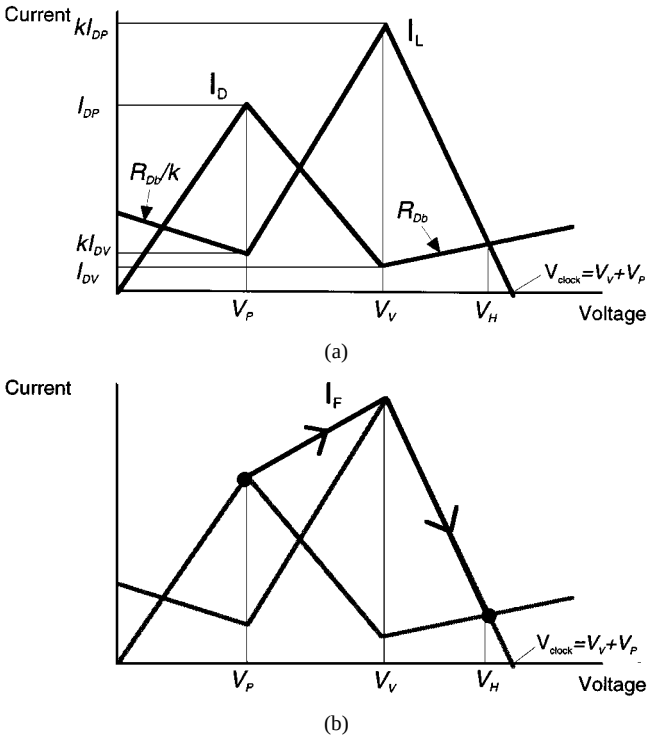

Fig. 12. Figures for calculating the switching delay time. (a) RTD I–V approximated as piecewise linear lines. (b) Variation of the current flowing into driver RTD ($I_{\rm F}$) with voltage.

1) Delay in switching from 0 to $V_{\rm P}$.

Delay in switching from 0 to $V_{\rm P}$ is calculated based on a small-signal transfer function from the clock input into the IC output. In this voltage region, both driver and load RTDs have positive resistance. The current source of the driver (load) RTD is represented by the resistance of $V_{\rm P}/I_{\rm DP}(V_{\rm P}/kI_{\rm DP})$. The transfer function from the clock input to the IC output is written as follows:

$$A(s)=\frac{kV_{\rm P}(I_{\rm DP}+sC_{\rm D}V_{\rm P})}{(k+1)V_{\rm P}I_{\rm DP}+sV_{\rm P}^2\{(k+1)C_{\rm D}+C_{\rm PD}\}}. \quad (12)$$

Using the method of Ashar [20], the delay time switching from 0 V to $V_{\rm P}(\tau_1)$ is given by

$$\tau_1=\frac{-\dfrac{dA(s)}{ds}}{A(s)}_{s=0}=\frac{1}{k+1}\,C_{\rm PD}\,\frac{V_{\rm DP}}{I_{\rm DP}}. \quad (13)$$

2) Delay in switching from $V_{\rm P}$ to $V_{\rm H}$

Delay in switching from $V_{\rm P}$ to the high level ($V_{\rm H}$) is calculated as 10%–90% time of charging $C_{\rm D}$ and $C_{\rm PD}$ [21]. In this voltage region, the current flowing into the driver RTD ($I_{\rm F}$) varies with voltage, as shown in Fig. 12(b).

The delay (τ_2) is equal to the 10%–90% charging time of $C_{\rm D}$ and $C_{\rm PD}$

$$\tau_2=\int_{V_{\rm P}+0.1(V_{\rm H}-V_{\rm P})}^{V_{\rm H}-0.1(V_{\rm H}-V_{\rm P})}\frac{C_{\rm D}+C_{\rm PD}}{I_{\rm F}(V)-I_{\rm D}(V)}\,dV. \quad (14)$$

Here, $I_{\rm F}$ and $I_{\rm D}$ are functions of voltage V

$$I_{\rm F}(V)=\frac{(k-1)I_{\rm DP}}{V_{\rm V}-V_{\rm P}}(V-V_{\rm P})+I_{\rm DP} \quad \text{for } V_{\rm P}\le V\le V_{\rm V}$$
$$=-\frac{kI_{\rm DP}}{V_{\rm P}}(V-V_{\rm P}-V_{\rm V}) \quad \text{for } V_{\rm P}\le V\le V_{\rm H} \quad (15)$$

$$I_{\rm D}(V)=-\frac{I_{\rm DP}-I_{\rm DV}}{V_{\rm V}-V_{\rm P}}(V-V_{\rm P})+I_{\rm DP} \quad \text{for } V_{\rm P}\le V\le V_{\rm V}$$
$$=-\frac{1}{R_{\rm Db}}(V-V_{\rm V})+I_{\rm DV} \quad \text{for } V_{\rm P}\le V\le V_{\rm H}. \quad (16)$$

$V_{\rm H}$ can be calculated from (15) and (16) since it is the crosspoint of the lines formed by (15) and (16)

$$V_{\rm H}=V_{\rm V}+\frac{kR_{\rm Db}I_{\rm DP}-R_{\rm Db}I_{\rm DV}}{V_{\rm P}+kR_{\rm Db}I_{\rm DP}}\,V_P. \quad (17)$$

Equations (14)–(17) give τ_2 as shown in (18), at the bottom of the next page. Total delay time (τ) is the sum of the delays calculated in 1) and 2). Therefore, the total delay (τ) becomes as shown in (19), at the bottom of the next page. τ expresses the switching time from the low level to the high level of the IC. Hence, the limit speed $f_2^{\rm limit}$ is given by

$$f_2^{\rm limit}=\frac{1}{2\tau}. \quad (20)$$

C. Bandwidth of UTC-PD

The bandwidth of the UTC-PD in our IC is defined as the bandwidth in converting from the optical signal to the

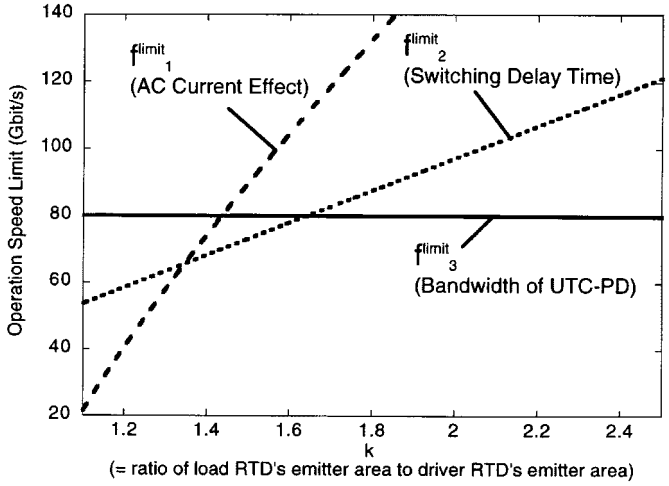

Fig. 13. Each limiting factor ($f_1^{\rm limit}$, $f_2^{\rm limit}$, and $f_3^{\rm limit}$) calculated while varying design parameter k (ratio of load RTD's emitter area to driver RTD's emitter area).

electrical current signal (bandwidth of O/EC) because the UTC-PD is used as the current modulator in our IC. However, the measured bandwidths of photodiodes are generally taken as the bandwidth in converting from an optical signal to an electrical voltage signal (bandwidth of O/EV). Hence, we need to take care when discussing the bandwidth of O/EC. Under the condition that the measured bandwidth of O/EV is not limited by the CR-time constant (here, C and R are the photodiode's capacitance and load resistance, respectively), the bandwidth of O/EC becomes identical to the measured bandwidth of O/EV. The measured bandwidth of the UTC-PD fabricated by the same process used for the IC was found to be 80 GHz [16]. Since the bandwidth limited by the CR-time constant was set to 350 GHz in this measurement ($C = 18.2$ fF, $R = 25\ \Omega$), the bandwidth of O/EC is also 80 GHz for the UTC-PD in our IC. Therefore, the maximum speed limited by the UTC-PD bandwidth in our IC ($f_3^{\rm limit}$) becomes 80 Gb/s when RZ pulses are used for input signals.

We calculated each limiting factor, that is $f_1^{\rm limit}$, $f_2^{\rm limit}$, and $f_3^{\rm limit}$, while varying the design parameter k (ratio of load RTD's emitter area to driver RTD's emitter area). Fig. 13 shows the results of the calculations. The calculations used the RTD and UTC-PD parameters, summarized in Table I, in order to verify the 80-Gb/s D-FF IC in this work. When $k < 1.35$, the ac current effect limits the IC speed. From $k = 1.35$ to 1.6, the maximum speed is determined by the switching delay time. When $k > 1.6$, the UTC-PD bandwidth restricts the operation speed. The speed limit of the IC in this work ($k = 2$) is restricted by the bandwidth of the UTC-PD to 80 Gb/s. However, we can expand the speed limit by using the reported UTC-PD whose bandwidth is 210 GHz and keeping the high saturation power of 0.2 V_{p-p} (under 25 Ω, corresponding to 8-mA output) [22]. In this case, the speed limit is around 100 Gb/s, which is restricted by the switching delay time.

V. Conclusion

An 80-Gb/s optoelectronic D-FF IC using RTDs and UTC-PD has been presented. The IC was newly designed by considering the ac currents flowing through the RTDs and the UTC-PD. The monolithically fabricated circuit successfully exhibited 80-Gb/s D-FF operation and retiming capability with an extremely low power consumption of 7.68 mW. 80-Gb/s flip-flop operation is the fastest ever reported. Furthermore, we discussed the maximum operating speed of the IC by analyzing the three factors that limit speed: the ac current flowing through the RTDs and the UTC-PD, the switching delay time, and the bandwidth of the UTC-PD. Analysis indicated that, while the bandwidth of the fabricated UTC-PD restricts the speed at present, the IC has the potential to operate at 100 Gb/s.

Acknowledgment

The authors would like to thank K. Sato, K. Yamasaki, Y. Ishii, M. Yamamoto, and T. Ishibashi for their continual encouragement during this work. They would also like to thank

$$\tau_2 = \frac{C_{\rm D}+C_{\rm PD}}{\dfrac{(k-1)I_{\rm DP}}{V_{\rm V}-V_{\rm P}}+\dfrac{I_{\rm DP}-I_{\rm DV}}{V_{\rm V}-V_{\rm P}}}\log\frac{10(V_{\rm V}-V_{\rm P})}{V_{\rm V}-\dfrac{R_{\rm Db}I_{\rm DV}+V_{\rm P}}{V_{\rm P}+kR_{\rm Db}I_{\rm DP}}V_{\rm P}}+\frac{C_{\rm D}+C_{\rm PD}}{k\dfrac{I_{\rm DP}}{V_{\rm P}}+\dfrac{1}{R_{\rm Db}}} \cdot\log\frac{10(kI_{\rm DP}-I_{\rm DV})}{\left(V_{\rm V}-\dfrac{R_{\rm Db}I_{\rm DV}+V_{\rm P}}{V_{\rm P}+kR_{\rm Db}I_{\rm DP}}V_{\rm P}\right)\left(k\dfrac{I_{\rm DP}}{V_{\rm P}}+\dfrac{1}{R_{\rm Db}}\right)} \tag{18}$$

$$\tau = \tau_1+\tau_2 = \frac{1}{k+1}C_{\rm PD}\frac{V_{\rm DP}}{I_{\rm DP}}+\frac{C_{\rm D}+C_{\rm PD}}{\dfrac{(k-1)I_{\rm DP}}{V_{\rm V}-V_{\rm P}}+\dfrac{I_{\rm DP}-I_{\rm DV}}{V_{\rm V}-V_{\rm P}}}\log\frac{10(V_{\rm V}-V_{\rm P})}{V_{\rm V}-\dfrac{R_{\rm Db}I_{\rm DV}+V_{\rm P}}{V_{\rm P}+kR_{\rm Db}I_{\rm DP}}V_{\rm P}} +\frac{C_{\rm D}+C_{\rm PD}}{k\dfrac{I_{\rm DP}}{V_{\rm P}}+\dfrac{1}{R_{\rm Db}}}\log\frac{10(kI_{\rm DP}-I_{\rm DV})}{\left(V_{\rm V}-\dfrac{R_{\rm Db}I_{\rm DV}+V_{\rm P}}{V_{\rm P}+kR_{\rm Db}I_{\rm DP}}V_{\rm P}\right)\left(k\dfrac{I_{\rm DP}}{V_{\rm P}}+\dfrac{1}{R_{\rm Db}}\right)} \tag{19}$$

H. Miyazawa and K. Noguchi for providing the high-frequency LN modulator used in the electro-optic pulse-pattern generator.

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