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A 40-Gbit/s Superdynamic Decision IC Fabricated with 0.12-μm GaAs MESFET's

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***Abstract*—This paper describes a 40-Gbit/s decision integrated circuit (IC) fabricated with 0.12-μm gate length GaAs metal–semiconductor field-effect transistors (MESFET's). A superdynamic flip-flop circuit and a wide-band amplifier were applied in order to attain 40-Gbit/s operation. A conventional static decision IC was also fabricated for comparison. The dynamic decision IC operated up to 40 Gbit/s, which is twice as fast as the conventional static decision IC. Error-free 40-Gbit/s operation is the fastest among GaAs MESFET decision IC's.**

***Index Terms*—Decision IC, flip-flop, GaAs MESFET, lightwave communication.**

I. Introduction

EMERGING lightwave communications technologies are about to bring 10-Gbit/s systems into commercial use [1]. Because of the growth of multimedia services, larger transmission capacity will be required in backbone networks. Intensive efforts are under way to develop large capacity systems using wavelength division multiplexing (WDM) and time division multiplexing (TDM) technologies. Recently, 40-Gbit/s-based WDM and TDM transmission experiments in the research stage were successfully carried out [2], [3]. The role of high-speed, reliable electronic components is becoming increasingly important in the development of cost-effective systems.

In these broad-band optical-fiber communications systems, the decision circuit is indispensable for realizing regeneration functions and is required 40-Gbit/s operation. In the last few years, various kinds of high-speed decision circuits using heterojunction bipolar transistor (HBT) [4], high electron mobility transistor (HEMT) [5], Si bipolar [6], and GaAs metal–semiconductor field-effect transistor (MESFET) [7] technologies have been reported. High-speed operation at, and/or beyond, 40 Gbit/s has been achieved only with the AlGaAs/GaAs HBT [4] and the InP HEMT [5]. Error-free operation at this bit rate has been confirmed only for the InP HEMT integrated circuit (IC). The GaAs MESFET is a promising candidate for fabricating cost-effective, high-speed digital IC's because of its process maturity.

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This paper describes circuit technologies for a 40-Gbit/s class decision IC fabricated with 0.12-μm GaAs MESFET's. The two keys to attaining high-speed decision circuit operation are the use of a high-speed flip-flop circuit and a wide-band amplifier. We adopted a superdynamic flip-flop circuit [7], because its high-speed operation using production-level GaAs MESFET's has been confirmed, and a parallel feedback amplifier and an inductor peaking amplifier for the input and output buffers. Using these circuit technologies, error-free 40-Gbit/s decision circuit operation was confirmed. For comparison purposes, we also fabricated a conventional master–slave static decision IC by the same process. Wide-band amplifiers were employed to suppress the degradation of the intrinsic static flip-flop circuit operation.

The next section outlines device parameter requirements for high-speed circuit performance and discusses the technical issues involved in attaining high-speed digital IC's. Section III describes the circuit design of the superdynamic flip-flop circuit and input and output buffers. Section IV describes the FET performances and measurement setup and presents and discusses the performance of IC's.

II. Device Parameter Requirements

Generally, circuit operation speed can be roughly predicted from the current-gain cutoff frequency f_T of the FET device. According to [8], the conventional master–slave D-type flip-flop (D-FF) can be operated at approximately 25% of the f_T. Likewise, a 24-Gbit/s superdynamic D-FF fabricated with 0.24-μm gate-length GaAs MESFET has been reported [7]. Since the f_T of the FET was 55 GHz, the superdynamic FF operated at 45% of the f_T. This indicates that a 40-Gbit/s static D-FF operation needs FET's that have an f_T over 160 GHz. However, a suitable GaAs MESFET has yet to be reported. We should, therefore, clarify the device design criteria to maximize IC speed performance as well as devise a new circuit design to improve the operation speed. In that sense, precise study on device figure of merits from the viewpoint of digital IC operation speed is very important to relaxing the device requirements as much as possible.

An analytical expression of the FF operation speed [9] has been derived on the basis of the small-signal transfer function of a source coupled FET logic (SCFL) inverter gate [10]. Fig. 1 shows the relationship between the results yielded by the analytical expression and those of HSPICE simulations. The unfilled rectangular symbols indicate the calculated results for the 0.2-μm GaAs MESFET, and the unfilled circles indicate

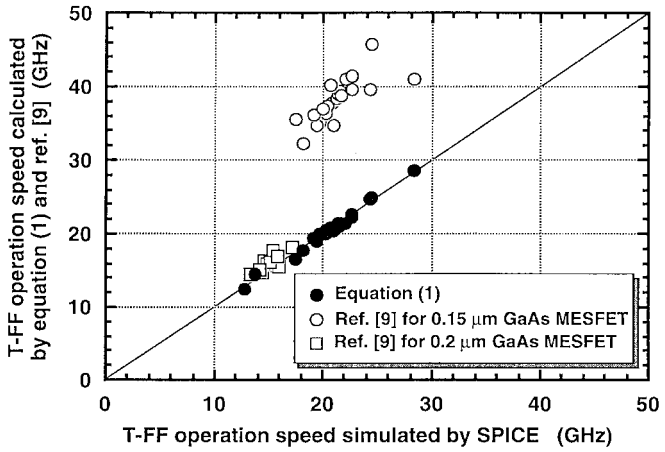

Fig. 1. The relationship between the results of SPICE simulation and those by (1).

TABLE I
FET PARAMETERS OF 0.15-μm GaAs MESFET

Gate width	*Wg*	50 μm
Transconductance	*gm*	22.8 mS
Drain conductance	*gd*	1.88 mS
Gate resistance	*rg*	12.85 Ω
Source resistance	*rs*	9.44 Ω
Drain resistance	*rd*	9.44 Ω
Gate-Source capacitance	*Cgs*	31.9 fF
Gate-Drain capacitance	*Cgd*	11.1 fF
Drain-Source capacitance	*Cds*	11.8 fF

*The values are at Vds = 1.5 V and Vgs = 0.55 V

TABLE II
EXTRACTED COEFFICIENTS OF (1)

α	7.35
β	1.4
γ	7.0
η	0.01
λ	- 2.0

those for the 0.15-μm-class GaAs MESFET. The calculated results for the 0.2-μm GaAs MESFET agree well with the SPICE simulation results. However, those for the 0.15-μm-class GaAs MESFET do not. This is because of the exclusion of large-signal behavior from the expression. In fact, the transconductance and gate-source capacitance have significant bias dependence, and in [9] and [10], each parameter is approximated to a constant value (mean value for large-signal operation). It is difficult to express the whole circuit behavior analytically. Especially in the case of short-channel FET's, the bias dependencies are more complicated due to short-channel effects. This is probably the reason for the large error in shorter gate-length FET's.

To solve these problems, we developed an FF-operation-speed equation. The method is a mixture of analytical and sensitivity analyses and has two features. The first is that the equation contains only the time constants extracted from the analytical delay time of an SCFL inverter gate based on a small-signal transfer function [10]. The second is that the sensitivity coefficients of the time constants are extracted by sensitivity analysis using SPICE circuit simulations. The first feature gives an intuitive understanding of the relations between circuit performance and device parameters. The second feature improves the accuracy of predicting circuit speed because the SPICE simulation results automatically include the bias dependency of each device parameter if we can obtain an accurate set of SPICE model parameters. In the proposed equation, the effects of the bias dependency of device parameters are included in the extracted sensitivity coefficients.

The proposed equation for an intrinsic toggle frequency $f_{\mathrm{MS-TFF}}$, excluding interconnection parasitics, is expressed in (1), shown at the bottom of the page, where gm, gd, rg, Cgs, Cgd, and Cds are transconductance, drain conductance, gate resistance, gate-source capacitance, gate-drain capacitance, and drain-source capacitance, respectively, and X is the product of gm and R_L, which corresponds to the logic swing of the FF circuit. Those FET parameters in (1) use the values at a standard bias point, which corresponds to the bias condition of the device characterization. The sensitivity coefficients α, β, γ, λ, and η are fitting parameters that are extracted by HSPICE simulation. Here, (1) was derived by rewriting the delay-time expression in [10] so as to include all time constants. All the factors of the time constants that appeared in the analytical expression in [9] and [10] are included, but the weighting of each time constant that contributes to circuit speed is optimized so as to satisfy sensitivity analysis.

The extraction method of the fitting parameters is as follows. First, the FET parameters are extracted as standard parameters for sensitivity analysis. As an example, 0.15-μm gate-length GaAs MESFET parameters are listed in Table I. These parameters were measured at a drain bias of 1.5 V and a gate bias of 0.55 V. A set of HSPICE model parameter is also extracted for transient simulations. Second, the circuit simulations are executed for a frequency divider. In this case, simulations for sensitivity analysis are executed within the range of $\pm$40% variation of the standard parameters. The variation range approximately corresponds to GaAs MESFET's with gate lengths from 0.24 to 0.12 μm [11]. Third, a set of fitting parameters is extracted to minimize the errors between the SPICE simulation and calculation using (1). The values of the coefficients extracted for 0.24–0.12-μm gate-length GaAs MESFET's are summarized in Table II. The relationship

$$f_{\mathrm{MS-TFF}} = \frac{gm}{\left\{\alpha \cdot Cgd \cdot \left(1+\frac{X}{1+X\frac{gd}{gm}}\right)\cdot(1+\eta\cdot rg)+\beta\cdot Cgs\cdot(1+\eta\cdot rg)+\gamma\cdot Cds\right\}\cdot\left(1+\left(\frac{1}{1+\lambda\frac{gd}{gm}}\right)\right)} \quad (1)$$

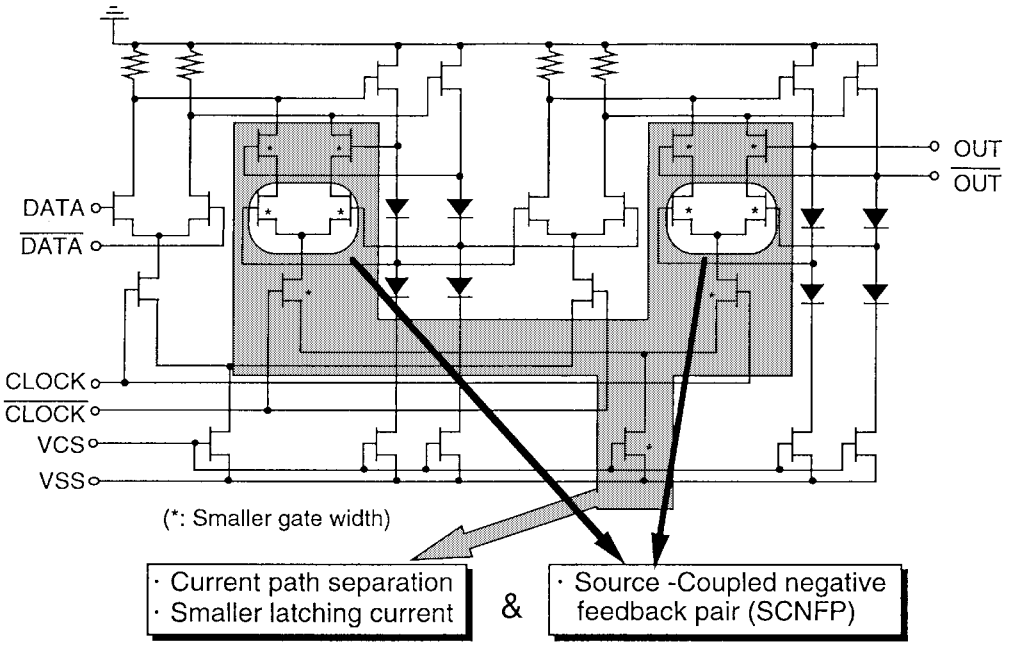

Fig. 2. Circuit diagram of the superdynamic D-FF.

between the SPICE simulation and the calculation by (1) is also shown in Fig. 1 with filled circles. The agreement is quite good, indicating that (1) accurately and sufficiently expresses the relationship between the circuit performance and the device parameters.

Equation (1) reveals that the circuit speed is proportional to gm, and the Cgd is the most dominant parameter that limits the IC speed. gd/gm is also an important parameter. The equation takes similar formations to the definition of f_T, which is expressed in (2), shown at the bottom of the page. The IC speed is related to the f_T, but not directly. In other words, FET's with lower f_T may bring faster IC operation than those with higher f_T if the Cgd is lower. The maximum intrinsic toggle frequency of a static frequency divider, when we assume a 0.15-μm gate-length GaAs MESFET in Table I, is calculated to 22.5 GHz using (1). The f_T needed for the 40-GHz static T-FF operation is estimated using (2). Here, device parameters are assumed to be attainable for a 0.15-μm GaAs MESFET. The ratio of gd and gm is 0.1. The rg is 12.8 Ω. Parameter X is four. Furthermore, Cgd is equal to Cds, and Cgd/Cgs is 0.33. As a result, an f_T of 160 GHz is required for 40-GHz static T-FF operation.

The shrinkage of the gate length is one way to improve device speed. A record f_T value of 163 GHz has been achieved for 0.06-μm gate-length GaAs MESFET's [12]. It is noted, however, that the short-channel effects become so severe as to considerably degrade the circuit speed performance. One of the most typical aspects is the dull slope of f_T (or transconductance) dependence on gate-source voltage Vgs. Although the threshold voltage decreases in the negative bias region as the gate length is shortened, the gate-source voltage Vgs point that gives the maximum f_T (or the maximum transconductance $gm_{\max}$) almost stays at a high level ($\sim$0.5 V). This, in turn, results in a dull DC transfer curve for a large-signal operation of logic circuits if the circuit is designed to make full use of the device speed.

Considering these short-channel effects, 40-Gbit/s static FF operation using 0.1-μm class GaAs MESFET is quite difficult. Therefore, circuital improvements, such as a dynamic operation, are indispensable.

III. Circuit Design

A. High-Speed Flip-Flop Circuit

As mentioned earlier, one of the keys to attaining high-speed decision circuit operation is to use a high-speed D-FF. We adopted the superdynamic D-FF [7] for 40-Gbit/s operation because its high-speed operation using production-level GaAs MESFET's has been confirmed. The circuit diagram of the superdynamic D-FF is shown in Fig. 2. The circuit features are:

1) a series-gate connection to separate the current path of the reading and latching circuits;
2) a smaller latching current (I-latch) than the reading current (I-read);
3) a source coupled negative feedback pair (SCNFP) inserted in the first-level latching differential pair in a cascode manner.

$$f_T = \frac{gm0}{2\pi[(Cgs+Cgd)\cdot\{1+gd\cdot(rs+rd)\}+Cgd\cdot gm0\cdot(rs+rd)]} \tag{2}$$

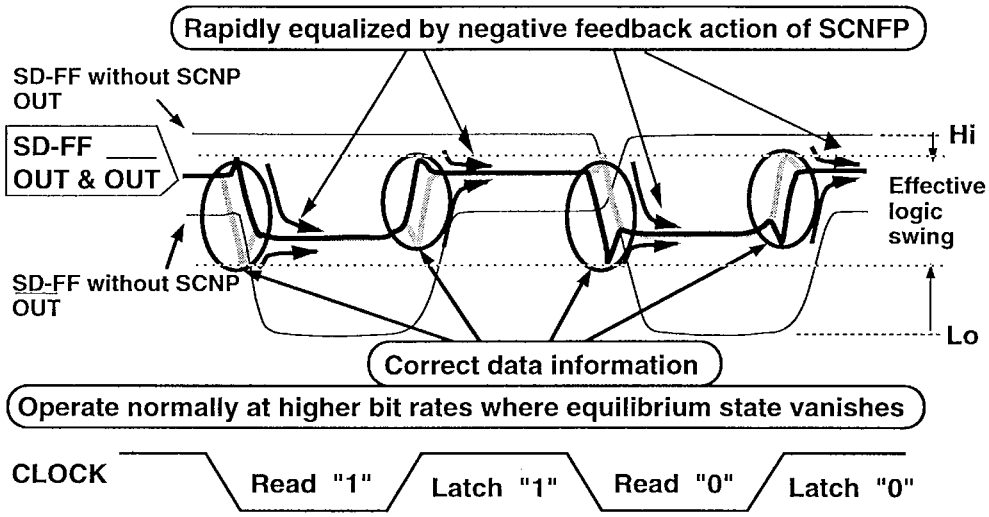

Fig. 3. Output waveform of the superdynamic D-FF at low clock frequency.

A schematic output waveform of the superdynamic D-FF at very low frequency is shown in Fig. 3. Due to the negative feedback action of the SCNFP, input data is stored for only a short time at every transition between the reading and latching operation. This makes the FF operate dynamically, which means that the FF has a minimum operation bit rate. It should be noted that the FF operates from DC for the data signal. The SCNFP can drastically reduce the effective logic swing from $R_L I$-read to $R_L/2$(I-read–I-latch) without any degradation of the signal transition slew rate, where R_L is the load resistance. This leads to faster operation.

Fig. 4 shows the operation speed of the superdynamic decision IC versus gate width ratio Wg-latch/Wg-read, which corresponds to I-latch/I-read. The circuit performance was simulated by HSPICE using a 0.12-μm gate-length class GaAs MESFET having an f_T of around 100 GHz. The operation speed was simulated assuming that the output voltage and phase margin were larger than 700 m$V_{\mathrm{p-p}}$ and 180°, respectively. In this case, a repeated (1000) pattern was used for the input data signal. The gate width of the reading circuit and load resistance R_L were fixed to optimized values of 30 μm and 350 Ω, respectively. The maximum operation speed increased as the gate-width ratio increased. The minimum operation speed also increased as the gate-width ratio increased. To obtain high-speed operation with a wide operation range, we adopted the gate-width ratio of 0.5. The maximum speed at this ratio was 100% higher than that of the conventional static master–slave D-FF.

To verify the contribution of the superdynamic D-FF to speed improvement, a conventional static decision IC with a master–slave D-FF was also fabricated. Fig. 5 is the circuit diagram of the master–slave D-FF. This circuit is designed in the same way as the superdynamic D-FF with respect to the supply voltage and the bias condition of each FET.

B. Wide-Band Buffer Circuits

The other key to attaining a high-speed decision IC is the wide-band amplifier. As the core D-FF speed increases,

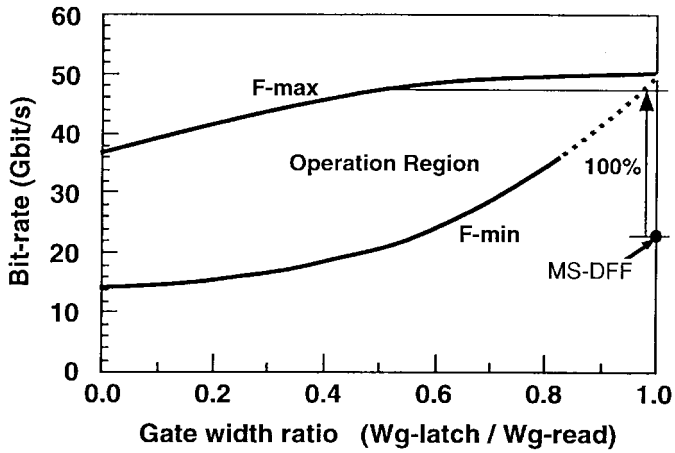

Fig. 4. Operation speed of the superdynamic decision IC versus gate-width ratio (Wg-latch/Wg-read).

the bandwidth of conventional data and clock buffers can no longer cover the flip-flop operation range. It has been reported that the bandwidth of these buffers causes degradation of the retiming capability of D-FF's [7].

The data and output buffer require a wide bandwidth from DC to the maximum FF operation frequency, as well as a high flat gain. These factors affect the input sensitivity of the decision IC and the quality of its output waveform. These buffers are usually required to cover bandwidths over approximately 70% of the input data bit rate. The parallel feedback differential amplifier [13] shown in Fig. 6 is employed in the data input buffer, and the inductor-peaking differential amplifier shown in Fig. 7, is adopted for the output buffer. For these buffers, capacitance peaking was also added to the source follower circuits to compensate for the loss of the source follower. Figs. 8 and 9 show the simulated gain-bandwidth characteristics of the input and output buffers, respectively. For the simulation of the input buffer, a reference DC voltage is fed to the complementary input terminal, considering a single-ended input interface condition. On the other hand, the output buffer is simulated with a differential input drive because the

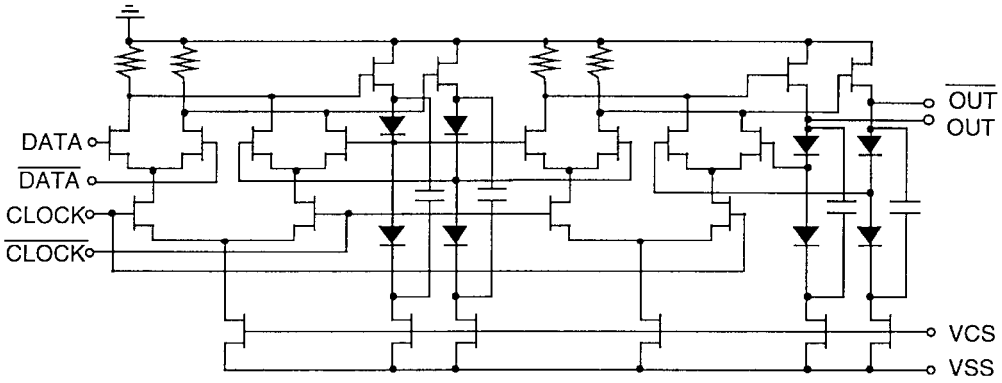

Fig. 5. Circuit diagram of the master–slave D-FF.

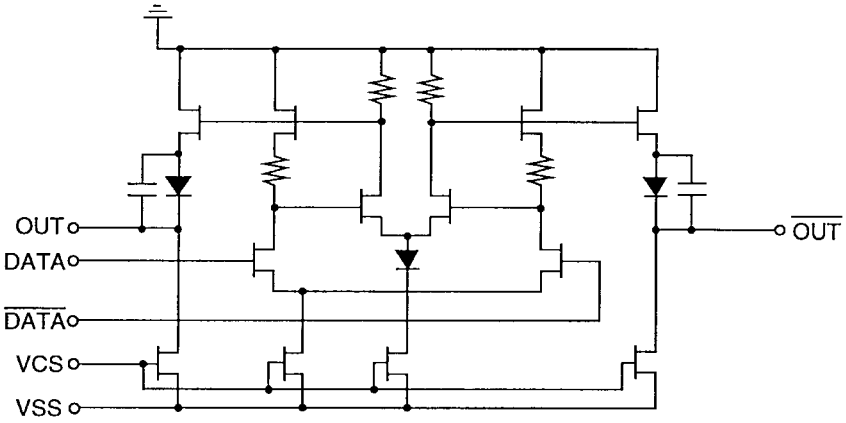

Fig. 6. Circuit diagram of the parallel feedback data buffer.

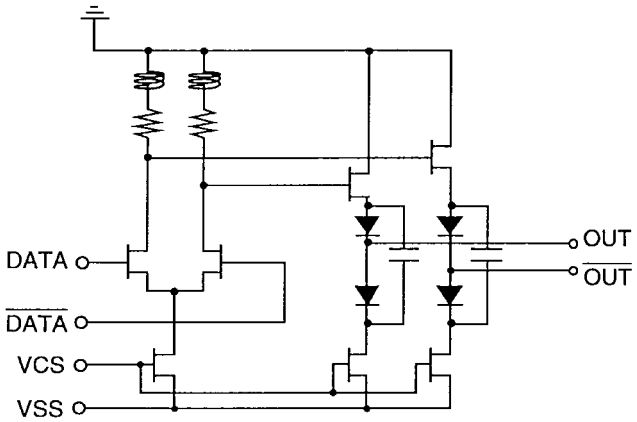

Fig. 7. Circuit diagram of the inductor-peaking output buffer.

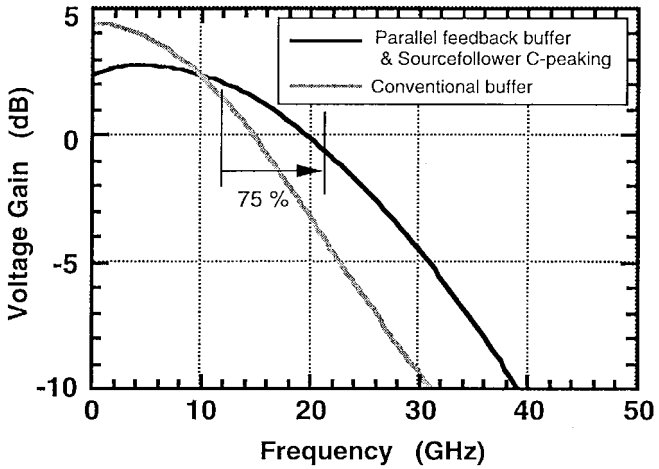

Fig. 8. Simulated gain bandwidth of the parallel feedback input buffer.

internal operation is assumed to be a differential operation. Simulation results indicate that the 3-dB down bandwidths for both the data input and output buffers are improved by 70% compared to those of conventional buffers. They almost completely cover the required bandwidth for the 40-Gbit/s data signal.

Clock buffers require high gain in the FF operation frequency region. Fig. 10 shows the simulated gain-bandwidth characteristics of the three-stage conventional amplifier. Since it is insufficient for both the static FF and the superdynamic FF, we investigated a three-stage inductor peaking buffer. The gain-bandwidth characteristic of the buffer is also shown in Fig. 10. The gain at 20 GHz is 5 dB, which is a significant improvement compared to that of the conventional one. Therefore, we adopted the buffer for the static decision IC. However, it still does not cover the 40-GHz range. Since the superdynamic D-FF has a minimum operation clock frequency, its clock buffer does not need broad-band operation from DC. Therefore, an AC-coupled passive level shifter shown

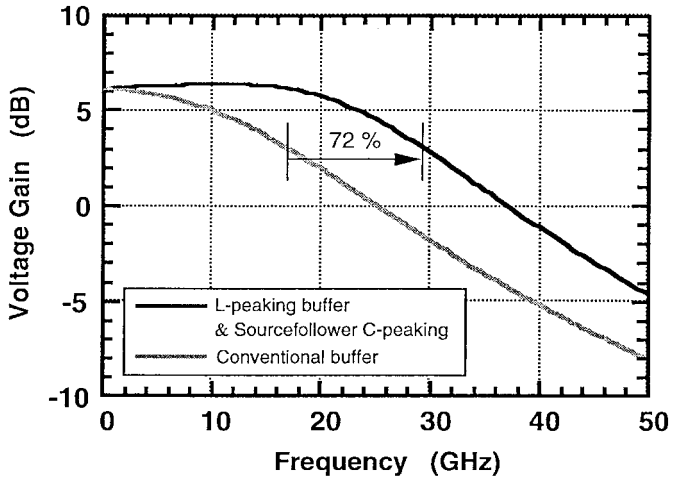

Fig. 9. Simulated gain bandwidth of the inductor peaking output buffer.

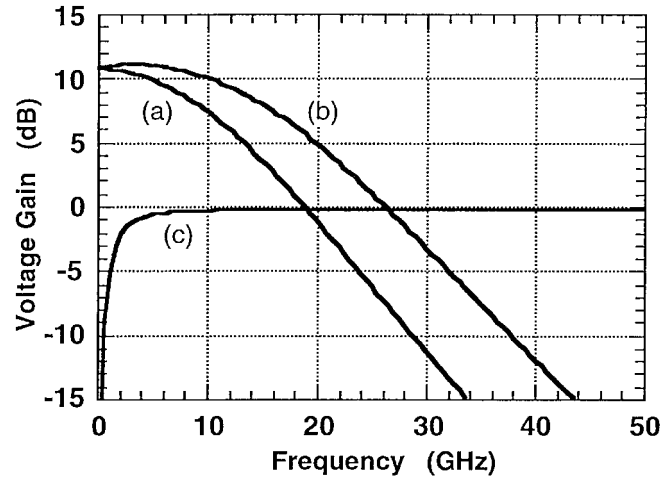

Fig. 10. Simulated gain bandwidth of clock buffers. (a) A three-stage conventional clock input buffer. (b) Three-stage inductor peaking clock input buffer. (c) AC-coupled passive level shifter.

in Fig. 11 was adopted for the clock buffer. It consists of a blocking capacitor and a resistive divider. Its gain-bandwidth plot is also shown in Fig. 10.

IV. Experiments

A. Circuit Configurations

All of the IC's are designed as SCFL series-gated circuits and can be directly connected to the SCFL interface. Both of the decision IC's have a single data input and differential outputs, which are, respectively, connected to impedance-matched 50 and 100 Ω termination resistors to obtain clear eye patterns. The supply voltage is −4.5 V. A block diagram of these IC's is shown in Fig. 12. The superdynamic decision IC consists of a two-stage parallel feedback amplifier data buffer, an inductor peaking output buffer, an AC coupled clock buffer, and a superdynamic D-FF. The static decision IC comprises a three-stage inductor peaking clock buffer, a conventional data buffer, an inductor peaking output buffer, and a master–slave D-FF.

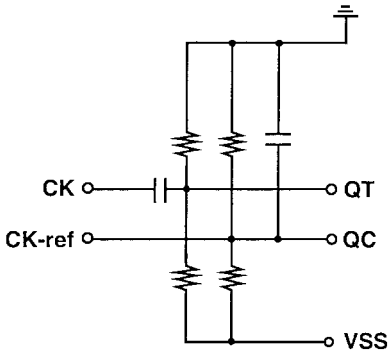

Fig. 11. Circuit diagram of an AC-coupled passive level shifter.

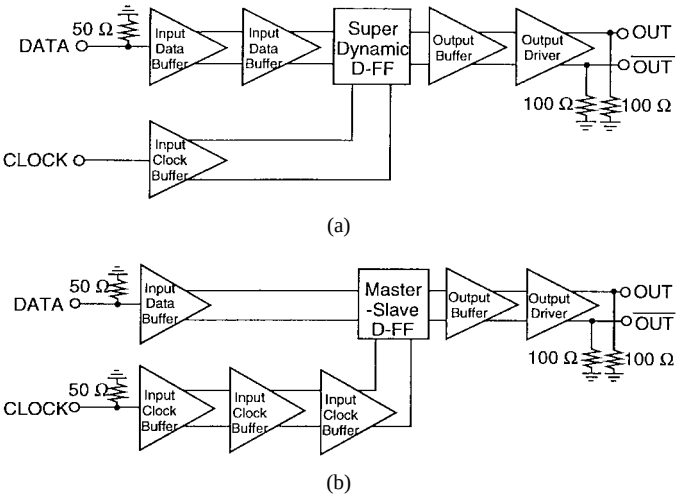

Fig. 12. Block diagrams of the fabricated IC's. (a) The superdynamic decision IC. (b) The static decision IC.

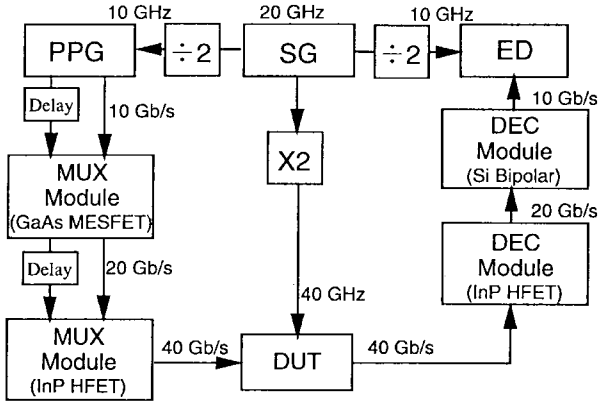

Fig. 13. Measurement setup.

B. FET Performance

The IC was fabricated with 0.12-μm self-aligned Au/WSiN-gate GaAs MESFET's [12]. A 0.12-μm gate length was obtained by i-line photolithography with shrinkage of the resist size by O_2 reactive ion and electron cyclotron resonance etching. Furthermore, a two-step buried p-layer lightly doped drain structure was applied in order to suppress short-channel effects. For the interconnection structure, a standard double Au-layer interconnection was employed. The threshold

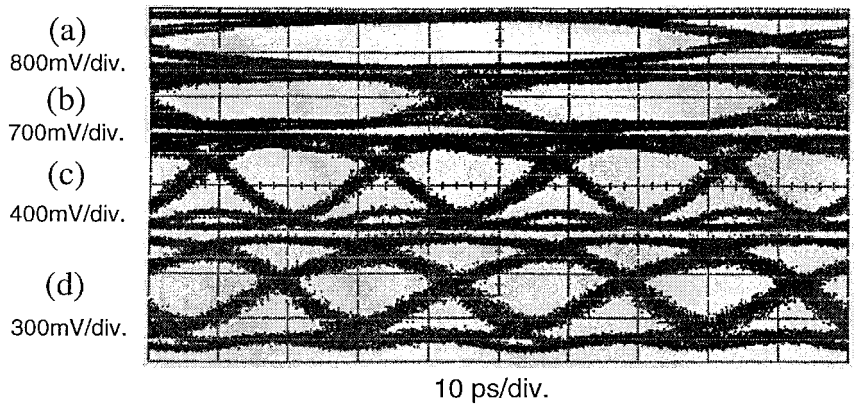

Fig. 14. Operation waveforms in 40-Gbit/s error-free confirmation. (a) 10-Gbit/s demultiplexed signal (Si Bipolar DEC output). (b) 20-Gbit/s demultiplexed signal (InP DEC output). (c) 40-Gbit/s DUT input signal. (d) 40-Gbit/s DUT output signal.

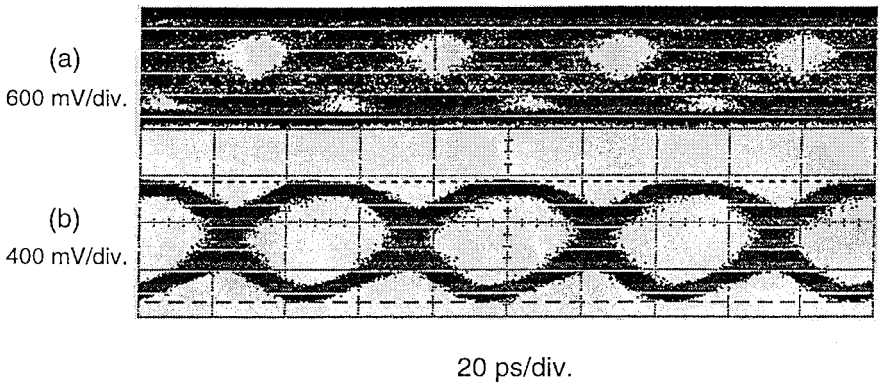

Fig. 15. Operation waveforms of the superdynamic decision IC at 20 Gbit/s. (a) Input. (b) Output.

voltage (V_{th}) was optimized to approximately 0.0 V for high-speed SCFL circuit operation. The transconductance was 481 mS/mm, and Cgd was 17.6 fF/100 μm. The average current-gain cutoff frequency f_T was 98 GHz, and the maximum frequency of oscillation $f_{\max}$ was 97 GHz.

C. Measurement Setup

The IC was tested on a wafer with dedicated 40-GHz bandwidth multiple contact probes. Fig. 13 shows the measurement setup. Complementary pairs of a fundamental pseudorandom data stream up to 10 Gbit/s were generated from a pulse pattern generator (PPG). The pairs were duplexed with appropriate delay against each other by a GaAs MESFET MUX unit [14] to obtain a complementary data stream up to 20 Gbit/s. They were also duplexed, again with appropriate delay against each other, by an InP HFET MUX module [15] to obtain a data stream up to 40 Gbit/s, and then input to the decision IC. The output of the decision IC was demultiplexed to 20 Gbit/s by an InP HFET demultiplexer module [15], and then to 10 Gbit/s by a Si bipolar decision IC to confirm error-free operation using a 10-Gbit/s error detector (ED). For the 20-Gbit/s measurements, the InP HEMT multiplexer and demultiplexer module were removed from the measurement setup.

In the measurement setup, the quality of clock synchronization becomes more important as the data bit rate increases. Conventional 10-MHz synchronization between plural synthesized clock sources is insufficient for stable error-free confirmation and waveform observation. Therefore, 40-GHz clock signals for the decision IC and 10-GHz clock signals for MUX, DEMUX, PPG, and ED were generated from a single 20-GHz synthesized signal source (SG) using a doubler and a frequency divider, respectively.

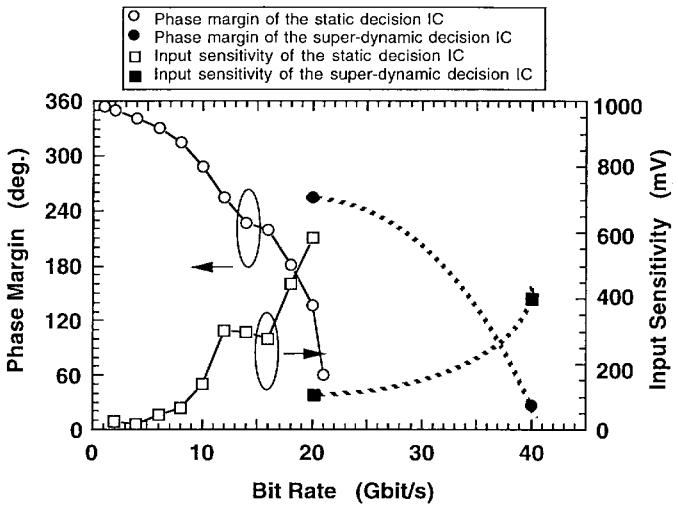

Fig. 16. Bit-rate dependency of the phase margin and input sensitivity of the decision IC's.

D. Circuit Performance

The superdynamic decision IC operated from under 20–40 Gbit/s. The power dissipation was 0.98 W. Fig. 14 shows the

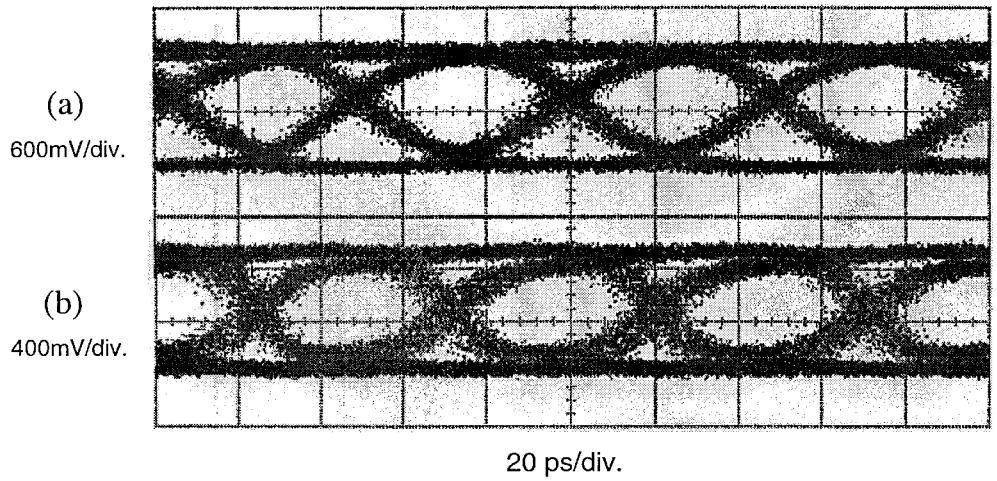

Fig. 17. Operation waveforms of the static decision IC at 20 Gbit/s. (a) Input. (b) Output.

input and output eye diagrams at 40 Gbit/s. Good eye opening with a 0.75 $V_{\mathrm{p-p}}$ swing was obtained. This indicates that the output buffer satisfied the required bandwidth for a 40-Gbit/s data signal. Fig. 14 also shows a 20-Gbit/s demultiplexed signal and a 10-Gbit/s demultiplexed signal in the 40-Gbit/s error-free confirmation. Under the above conditions, stable error-free operation at 40 Gbit/s was confirmed. The input sensitivity and phase margin of the IC at 40 Gbit/s (PN $2^{23}-1$) were approximately 400 mV and 27°, respectively. When the fundamental 10-Gbit/s pseudorandom bit sequence (PRBS) was shortened to PN $2^{15}-1$, phase margin was increased to 57°. A higher gain and wider bandwidth will be required for the input buffers in order to improve the input sensitivity.

Fig. 15 shows the input and output eye diagrams at 20 Gbit/s, which is close to the lower speed limit. To show the retiming performance, the input data timing was swept by 220°. Because of the dynamic circuit operation, low and high levels cannot be kept constant and are periodically forced to the center level at every transition timing. The measured phase margin at this bit rate was 254°, which is wide enough. Except for the dynamic operation, the output exhibits a clear eye-opening. Therefore, this circuit works well as a retimer circuit even at this low bit rate. The phase margin and input sensitivity of the IC are plotted in Fig. 16. Because of the complexity of the measurement setup, error-free operation was not confirmed at other bit rates between 20–40 Gbit/s. However, we obtained good eye diagrams in those bit rates.

The static decision IC was tested with a PN 23 PRBS data signal. Error-free operation was confirmed up to 21 Gbit/s. The power dissipation was 1.2 W. Fig. 17 shows the input and output eye diagrams at 20 Gbit/s. Good eye opening with 1.0 $V_{\mathrm{p-p}}$ voltage swing was obtained. Fig. 16 also shows the bit-rate dependency of the phase margin and input sensitivity of the IC. The input sensitivity and phase margin at 20-Gbit/s operation were 590 mV and 137°, respectively.

The superdynamic decision IC operates approximately 100% faster than the conventional one does. The operation speed reached 40% of the cutoff frequency of the FET. This indicates that the superdynamic flip-flop and wider-bandwidth buffers are indispensable to relaxing the requirement for device speed performance.

V. Conclusion

We have described circuit design technologies for a high-speed decision IC using short-gate GaAs MESFET's. First, we introduced an FF operation speed equation containing FET parameters. Concerning FET parameters, high transconductance with short-channel effect suppression and lower gate-drain capacitance are essential for improving digital circuit performance. These analytical results indicated that a dynamic FF is indispensable for realizing a 40-Gbit/s decision IC using 100-GHz f_T class 0.12-μm GaAs MESFET's. To clear 40-Gbit/s operation, a superdynamic FF, which operates twice as fast as a conventional master–slave FF, was adopted. Additionally, wide-band amplifier circuits for clock and data buffers were used to maximize the decision circuit performance up to the FF speed limit. The superdynamic decision IC fabricated with 0.12-μm gate-length GaAs MESFET's successfully exhibited error-free 40-Gbit/s operation. The operation speed reached 40% of the current-gain cutoff frequency of the FET. This indicates that the superdynamic flip-flop and wider bandwidth buffers are indispensable to relaxing the requirement for device speed performance.

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