An 80-Gbit/s multiplexer IC using InAlAs/InGaAs/InP HEMTs

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An 80-Gbit/s Multiplexer IC Using InAlAs/InGaAs/InP HEMT's

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***Abstract*— This paper describes the design and performance of an 80-Gbit/s 2 : 1 selector-type multiplexer IC fabricated with InAlAs/InGaAs/InP HEMT's. By using a double-layer interconnection process with a low-dielectric insulator, microstrip lines were designed to make impedance-matched, high-speed intercell connection of critical signal paths. The record operating data rate was measured on a 3-in wafer. In spite of the bandwidth limitation on the measurement setup, clear eye patterns were successfully observed for the first time. The obtained circuit speed improvement from the previous result of 64 Gbit/s owes much to this high-speed interconnection design.**

***Index Terms*— HEMT, IC, multiplexer, optical communications.**

I. Introduction

THE rapid movement toward broad-band integrated services digital network (ISDN) and multimedia services urgently demands an expansion of transmission capacity to a level beyond a terabit per second. In terms of system practicality, reliability, and cost, we still have to improve the speed of electronic IC's to around 40 Gbit/s and more even though wavelength-division multiplexing (WDM) and optical time-division multiplexing (OTDM) technologies relax the demands on the single-channel bit rate. Recently, several 40-Gbit/s class IC's were developed [1]–[10], and a fully-electrical TDM (ETDM) optical fiber transmission experiment was demonstrated at this bit rate [11], [12].

High-speed time-division multiplexers (MUX's) are key components in broad-band optical fiber communication systems. Recently, 40-Gbit/s-class MUX IC's were developed using various high-speed devices: Si bipolar transistors [3], heterojunction bipolar transistors (HBT's) based on SiGe [6], GaAs [4], and InP [2], [5], GaAs metal-semiconductor field-effect transistors (MESFET's) [8], and high-electron mobility transistors (HEMT's) based on GaAs [9] or InP [1], [10]. To date, the highest data rate of the MUX reported so far is 64 Gbit/s on a wafer [10], 60 Gbit/s on a test fixture [6], and 52 Gbit/s on a packaged module [10]. The trend shows that the FET-based MUX IC speed reaches around one-half the current-gain cutoff frequency (f_T) of the FET's used. In terms of device speed potential, InP-based HEMT's (having an f_T of beyond 200 GHz) seem to achieve the highest MUX IC speed of around 100 Gbit/s.

In such an ultrahigh-speed region, however, the signal wavelength approaches the physical dimensions of circuit size, which in turn causes numerous parasitic effects that limit circuit speed. This is the main reason why the device speed no longer directly reflects the IC speed. In that sense, distributed treatment becomes very important in IC design.

In this paper, we describe the design and performance of a very-high-speed 2 : 1 MUX IC we developed using InAlAs/InGaAs/InP HEMT's. A new impedance-matched interconnection technique was adopted for the intercell connections of critical signal paths. This drastically reduces the waveform distortion due to multiple reflection along the interconnection lines that critically limits circuit speed. An excellent eye opening at the record bit rate of 80 Gbit/s was demonstrated from a fabricated chip on a wafer.

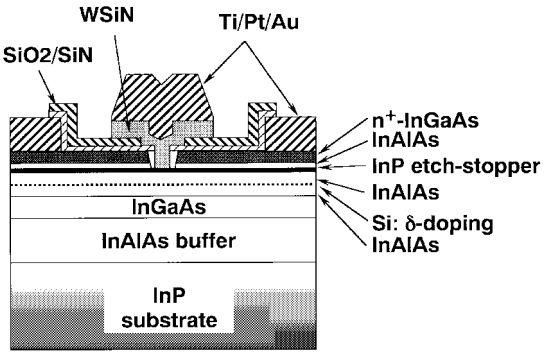

Fig. 1. Cross-sectional view of the HEMT structure.

II. Process Technology

The IC process we used is a 0.1-μm gate length InAlAs/InGaAs/InP HEMT process [13], [14]. Fig. 1 shows the cross-sectional view of the HEMT structure. The electron channel is formed with a 15-nm-thick InGaAs layer. The carrier-supplying layer is formed with an InAlAs layer with Si-delta doping (4.5×10^{12} cm^{-2}). A novel InP gate-recess-etch stopper inserted into the InAlAs barrier layer dramatically improves the uniformity of the transistor performance [the average threshold voltage (Vth): -0.65 V with a standard deviation of less than 40 mV in a 3-in wafer]. The average transconductance, f_T, and $f_{\max}$ are 1050 mS/mm, 195 GHz, and 230 GHz, respectively.

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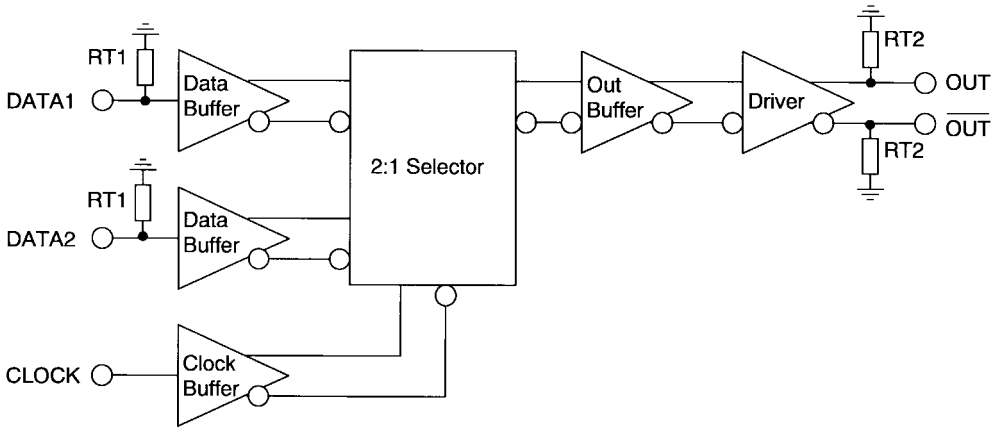

Fig. 2. Circuit block diagram of the MUX IC.

As the device speed increases, the interconnection propagation delay begins to dominate circuit speed performance [15]. Thus, high-speed interconnection technology is crucial. To reduce interconnection propagation delay by making the layout denser, small low-loss Schottky diodes using additional i-InAlAs/n^+-InAlAs layers were introduced.

In addition, we newly adopted a high-speed interconnection process using two metal layers consisting of gold and a 2-μm thick benzocyclobutene (BCB) film as an interlevel dielectric with a low permittivity ($\varepsilon_r = 2.8$). This process allows configuration of a microstrip line (MSL) structure that cannot be made with a conventional air-bridged metal interconnection process. An MSL with a narrow second-layer conductor on top of the first-layer ground can offer a high-speed signal transmission with a low characteristic impedance [16]. This is the key to achieving ultrahigh-speed operation for digital IC's as explained in the following discussion.

III. Circuit Design

A. Core Circuit Design

Fig. 2 shows the circuit block diagram of the MUX. Each block is based on the SCFL (source-coupled FET logic) series-gated circuitry. Internal differential circuitry consists of 20-μm FET's and 130-Ω load resistors. All the data and clock inputs are single-ended. The data/clock inputs are matched to 50 Ω with internal termination resistors.

The core of the MUX is based on a simple selector circuitry as shown in Fig. 3. Capacitive peaking was incorporated into the source followers, which compensates for the loss at high frequencies resulting in higher speed operation (the speed improvement is about 15%). HSPICE simulation shows that the selector core circuit can operate faster than 75 Gbit/s under an ideal data/clock input condition.

As the core circuit operates faster, data and clock buffers should expand their bandwidth to maximize the speed performance of the whole circuit. The data input stage of the MUX was designed as a data buffer with three stages as shown in Fig. 4. Each stage consists of a capacitive-feedback differential amplifier [17] and a couple of source followers with capacitive peaking. The capacitive feedback cancels the influence of the parasitic gate capacitance. A simulated gain-bandwidth of the data buffer is shown in Fig. 5. This input stage has a -3-dB bandwidth of 25 GHz with a dc voltage gain of 12 dB, which assures us of >35-Gbit/s nonreturn-to-zero data amplification.

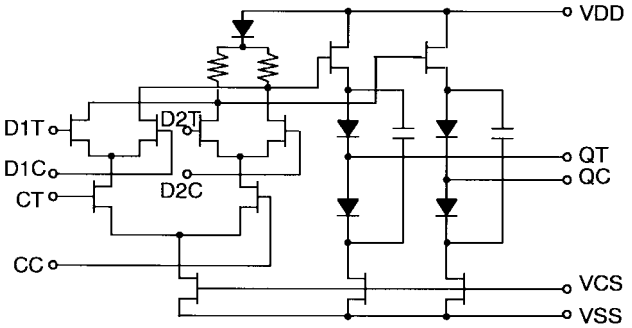

Fig. 3. Circuit diagram of the selector core.

The circuit diagram of the clock buffer is shown in Fig. 6, which consists of a two-stage inductor peaking differential buffer. A capacitively coupled resistive divider instead of a source follower was introduced as a low-loss passive RF level shifter. The input-impedance of the first-stage level shifter was designed to be 50 Ω for better impedance matching to the outer transmission line, and others were designed to be larger than 1 kΩ taking into account the relatively low drivability of the internal SCFL gate. The lower cutoff frequency of the passive RF level shifter was designed at less than 2 GHz so that a wide operating range from less than two to more than 40 GHz could be obtained. A simulated gain-bandwidth of the clock buffer is shown in Fig. 7.

The output stage consists of a series with a two-stage buffer (20-μm FET's for the first stage and 40-μm FET's for the second one) and a driver (70-μm FET's) with impedance-matched termination resistors at the differential output drain nodes. The power supply voltage is -5.2 V. The chip consumes 2.7 W. The chip size is 2×2 mm. A microphoto of the chip is shown in Fig. 8.

B. High-Speed Interconnection Design

The SCFL circuit has a low-output-impedance and high-input impedance. The dc output impedance of the source

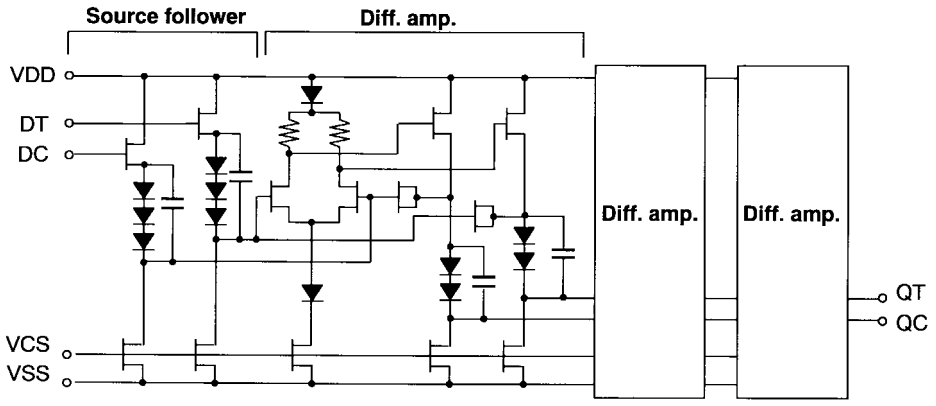

Fig. 4. Circuit diagram of the data buffer.

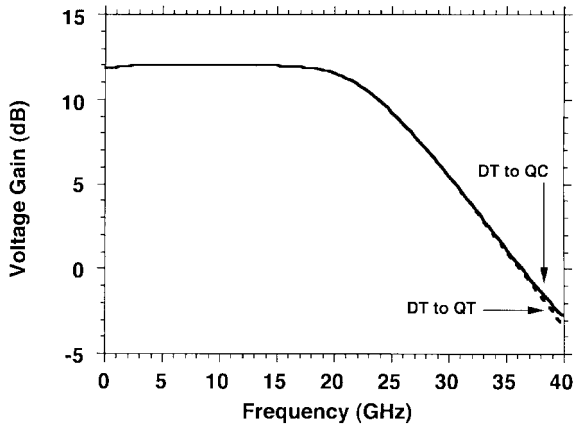

Fig. 5. Simulated gain-bandwidth characteristics of the data buffer.

follower is approximately given by $1/(gm+gds)$, where gm and gds are the FET transconductance and drain conductance and is generally in a range of 20–40 Ω. At high frequencies, the output impedance decreases a little more due to FET parasitic capacitances. The input is the gate node, so its impedance is very high (in the order of tens of kΩ). The problem occurs when the line length approaches one-tenth of the signal wave length and the line acts as a distributed element. Assuming a 40-GHz frequency and an effective dielectric constant of 7.0, the physical length corresponding to one-tenth of the signal wavelength would be 280 μm, which is comparable to or less than the length of the intercell connection of critical signal paths. In this case, the output forward going signal is perfectly reflected at the far end, so the problem is with multiple reflection, which is caused by the mismatch between the line impedance and the output impedance. For the digital IC layout, a simple strip line (SL), shown in Fig. 9(a), is generally used. This is reasonable for the dense interconnection required of digital IC's. The characteristic impedance of the SL is relatively high, however (around 150 to over 200 Ω). Therefore, severe distortion occurs and degrades speed performance.

In general, differentially driven circuits, such as SCFL's, generally use a double-railed SL layout for intercell connection of the critical paths. This helps reduce the characteristic impedance. Line impedance is still larger than the SCFL output impedance, however, and largely varies with the other SL's potential and also with surrounding environments because of the lack of steady ground.

A microstrip line (MSL) with a narrow second-layer conductor on top of the first-layer ground, shown in Fig. 9(b), is best suited for high-speed, low-impedance signal transmission on IC's. Fig. 10 plots the simulated characteristic impedance (Zo) and propagation velocity (vp) for SL and MSL as a function of the ground width L. The cross-sectional view of the simulated MSL is shown in Fig. 9(b). We used an in-house quasi-static two-dimensional electromagnetic simulator. The parameters are a signal line width W, a ground line width L. The relative dielectric constant of the insulator (BCB) is 2.8. The metal thickness is 0.7 μm for the first layer and 1.5 μm for the second layer. The insulator was assumed to be perfectly flattened, and its thickness is 1.5 μm on top of the first-layer metal. The InP substrate thickness is 600 μm. Since electromagnetic field distribution is almost concentrated just under the signal line, a narrow first-layer ground line having an L only twice as large as W can almost isolate the signal line from the InP substrate. Then, the effective dielectric constant is drastically reduced from 6.7 to 2.6, and the vp increases by 50%. In addition, the Zo of the MSL is drastically reduced from 200 Ω to 40–70 Ω. This makes for better matching to the output impedances of the data and clock buffers.

The MSL was adopted for intercell connection from the data buffer to the selector core and from the clock buffer to the selector core. The physical lengths of these connections are 400 and 330 μm, respectively. The MSL's are double-railed with a W of 2 μm, a distance between signal lines of 5 μm, and a L of 18 μm. The high-speed interconnection helped reduce their electrical lengths below one-tenth of the wavelength at frequencies of up to 50 GHz. In addition, the characteristic impedance of the MSL is very low (63 Ω) when compared to a conventional line without a first-layer ground (∼150 Ω), which results in better matching to the low output impedances (∼25 Ω and ∼60 Ω) of the data and clock buffers.

Fig. 11 shows simulated 40-Gbit/s waveforms at the data input node of the selector core circuit, which corresponds to an 80-Gbit/s selector operation. For comparison, a conventional layout using SL's was also simulated. The line parameters W and D were the same as for MSL's. The procedure of

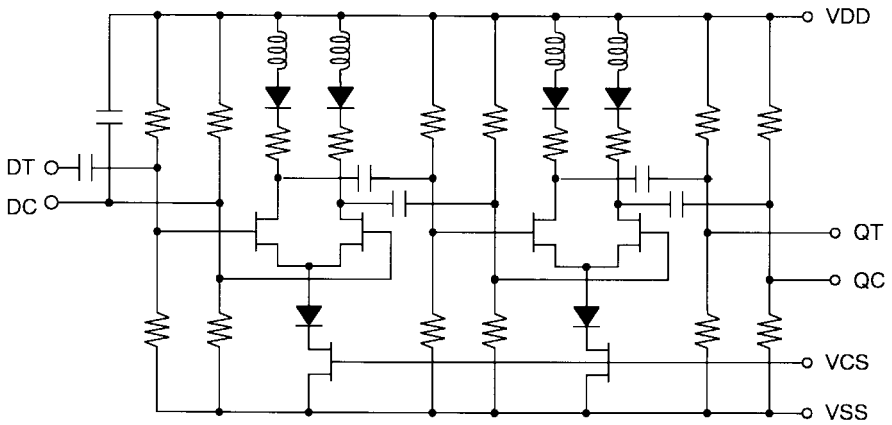

Fig. 6. Circuit diagram of the clock buffer.

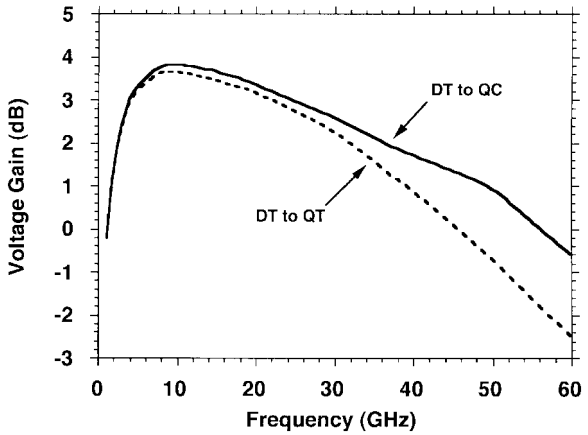

Fig. 7. Simulated gain-bandwidth characteristics of the clock buffer.

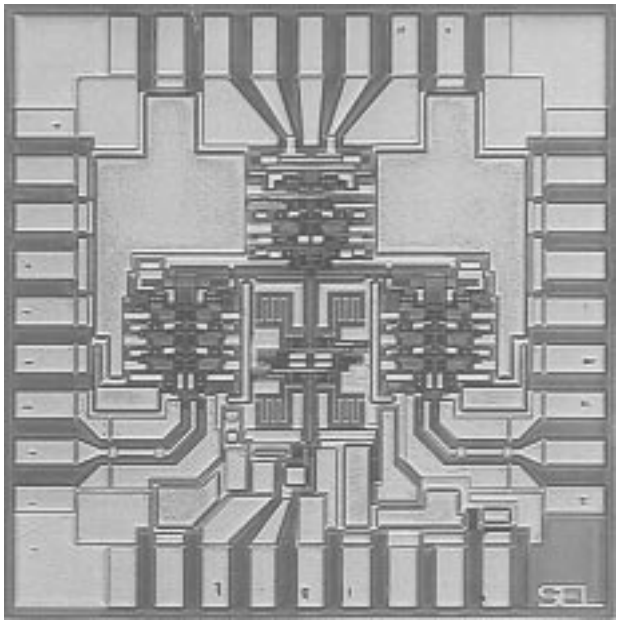

Fig. 8. Microphoto of the MUX IC (2 mm × 2 mm).

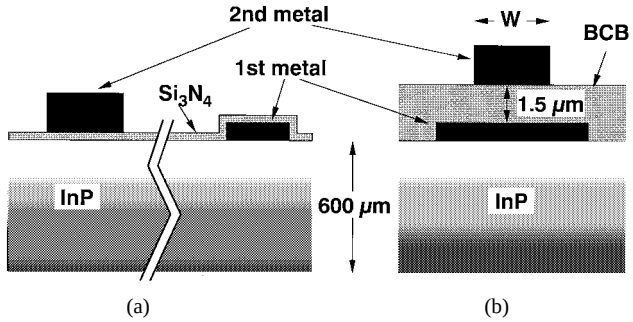

Fig. 9. Cross-sectional view of (a) the strip line and (b) the microstrip line.

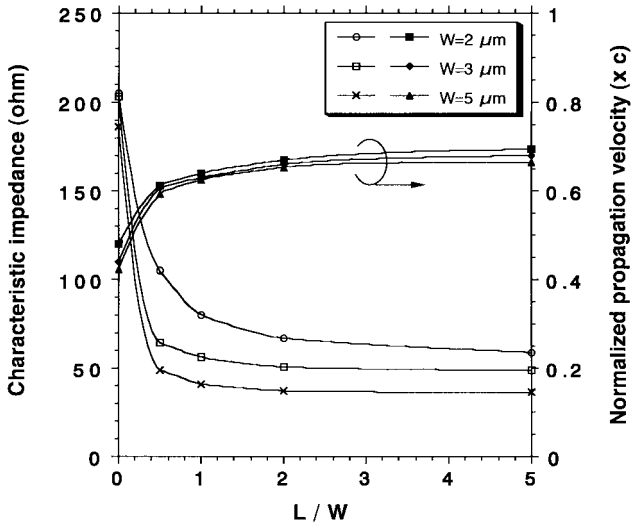

Fig. 10. Simulated characteristic impedance (Zo) and propagation velocity (vp) of MSL's. The vp is normalized to the velocity of light in a vacuum.

the simulation is as follows. First, the S parameters of those lines were analyzed. Second, the lines were modeled in a LCR ladder circuit (with a unit section length of 10 μm), and its circuit parameters were extracted so as to fit the circuit response to the results of an electromagnetic simulator by using the optimization function of the microwave circuit design simulator MDS. Third, the line model was incorporated into the HSPICE net list of the IC. Finally, the transient response of the IC was simulated. The signal distortions, due to multiple-reflection along the interconnection lines, are well suppressed for the high-speed interconnection while a conventional case exhibits severe distortion. These are keys to achieving high-speed circuit operation beyond 60 Gbit/s.

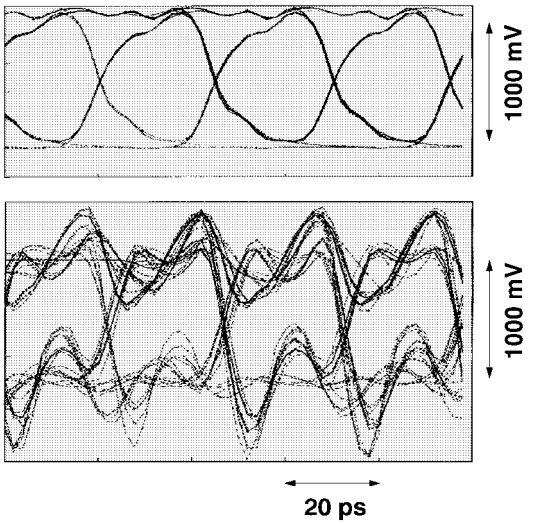

Fig. 11. Simulated eye diagrams at the data input node of the selector core circuit for 40-Gbit/s PRBS data. Upper: high-speed interconnection; lower: conventional.

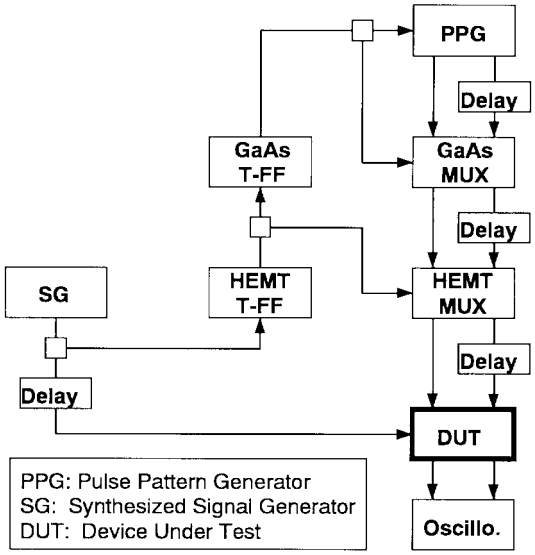

Fig. 12. Measurement setup.

IV. Experimental Results

A. Measurement Setup

The fabricated chips were first measured on a wafer with dedicated 40-GHz bandwidth multiple contact probe heads. The measurement setup is schematically shown in Fig. 12. A complimentary pair of fundamental pseudorandom data streams (PN $2^{23}-1$) of up to 10 Gbit/s were generated from a pulse pattern generator (PPG). These were quadrupled using a GaAs MESFET 2:1 MUX unit and a HEMT 2:1 MUX module [1]. A pair of final bit-rate signals were input into the IC under measurement, with an appropriate delay for each.

A master clock signal (up to 40 GHz) for the IC under test was generated by a synthesized signal generator. All the other clock signals (the half-rate clock for the HEMT MUX module and the quarter-rate clocks for the PPG and the GaAs MUX unit) were generated from the master clock using HEMT and GaAs MESFET T-FF's [12], [18]. This clock distribution

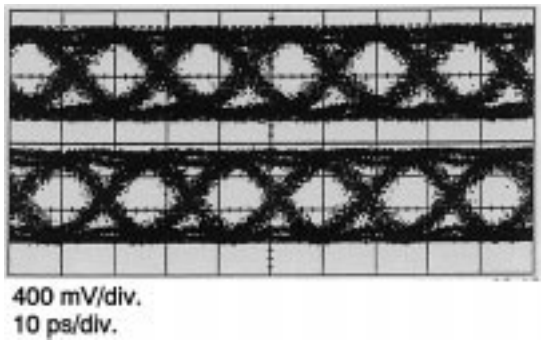

Fig. 13. Output eye diagrams at 60 Gbit/s. Upper: OUT; lower: /OUT.

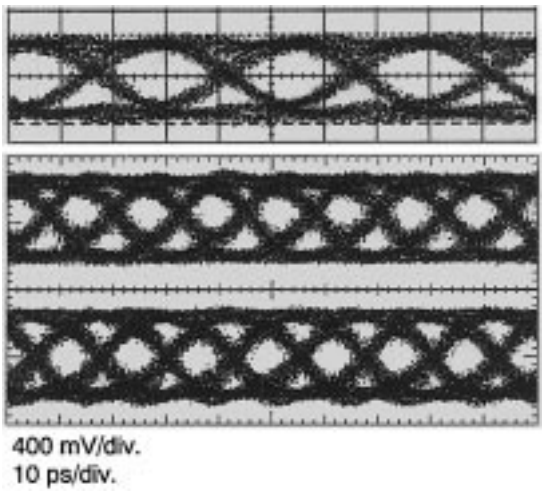

Fig. 14. Output eye diagrams at 80 Gbit/s. Upper: Input data; middle: OUT; lower: /OUT.

scheme with a single clock source is the key to performing stable, low-jitter measurements at such high bit rates. The complimentary outputs of the MUX IC were monitored with a 50-GHz bandwidth digitizing scope, HP 54123-T, by way of 50-cm long, 40-GHz bandwidth coaxial cables.

B. Results and Discussion

First, we performed the go/no-go test for all the chips by measuring the output eye opening at 60 Gbit/s. The yield was 48% for the best wafer. A typical measured eye pattern of the MUX IC output at 60 Gbit/s is shown in Fig. 13. A very clear eye opening was obtained. The voltage swing was 1100 $mV_{p\text{-}p}$, which is sufficient for an SCFL interface. Error-free operation of the MUX IC was as good as expected.

Because of the measurement instrumentation limit, bit error rate (BER) measurement cannot be performed with stability at bit rates of beyond 46 Gbit/s. So, we measured the BER's for those MUX IC's at 40 Gbit/s. The MUX output was first demultiplexed into two channels of 20 Gbit/s by using a HEMT 1:2 demultiplexer module [19] and further demultiplexed into four channels of 10 Gbit/s by using Si bipolar D-FF's and were then introduced into an error detector (channel by channel). Error-free operation (bit error rate $<10^{-10}$) was confirmed for all four channels of 10-Gbit/s data.

We attempted to measure the maximum operating speed for some chips. Fig. 14 shows a typical measured eye pattern of

a MUX IC at 80 Gbit/s. Although an insufficient bandwidth of the measurement instruments degrades the transition speed on the waveform, its eye opening is still clear. The rise and fall times of 20–80% of the amplitude are about 9 ps for both, which corresponds to a −3-dB bandwidth of 40 GHz for the measurement instruments. Error-free operation is expected at this bit rate. Much higher-speed operation of near 100 Gbit/s is also expected.

The circuit speed improvement obtained over the previous report of 64 Gbit/s [10] owes much to the newly introduced high-speed interconnection technology. High-propagation-speed, low-characteristic impedance MSL's made using a double-layered metal interconnection process with a thick, low-dielectric insulation layer is indispensable in very high-speed digital IC design.

V. Conclusion

An 80-Gbit/s 2:1 selector-type multiplexer IC was developed using InAlAs/InGaAs/InP HEMT's incorporating a high-speed double-layer interconnection process with a low-permittivity insulator. MSL's were designed to make impedance-matched, high-speed intercell connection of critical signal paths by using the interconnection process. The characteristic impedance of MSL's can well match to the output impedance of the internal logic cells. This drastically reduces the waveform distortion caused by the impedance mismatch that critically limits circuit speed performance at data rates beyond 60 Gbit/s. The record operating data rate was measured on a 3-in wafer. In spite of the bandwidth limitation on the measurement setup, clear eye patterns were successfully observed for the first time. BER measurement at around 80 Gbit/s, which is currently limited to a level below 46 Gbit/s by measurement instruments, is a future subject. The circuit speed improvement obtained over the previous report of 64 Gbit/s owes much to the newly introduced high-speed interconnection technology. Real 100-Gbit/s electronic IC's will become a reality in the near future.

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