A picosecond-accuracy, 700-MHz range, Si-bipolar time interval counter LSI

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A Picosecond-Accuracy, 700-MHz Range, Si-Bipolar Time Interval Counter LSI

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Abstract—**This paper describes a picosecond-accuracy digital vernier-based single-chip time interval counter (TIC) LSI applicable to timing calibration in state-of-the-art high-speed LSI test systems. Jitter performance is improved to three times higher than in conventional circuitry by using a new skew detection circuit that is insensitive to the jitter caused by metastable transitions in flip-flops. All the hardware except the signal sources has been integrated on a Si bipolar 2.5K-gate array LSI by developing fully digitally processed beat-signal and trigger control circuits. The chip is mounted on a dedicated ceramic package employing coplanar lines with a 3-GHz bandwidth. Overall performance achieves 2.3-ps standard deviation, ±3-ps linearity, zero-skew offset of ±2.7 ps, and an equivalent input slew time of 33.6 ps/V at input clock rates up to 700 MHz.**

I. Introduction

RAPID progress in LSI technology has driven the chip operating speeds nearly to the gigahertz region [1]. There is, therefore, an urgent need for higher speed and accuracy in LSI test technology. In particular, for automatic test equipment (ATE) systems, test timing control with tens of picoseconds accuracy at around 500 MHz is a critical milestone [2]. In order to maintain such timing performance, the calibration hardware that measures the time interval between a marker clock signal and the target clock signals such as tester driver outputs needs subpicosecond resolution and picosecond accuracy (linearity and deviation) at operating clock rates from the minimum test rate of around 1 MHz to the maximum test rate. Therefore, the time intervals to be discussed in this paper range from 10^{-12} to 10^{-6} s.

The principal methods of time interval measurement in the subnanosecond regime were reviewed by Porat [3]. A time-to-digital converter technique, in which input signals are recorded to memory cells at a specific time interval, has been developed by Arai *et al.* [4], for use in nucleon time-of-flight measurement. However, its measurement resolution is limited to around 1 ns by the time resolution of delay lines used in the circuit. In principle, the advantage of near picosecond resolution is provided by a time-to-voltage conversion (TVC) technique, in which a converted voltage is measured by A/D converters, and also by a digital vernier technique, in which a short time interval is expanded by beat signals and then interpolated. Many TVC-based [5]–[8] and digital vernier-based [9]–[11] time interval measuring instruments and systems have already been developed in several application fields. However, obtained timing performance and input clock range did not meet the above target specifications in spite of their costly analog-based circuit configurations. Bottlenecks in achieving picosecond accuracy are: 1) the jitter due to the metastable transition in flip-flops used as the first-stage comparator, which increases the measurement deviation; and 2) waveform degradation due to multireflection and crosstalk along the transmission paths, which degrades the timing linearity.

This paper describes a digital vernier-based single-chip time interval counter (TIC) LSI with subpicosecond resolution, ±3-ps linearity, and 2.5-ps standard deviation operating at input clock rates of up to 700 MHz. A new skew detection circuit, which is insensitive to the metastable-dependent jitter, is implemented in the first stage. It includes a fully digitally processed beat-signal/trigger control circuit. This makes it possible to integrate all the hardware except the signal sources into a single-chip gate array. Its circuit features, LSI design, and performance will be described in detail.

II. Principle of Operation

The circuit block diagram is shown in Fig. 1(a) and an operation time chart is shown in Fig. 1(b). A pair of measured clock signals $S1$ and $S2$ with the same frequency (f_0) whose time interval is to be measured is input to the skew detection block. A reference clock RF whose frequency (f_R) is slightly different from $S1$ and $S2$ is also input to the skew detection block. In a real case of tester timing calibration, a marker clock signal may be introduced to $S1$ and one tester driver output may be introduced to $S2$. Output timings of all tester drivers are measured as the time intervals from the marker signal timing.

The skew detection block consists of the equivalent three skew detection circuits, $D1, D2$, and $D3$, which detect the skew between $S1$ and RF, $S2$ and RF, and $S1$ and $S2$, respectively. Thus, $D1$ and $D2$ yield the beat signals between $S1$ and RF and $S2$ and RF, respectively, whose periods are expanded from those of $S1$ and $S2\,(f_0)$ by the factor of $f_R/|f_0 - f_R|$. Therefore, the measured time resolution and beat frequency are given by $|f_0 - f_R|/(f_0 f_R)$ and $|f_0 - f_R|$, respectively. The polarity of the skew between $S1$ and $S2$ is obtained from $D3$, which is necessary for accurately processing the beat signals as described later.

The timing difference between the beat signals is equivalent to the multiplication of the time interval between $S1$ and $S2$ and the expanding factor of $f_R/|f_0 - f_R|$, so it can be digitized as a multiple (N times) of the input signal period $(1/f_0)$ by

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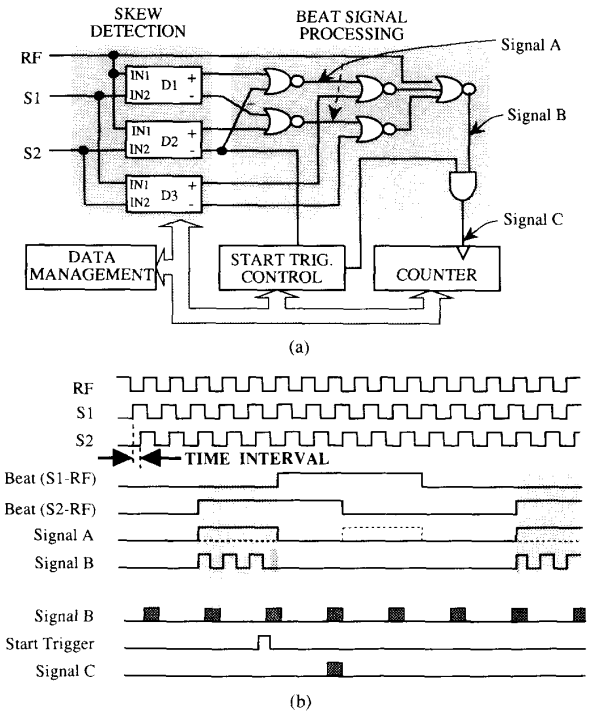

Fig. 1. Principle of time interval measurement: (a) circuit diagram and (b) time chart.

means of the beat signal processing, the start trigger control, and the counter blocks (see signal C in Fig. 1). Therefore, the time interval is given by $N|f_0 - f_R|/(f_0 f_R)$. A single measurement takes $|f_0 - f_R|^{-1}$ seconds. When the input clock frequency and resolution are set to 100 MHz and 1 ps, respectively, a single measurement takes only 100 μs.

The measurement accuracy is fundamentally limited by the frequency purity and the stability of the signal sources. Taking a millisecond-order measurement time with a picosecond resolution into account, a frequency stability of 10^{-9}/h and an SSB noise of -60 dBc/Hz at 20 Hz from the carrier frequency are required for picosecond accuracy. Many commercially available signal sources meet these specifications.

III. LSI Design

A. Process Technology

In order to achieve accuracy of the order of picoseconds and near-gigahertz operation, a high-speed Si bipolar process with a 15-GHz f_T called SST-1A [12] was used for the LSI fabrication. The transistor parameters are summarized in Table I. The physical dimensions of the internal circuit transistors used in this study are an emitter stripe of $0.5 \times 10.0\,\mu\text{m}^2$ and a double base electrode of $0.3 \times 11.5\,\mu\text{m}^2$ for each.

B. Skew Detection Circuit

A D-flip-flop-based latching comparator is generally used for detecting the skew between two repetitive clock signals [11], [13]. One target signal is input to the data port and

TABLE I
SST-1A Transistor Parameters

Symbol	Definition	Unit	Value
Is	Transport saturation current	aA	19
βf	Forward current gain	-	100
βr	Reverse current gain	-	14
τf	Forward transit time	ps	10.2
τr	Reverse transit time	ps	350
rb	Base resistance at non-bias	Ω	285
rc	Collector resistance at non-bias	Ω	68
re	Emitter resistance at non-bias	Ω	24
Cje	Base-emitter capacitance at non-bias	fF	17
Cjc	Base-collector capacitance at non-bias	fF	18
Cjs	Collector-substrate capacitance at non-bias	fF	47
Mje	Base-emitter junction grading factor	-	0.46
Mjc	Base-collector junction grading factor	-	0.38
Mjs	Collector-substrate junction grading factor	-	0.35
VAf	Forward Early voltage	V	15

the other is to the strobe port. However, the skew detection sensitivity becomes a critical factor in achieving picosecond sensitivity. This is because the sensitivity is substantially limited by the metastable transition width of the flip-flop as follows. Let's define the skew detection sensitivity τ_s as the time span necessary for passing through the metastable transition by sweeping the strobe or data input timing, and suppose the change in the collector node voltage of the flip-flop corresponding to the metastable transition width as V_{height}, which is comparable to the thermal voltage. According to the delay approximation for bipolar transistors by Yang and Chang [14], where the base current of the data input transistor is treated as a linear function, τ_s for the conventional circuit is obtained analytically as follows:

$$\tau_s = (2V_{\text{height}}/\phi)[2\tau_f r_b \tau_{\text{slew}}(\phi + V_{\text{height}})/(R_C\phi)]^{1/2} \quad (1)$$

where $\tau_f, r_b, \tau_{\text{slew}}, R_C$, and ϕ are the transistor forward transit time, the transistor base resistance, the input slew time, the collector load resistance, and the logic swing, respectively. Substituting practical values for these parameters, $\tau_f = 10.2$ ps, $r_b = 285\,\Omega, \tau_{\text{slew}} = 200$ ps, $R_C = 650\,\Omega, \phi = 400$ mV, and $V_{\text{height}} = 26$ mV, the detection sensitivity is calculated to be no less than 4.5 ps, which is not acceptable.

A new skew detection circuit is proposed here. The circuit block diagram and operation time chart are shown in Fig. 2(a) and (b). First the voltage levels of the two signals are normalized in the level converter (LVC) block. The second block (DEF) is the key and differentially amplifies the voltage difference caused by the timing skew. The voltage difference is input to the complementary D-latch (LATCH). Meanwhile, the strobe pulse is generated in block (SB) synchronously with the rising edges of one of the input signals, and input to the latch. Therefore, the output levels of Q and $\overline{Q}$ are fixed to complementary logical levels according to the skew polarity.

This circuit has the advantage that an in-phase skew can be successfully transformed to the differential voltage amplitude even for a very small skew, because the voltage difference is maintained at least during an input signal slew time of about 200 ps. Thus, the differential voltage can be maintained during the latch strobe timing by optimizing the strobe pulse width and timing. Consequently a very small in-phase skew can be detected as shown in Fig. 2(b). Since the voltage gain of the

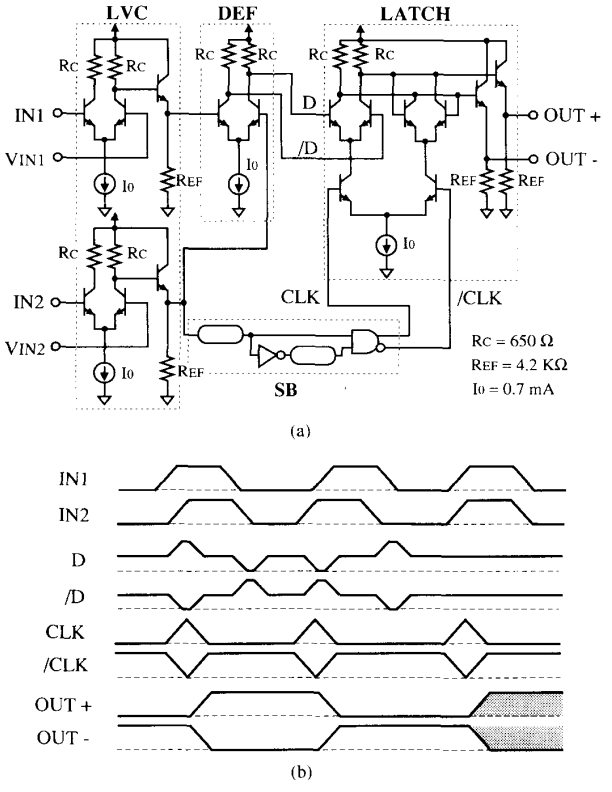

Fig. 2. New skew detection circuit: (a) circuit diagram and (b) time chart.

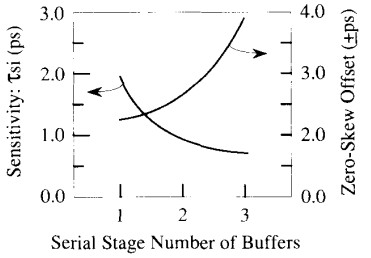

Fig. 3. Simulated results for the dependence of the in-phase skew detection sensitivity and the zero-skew offset on voltage gain. The zero-skew offset was calculated as the maximum deviation of zero-skew timing under the condition of ±0.5% device parameter deviation and ±50-mV input signal offset. The gain is controlled by the serial stage number of differential I/O buffers.

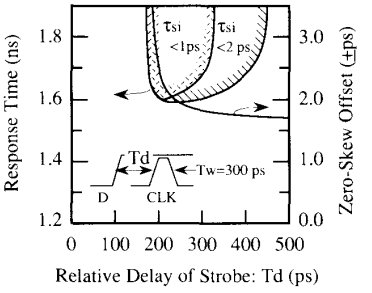

Fig. 4. Simulated results for the dependence of the response time and the zero-skew offset on strobe timing. A process deviation of ±0.5% and an input signal offset of ±50 mV are assumed The parameter is attainable skew detection sensitivity. The hatched areas show the stable operation regions that can achieve <1- and <2-ps skew detection sensitivity, respectively.

differential amplifier is given by the product of R_C and the transconductance g_m, the in-phase skew detection sensitivity τ_{si} is given by

$$\tau_{si} = V_{\text{height}}\tau_{\text{slew}}/(g_m R_C \phi). \tag{2}$$

This indicates that τ_{si} is insensitive to the metastable transition. g_m can be assumed to be as follows under the zero-skew condition,

$$g_m = \beta_f q I_0/[kT(1+\beta_f)] \tag{3}$$

where β_f, q, I_0, k, and T are the forward current gain, the electron charge, the gate current, Boltzmann constant, and absolute temperature, respectively. Therefore, for a practical case of $g_m = 27$ mS ($I_0 = 0.7$ mA, $T = 300$ K), τ_{si} is estimated to be 0.8 ps.

On the other hand, the differentially transformed voltages for an out-phase skew are interchanged in their polarity during the latch strobe timing, and their transient speeds are limited by the transistor speed, which is the same as the conventional circuit. This results in a comparable detection sensitivity to the conventional circuits. Thus, the out-phase-skew-dependent information is not utilized for skew data processing as shown later.

The factors that determine τ_{si} are 1) the voltage gain, 2) the strobe pulse width, 3) the strobe timing, 4) process variance, and 5) systematic disturbance such as input signal offset, jitter, and noise. Then the first three factors are optimized by using SPICE simulation taking a certain tolerance in the last two factors into account. In the LSI design, relative deviations of ±0.5% for the device parameters and of ±50 mV for the input signal offset were assumed. A low-jitter design technique described in [15] was also applied. Fig. 3 shows the simulated results for the dependence of τ_{si} and the detection accuracy due to factors 4 and 5 on voltage gain. The detection accuracy was calculated as the maximum deviation of zero-skew timing under the condition of ±0.5% device parameter deviation and ±50-mV input signal offset. The voltage gain was controlled by the serial stage number of differential input/output buffers. By taking the product of τ_{si} and the detection accuracy as a figure of merit, the serial stage number of two was selected. A strobe pulse width of 300 ps was adopted with a good margin.

Fig. 4 shows the simulated results for the dependence of the response time in the latch on strobe timing. The parameter is possible detection sensitivity τ_{si}. Because of asymmetrical stability regions against the strobe timing, which is caused by asymmetrical rise/fall edges at the outputs of the differential buffer gate, the design center for the strobe timing is slightly shifted to the larger point of 300 ps. From this figure, maximum operating frequencies of 625 and 600 MHz are expected for 2- and 1-ps sensitivities, respectively.

The first prototype fabrication used a standard ECL-to-LCML interface buffer for the level converter circuit. This permits input signal levels in the range from −2.0 to 0.0 V. The input voltage offset of the buffer, which causes a zero-skew timing offset, was not adjusted. With regard to the

process deviation, a peak-to-peak offset voltage of ± 5.5 mV (as a six-time standard deviation value) and its temperature coefficient of $8\,\mu V/°C$ are estimated [16]. This would result in a zero-skew timing offset of ± 1.8 ps with a temperature drift of 2.4 fs/°C, which would be acceptable.

C. Beat Signal Processing Circuit

The beat signal processing block alternately extracts the phase difference of the rising or falling part between beat signals as shown in Fig. 1(a) and (b). The former occurs at the in-phase skew transition where the rising edge of $S1$ or $S2$ overlaps the rising edge of RF. The latter is made by the out-phase skew transition where the rising edge of $S1$ or $S2$ overlaps the falling edge of RF. The amount of both of those phase differences is logically equivalent to the multiplication of the time interval between $S1$ and $S2$ and the expanding factor of $f_R/|f_0 - f_R|$. However, their repeatability and accuracy are due to the detection sensitivity of the skew detectors. In order to minimize the measurement deviation, only the phase information made by the in-phase skew transition having higher detection sensitivity is extracted as shown in Fig. 1(a) and (b). For experimental use only, the phase information made by out-phase skew transition can be extracted by a mode selection as described in Section IV. The input signal RF is enabled to clock the counter during the extracted time (see signal A in Fig. 1). In the case of the counter, a 20-b binary counter was configured to give a dynamic range of 6 decades for the time interval range. An 8-b I/O bus was provided to manage all the data read/write control from outside the chip.

D. Edge-Count Trigger Circuit

The start trigger control block passes the clock input to the counter block only for a single cycle of the beat signal after the start command is asserted (see signals B and C in Fig. 1(b)). When the time resolution is comparable to the jitter of an input signal and the circuit, random chattering will occur around the rising and falling edges. Therefore, low-pass filtering is necessary for stable triggering by sensing the intrinsic edge of the beat signal. However, conventional low-pass filtering using analog circuits degrades the edge rate according to the cutoff frequency, which results in a large measurement deviation, and is not adequate for integrating on a gate array LSI.

In this work, a fully digitally processed edge-count trigger circuit was specially developed. Its circuit configuration and operating time chart are shown in Fig. 5(a) and (b). This circuit employs two counters CT1, CT2 and edge sensor logics ES1 and ES2. CT1 and ES1 are assigned to rising edge detection, and CT2 and ES2 are assigned to falling edge detection. Initially a count value that is sufficiently larger than the chattering count in a single beat period is set to each counter. When the start signal is asserted, the counter CT1 starts to count down the edge sense signal from ES1 until borrowing. Then the second counter CT2 is triggered to count down the edge sense signal from ES2 until borrowing. At this moment, the gate signal is enabled. After one more recursive operation, the gate signal is disabled until the next start requirement. Consequently a stable trigger operation can

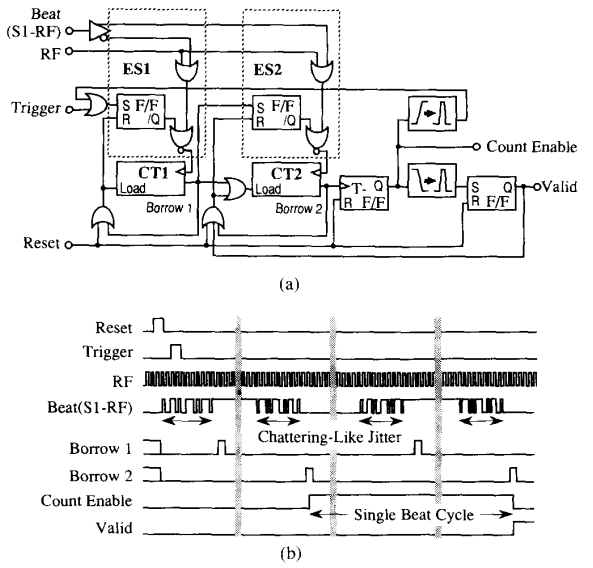

Fig. 5. (a) Block diagram and (b) time chart of a fully digitally processed edge-count trigger circuit.

be successfully performed. The counter bit was designed to be 8, which permits about 250-ps total jitter for a 1-ps resolution.

E. Layout and Packaging

The whole circuit was laid out with about 3000 transistors on an SST 2.5K-gate array chip [17]. The skew detection block was isolated from the other digital blocks so as not to share the power and reference-level mother lines. This could help to minimize the crosstalk-dependent error. In particular, the differentially operating circuit elements and interconnection lines, including their crossover along the critical paths, were symmetrically laid out in order to minimize the process-dependent deviation in device parameters. The total power dissipation of the fabricated chip was 3200 mW for a power supply voltage of V_{CC} (= GND) − 3.3 V.

The chip was mounted on a dedicated ceramic substrate. The top view of the package is shown in Fig. 6. It consists of a thin film on top of seven-layer thick films with a cavity for mounting the chip. In order to reduce multireflection-dependent and crosstalk-dependent errors while maintaining low insertion loss, a grounded coplanar structure was used for the input signal lines. Each coplanar line is fed through the die pad, which allows the module to be used in time-domain reflectometry (TDR) applications [18]. The other data and control lines were made by a microstrip structure. Microchip bypass capacitors were bonded at the lands on the thin film for stabilizing power planes and reference signal lines. Minimizing the bonding wires of the input lines is another key to reducing the impedance mismatch. This could also help to reduce the zero-skew timing error. The module was carefully designed and assembled as follows:

1. the surface of the die was aligned to that of the substrate by designing the cavity depth equal to the die height;
2. the die was bonded on the cavity so that it approached the input side as much as possible.

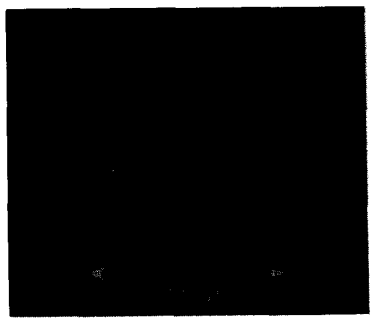

Fig. 6. Top view of the time interval counter module before sealing with a cap.

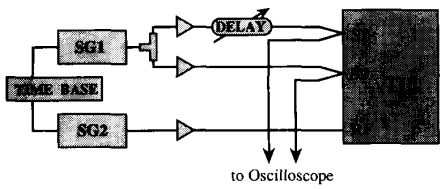

Fig. 7. Measurement setup.

Transmission characteristics for the grounded coplanar feedthrough paths were measured. An insertion loss of -1 dB, a return loss of <-15 dB, and an isolation of <-45 dB were obtained at frequencies up to 3 GHz.

IV. Results and Discussion

A. Measurement Setup

Timing performance was evaluated for the fabricated samples. The measurement setup is shown in Fig. 7. The signal sources were synthesized signal generators (SG's) with <-80 dB, <-120 dB of SSB noise at 20 Hz, 1 kHz from the carrier frequency. Two of the SG's were synchronized by a single high-stability time base consisting of a temperature-controlled quartz crystal oscillator. These outputs were reshaped to rectangular waves by SST buffer gates and then input to the modules. Time jitter of the output signal had a standard deviation of 1.2 ps. One of the SG outputs was split into two paths. One path was directly connected to $S1$, and the other was connected to $S2$ through a variable delay line with less than 1-ps linearity error. The other end of each feedthrough path was connected to a sampling head (HP54123T) and monitored. Care must be taken because the sampling oscilloscope has a linearity error of around ± 10 ps due to a nonlinearity of its triggered delay control circuitry. Therefore, the error was precisely measured by means of a sophisticated technique based on a regression analysis [19]. By using the SG output signal as a frequency standard the time axis error was calibrated to within ± 2 ps beforehand. The measured time axis error is shown in Fig. 8.

B. Jitter and Deviation

In order to evaluate the intrinsic jitter of the module itself, the deviation of the measured data was monitored while changing the vernier resolution $|f_0 - f_R|/(f_0 f_R)$ from 5 ps to 500 fs. A typical result obtained at an input clock rate of 500 MHz is shown in Fig. 9. The data for conventional skew detector circuitry, which is obtained by selecting out-phase skew information as described in Section III-B, are also plotted. The measurement deviation for this work is saturated to 2.3 ps while that for the conventional approach is to 6.2 ps. The inset shows a Gaussian-like distribution of measured data at an 800-fs vernier resolution for the new circuit. Taking the input signal jitter of 1.2 ps into account, the intrinsic rms jitters of new and conventional circuits are estimated to be 1.96 and 6.1 ps, respectively. These results agree well with the analytical estimation described in Section III. The tolerance of accumulated averaging data shows that averaging over 30 measurements can produce repeatability of less than ± 700 fs. This performance was maintained up to a maximum clock rate of 700 MHz. The vernier resolution was fixed at 800 fs in the following experiments. (The jitter caused by the LSI itself is estimated to be 2.31 ps.)

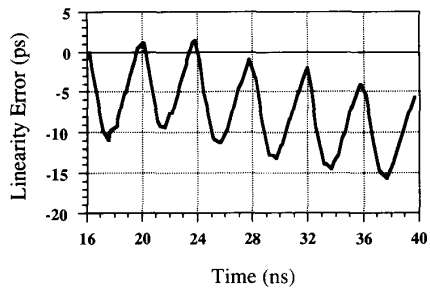

Fig. 8. Time axis linearity error of the digitizing oscilloscope.

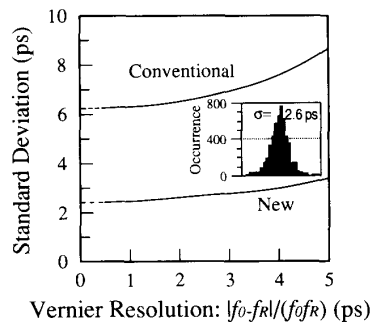

Fig. 9. Deviation of measured data as a function of the vernier resolution, obtained from conventional and new circuits for an input signal amplitude of 1000 mV and a clock rate of 500 MHz. The inset shows the Gaussian-like distribution of measured data obtained from the new circuit at a vernier resolution of 800 fs.

The above-mentioned stable operation is maintained for threshold levels ranging from 10% to 90% of the input signal amplitude. The dependence of the standard deviation on amplitude, obtained for a 50% threshold level, is shown in Fig. 10. A minimum amplitude of 200 mV was detected. This limit seems to depend on the total gain of the level converter and cascaded differential amplifiers.

C. Linearity

The linearity depends strongly on the input signal rise time and the transmission bandwidth. Regarding the obtained

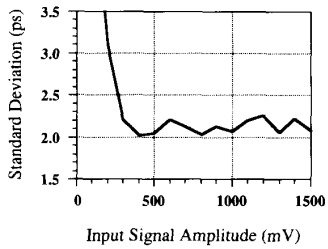

Fig. 10. Dependence of measurement deviation on amplitude for an input signal amplitude of 1000 mV and a clock rate of 500 MHz. The threshold level is set to be 50% of the input level.

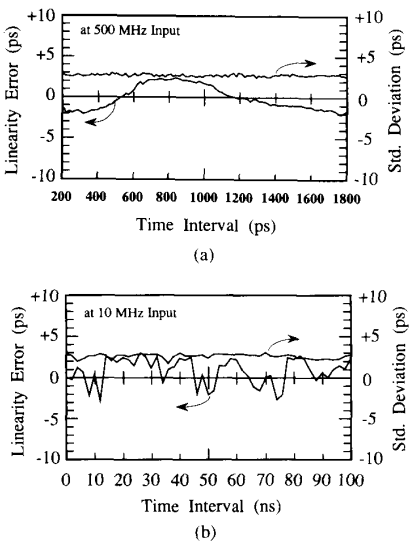

Fig. 11. Measured timing linearity obtained at an input clock rate of (a) 500 MHz and (b) 10 MHz.

transmission bandwidth of 3 GHz along the input coplanar lines, an input signal having a rise time of 300 ps/V was used. Typical linearity error obtained at an input clock rate of 500 MHz is shown in Fig. 11(a) where the time intervals are measured with a 1.0-ps step over a 1800-ps range. Good linearity of less than ± 3 ps is achieved. The linearity for a long time interval of 100 ns was also measured where the time interval between the 10-MHz input signals was digitally swept with a 2-ns step by using a vector generation function of a 500-MHz VLSI test system [20]. The results shown in Fig. 11(b) indicate that the linearity is maintained within ± 3 ps. From the above results, it is considered that the systematic error due to multireflection and crosstalk can be successfully suppressed in a bandwidth of 3 GHz.

D. Zero-Skew Offset

The zero-skew timing was evaluated for 20 fabrication samples by sweeping the time interval between the two inputs. The distribution of the zero-skew timing is shown in Fig. 12. This result was obtained under typical conditions of $V_{EE} = -3.3$ V and a package temperature of 47.0°C, but it was only slightly sensitive to V_{EE} and temperature as had been

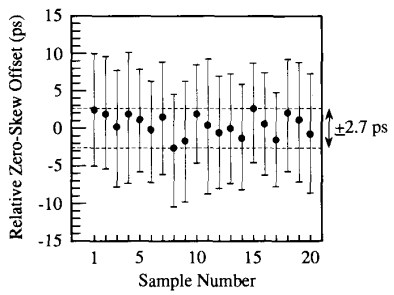

Fig. 12. Distribution of zero-skew timing among 20 samples for an input signal amplitude of 1000 mV and a clock rate of 500 MHz. The error bars indicate the peak-to-peak distribution ranges of 5000 measurements for each. The dots indicate the averaged values.

expected. The distribution of averaged zero-skew timing has a peak-to-peak deviation of ± 2.7 ps, which is slightly larger than the estimated value of ± 1.8 ps. This is believed to be a reasonable result considering assembly variations such as bonding wire length. As a further improvement, tab bonding instead of wire bonding promises a near-picosecond zero-skew offset without extra treatment of voltage offset reduction for the input buffers as in [16] and [21].

E. Response Time

The response time of the input-stage circuit depends on the input signal slew time, the threshold offset, and the input signal amplitude. These response delay characteristics are attributed to the speed performance of the transistors used in the circuit. This causes a timing offset in the time interval measurement for input signals having different values of these parameters.

Fig. 13(a) shows the dependence of the response time on threshold offset. The parameter is input signal rise time. The relative response delay for an input having slower slew time of 112 ps/V is negligibly small. For a faster 37-ps/V slew-time input, however, a response delay of 13 ps is seen among the threshold offsets from 20 to 80% of the input signal level. From these results, the system bandwidth of the time interval counter can be expressed as an equivalent input rise time of 33.6 ps $(= \sqrt{50^2 - 37^2})$. This must be considered when the module is used for slew time measurement such as for precise TDR measurement [18].

Fig. 13(b) shows the dependence of the response time on the input amplitude. A relative response delay from +28 to -13 ps was observed for input signal amplitudes of 1000 ± 800 mV. Because of the monotonic dependence of the response time on input amplitude, it could be easily compensated for by using linear error modeling [22]. It is concluded from the response characteristics that only the dependence of the response delay on amplitude must be taken into account when the module is used for timing calibration in state-of-the-art LSI test systems, since their slew times are larger than 100 ps/V.

V. Conclusions

A digital vernier-based single-chip time interval counter LSI was developed by using Si bipolar SST-1A technology. A novel skew detector circuit insensitive to the jitter due to

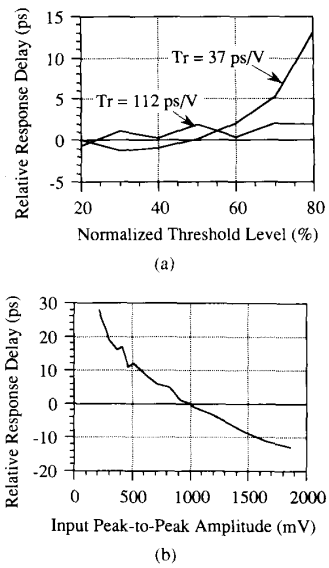

Fig. 13. (a) Response time versus threshold level. The parameter T_r is the input signal slew time. (b) Response time versus input signal amplitude.

the metastable transition of flip-flops was implemented. By optimizing the design parameters (gain, strobe timing, and strobe pulse width), a 2-ps rms jitter was successfully obtained, which was one third of conventional circuits. All the hardware except the signal sources were integrated on a 2.5K-gate array LSI by developing fully digitally processed beat-signal and trigger control circuits. The fabricated chip was mounted on a dedicated ceramic package employing coplanar lines with a 3-GHz bandwidth. The results are as follows: total performance of 2.3-ps standard deviation, ±3-ps linearity, zero-skew offset of ±2.7 ps, and equivalent input slew time of 33.6 ps/V at input clock rates up to 700 MHz. For use in ATE calibration with near-picosecond accuracy, the dependence of the circuit response time (about 20 ps/V) on input signal amplitude should be compensated for. In conclusion, the LSI circuit and design technologies proposed and demonstrated here can achieve picosecond accuracy time interval measurement with nearly 1-GHz bandwidth.

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