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A Novel High-Speed Latching Operation Flip-Flop (HLO-FF) Circuit and its Application to a 19-Gb/s Decision Circuit Using a 0.2-μm GaAs MESFET

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***Abstract*—This paper describes a novel high-speed flip-flop circuit named the High-speed Latching Operation Flip-Flop (HLO-FF) for GaAs Low-power Source-Coupled FET Logic (LSCFL). We reveal the high-speed operation mechanism of the HLO-FF using newly proposed analytical propagation delay time expressions. A design methodology for series-gated master slave flip-flops and HLO-FF's based on these expressions is also proposed. A SPICE simulation and the fabrication of two decision IC's confirm the accuracy of our analytical method and the high-speed operation of a HLO-FF decision circuit at 19 Gb/s.**

I. Introduction

THE transmission capacity of optical communication systems is rapidly increasing. A 10-Gb/s system has been demonstrated, and transmission experiments at 20 Gb/s have been reported [1], [2]. In transmission systems, the decision circuit is one of the key electronic components to regenerate or demultiplex the received signal. In particular, the flip-flop circuit is the most important fundamental circuit because it governs the speed performance of SSI and MSI such as decision circuits, multiplexers, and demultiplexers. In order to realize above 10-Gb/s decision IC's, very high f_T and $f_{\max}$ are required. For example, it is predicted that f_T and $f_{\max}$ must be 200 GHz to realize a 40-Gb/s D-type Flip-Flop (D-FF) using GaAs MESFET's [3]. Therefore, circuit design and circuit configuration technology to reduce these requirements for device parameters become more important as well as advanced device technology.

We previously proposed the High-speed Latching Operation Flip-Flop (HLO-FF) for GaAs Low-power Source-Coupled FET Logic (LSCFL) in high-speed IC applications and experimentally confirmed that the T-type HLO-FF operated approximately 30% faster than a conventional master-slave flip-flop (MS-FF) using 0.2-μm GaAs MESFET technology [4]. However, its application to decision circuits was not demonstrated, and the mechanism of the high-speed operation was explained qualitatively. In order to develop ultrahigh-speed circuits, we must clarify the relationship between device parameters and circuit performance, and develop a circuit design methodology to extract maximum circuit performance. Analytical delay time expressions are suitable for this purpose because they give intuitive understanding of the relationship between device parameters and circuit performance. The analytical delay expression of the GaAs LSCFL inverter has been reported [5]. However, that for flip-flop circuits has not been reported.

First, we describe the HLO-FF decision circuit characteristics. We then propose analytical delay time expressions for the GaAs LSCFL flip-flop circuit. Using the expressions, we reveal the high-speed operation mechanism and develop a circuit design methodology to optimize circuit performance. We simulate the maximum toggle frequency of the T-type flip-flop to confirm the accuracy of the proposed expressions. Furthermore, in order to verify the proposed design methodology and consider the application of the HLO-FF to high-speed decision circuits, a dynamic and a static decision IC's are fabricated as 0.2-μm GaAs MESFET's. We also describe the experimental results.

II. HLO-FF Circuit Configuration

Figs. 1 and 2 show the MS-FF and HLO-FF circuit diagram for LSCFL GaAs FET Logic, respectively. The important difference between the MS-FF and the HLO-FF is the combination of second-level FET's in the series gate circuits. The series-gate connection in HLO-FF separates the current paths of the reading and latching circuits, so the switching currents of the reading and latching circuit can be designed individually.

Fig. 3 shows the SPICE simulation results of the operating speed of the HLO-FF decision circuit versus gate-width ratio for reading and latching circuits. The simulation used the device parameters of a 0.2-μm GaAs MESFET. The maximum operating speed increases as the gate-width of the latching circuit decreases. On the other hand, the minimum operating speed increases at gate-width ratios under 0.4. The HLO-FF decision circuit operates as a static flip-flop circuit at gate-width ratios from 0.4 to 1.0 and as a dynamic flip-flop circuit at gate-width ratios under 0.4. The circuit operating region can be optimized from completely dynamic operation (0.0

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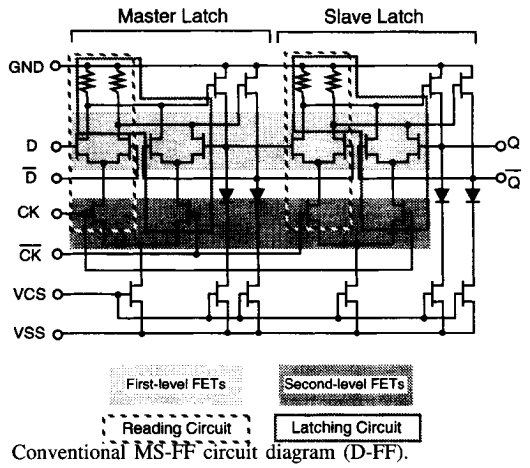


Fig. 1. Conventional MS-FF circuit diagram (D-FF).

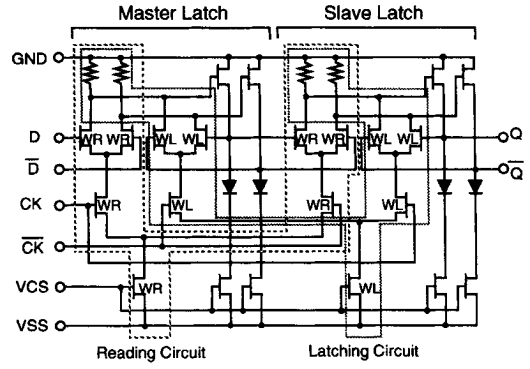


Fig. 2. HLO-FF circuit diagram (D-FF).

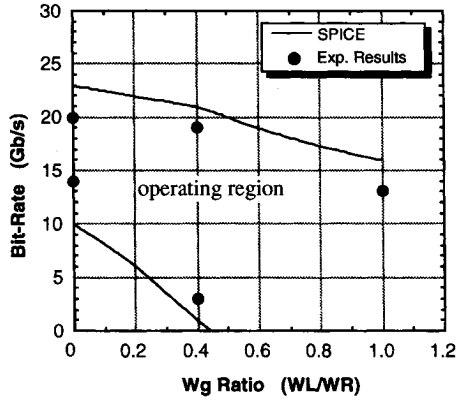


Fig. 3. SPICE simulation and experimental results of the operating speed of the HLO-FF decision circuit versus the gate-width ratio for reading and latching circuit.

gate-width ratio) to completely static operation (1.0 gate-width ratio) by adjusting the gate-width of the latching circuit. Here, the dynamic flip-flop (0.0 gate-width ratio) has the circuit configuration that removes the latching circuit from the HLO-FF [6]. The circuit diagram is shown in Fig. 4.

The HLO-FF has the characteristics of high-speed and a wide operating region. For example, the maximum operating speed of the HLO-FF at the gate-width ratio of 0.4 is only

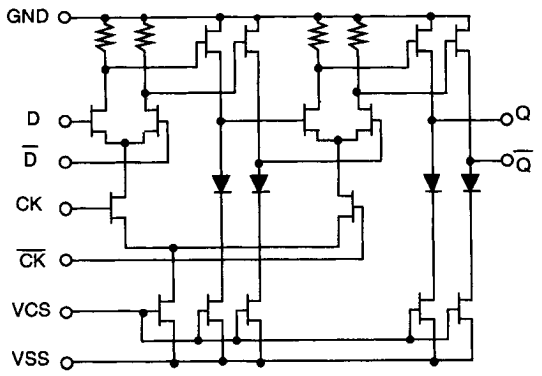


Fig. 4. Dynamic flip-flop circuit diagram (D-FF).

10% lower than that of the dynamic flip-flop as shown in Fig. 3. On the other hand, its operating region is approximately one and a half times that of the dynamic flip-flop. Therefore, the HLO-FF is more feasible for practical high-speed IC devices because it offers high yield against process variation due to its wide operating region.

III. Analytical Delay Time Expressions

A. Conventional MS-FF

In order to introduce a set of analytical delay time expressions for a conventional GaAs LSCFL MS-FF, the following three points are assumed:

1) the delay time of MS-FF is governed by the delay time of the first-level circuit,
2) the total delay time is expressed as the sum of those for switch part and source follower part, and
3) the input of the latching circuit is biased by the average level of the flip-flop output logic level, $Vref$.

Fig. 5(a) shows the equivalent circuit from the first assumption. Furthermore, Fig. 5(b) shows the equivalent circuit based on all three assumptions. These show an MS-FF master latch, which consists of a switch part and a source follower part. CL is the total input capacitance loaded on the source follower. Therefore, CL is the sum of the input capacitance of the reading circuit of slave latch and that of the latching circuit of master latch. RS is the output resistance of the current source of the source follower. Fig. 6(a) and (b) shows the transistor level equivalent circuits. In these figures, suffix C, L, F refer to reading circuit, latching circuit, and source follower circuit, respectively.

According to the calculation method proposed by Asher [7], the propagation delay times (50%–50% delay) for the switch part $TDSW$ and source follower part $TDSF$ are given by

$$TDSW = \left[-\frac{d[A(s)/ds]}{A(s)}\right]_{s=0}$$

and

$$TDSF = \left[-\frac{d[B(s)/ds]}{B(s)}\right]_{s=0}. \quad (1)$$

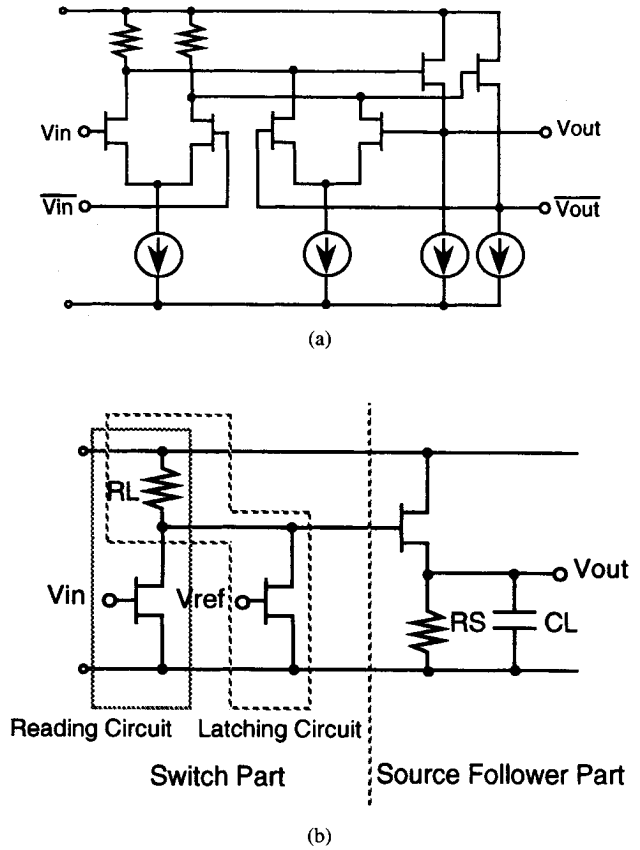


Fig. 5. (a) Flip-flop equivalent circuit from the first assumption (master latch). (b) Flip-flop equivalent circuit (master latch).

Here, $A(s)$ and $B(s)$ are transfer functions for the switch part and source follower part, respectively. These transfer functions can be introduced by solving the circuit equations for Fig. 6(a) and (b), so that $TDSW$ and $TDSF$ are expressed as follows. (The introduction of these transfer functions is given in the Appendix.)

$$TDSW = \frac{Cgd(C)}{gm(C)} + [Cgd(C) + Cgs(C)] \cdot Rg(C) + \{[Cgd(C) + Cds(C) + Cgd(L) + Cds(L)] \cdot RL + Cgd(C) \cdot gm(C) \cdot Rg(C) \cdot RL\} / \{1 + [gds(C) + gds(L)] \cdot RL\}. \quad (2)$$

$$TDSF = Cgd(F) \cdot [RL + Rg(F)] + Cgs(F) \cdot \left\{ RL + Rg(F) + \frac{1 - gm(F) \cdot [RL + Rg(F)]}{\left[gm(F) + gds(F) + \frac{1}{RS}\right]} - \frac{1}{gm(F)} \right\} + \frac{CL + Cds(F)}{gm(F) + gds(F) + \frac{1}{RS}}. \quad (3)$$

Here, we assume that gm, Cgs, and Cgd depend on bias voltages and that the other parameters are constant [5]. Gate capacitances are approximated by the following equation:

$$Cgi = Cpi + \frac{\int_{Vgi1}^{Vgi2} Cgi0 \cdot \left(1 - \frac{V}{\phi}\right)^{-m} dV}{Vgi2 - Vgi1} \quad (i = s \text{ or } d). \quad (4)$$

Here, suffix g, s, and d refer to gate, source, and drain, respectively. $Cgi0$, ϕ, m, and Cpi express the zero-bias capacitance, the built-in potential, the grading coefficient, and the parasitic capacitance which is independent of the bias voltage and gate-width, respectively. $Vgi1$ and $Vgi2$ are minimum bias voltage and maximum bias voltage fed to gate, respectively. The transconductances are approximated by average values and are given by

$$gm(C) = gmmax/2$$

and

$$gm(F) = gmmax. \quad (5)$$

The total delay time for the master latch circuit is expressed as follows using the second assumption:

$$tpd = TDSW + TDSF. \quad (6)$$

B. HLO-FF

Fig. 7 plots the waveforms of the HLO-FF circuit as the solid lines and those of the MS-FF circuit as the dotted line. From (6), the tpd of the HLO-FF is smaller than that of the MS-FF because of the decreased gate-width of the latching circuit. It is shown as the gray line in Fig. 7. However, in the HLO-FF, the logic swing on the latching operation period is shortened by the decreased switching current of the latching circuit. Therefore, the cross point of the differential signal is shifted forward further compared to that calculated from (6). The shift is shown as $\Delta t1$ in Fig. 7.

We approximated this cross point shift effect as a ramp signal response. The delay time of the HLO-FF, TPD can be expressed by the following equation:

$$TPD = tpd(HLO - FF) - \Delta t1 + \Delta t2. \quad (7)$$

Here, we consider parameter $\Delta t2$, which is the delay time due to the metastable transition width of the latching circuit ΔV. Using parameters α, β, and γ, which are defined by (9), TPD is rewritten to yield (8)

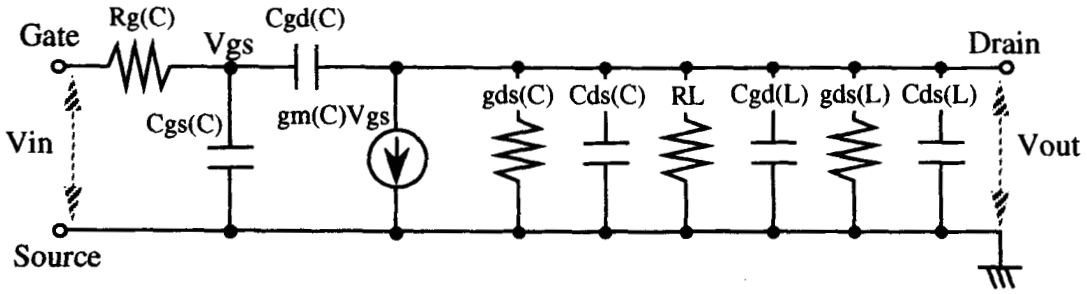
$$TPD = tpd \cdot \left\{ 1 + \frac{1}{\beta \cdot (1 - \alpha)} - \sqrt{1 - \frac{2 \cdot \gamma}{\beta \cdot (1 - \alpha)} + \frac{1}{\beta^2 \cdot (1 - \alpha)^2}} \right\} \quad (8)$$

$$\alpha = \frac{WL}{WR}$$

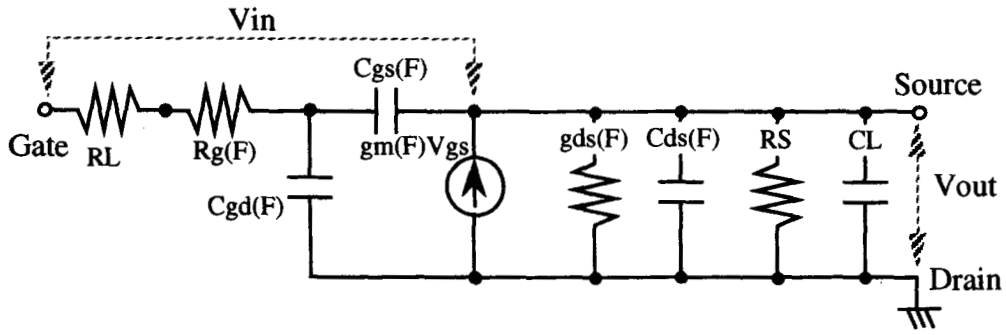
$$\beta = \frac{tpd}{Tdelay}$$

and

$$\gamma = \frac{\Delta V}{Vo}. \quad (9)$$



(a)



(b)

Fig. 6. (a) Switch part of flip-flop equivalent circuit. (b) Source follower part of flip-flop equivalent circuit.

Here, WR and WL are gate-widths for reading circuit and latching circuit, respectively, tpd is the delay time from (6), and Vo is the logic swing of reading circuit.

$Tdelay$ is the time constant of the low-level transition of the latching circuit over the latching operation period. Therefore, we assumed that $Tdelay$ is the propagation delay time from gate input of the second-level FET to drain output of the first-level FET whose gate is biased at constant voltage. Fig. 8 shows the equivalent circuit of latching circuit over latching period. From the equivalent circuit, $Tdelay$ is introduced based on the same procedure for tpd

$$Tdelay = \frac{[2 \cdot Cgd(L) + Cgs(L)]}{gm(L)} + [Cgd(L) + Cgd(C) + Cgd(F) + Cds(C)] \cdot RL. \quad (10)$$

C. Verification of Proposed Delay Time Expressions

In order to confirm the accuracy of these delay time expressions, we simulated the toggle frequencies of the T-type flip-flop circuit with no load. The device parameters at 10-μm gate-width for the SPICE simulation and propagation delay time calculations are shown in Table I. In the calculation, CL and RS were approximated by (11) and (12), respectively

$$CL = Cgs(L) + [1 + Av(L)] \cdot Cgd(L) + Cgs(C) + [1 + Av(C)] \cdot Cgd(C). \quad (11)$$

$$RS = 1/gds(F). \quad (12)$$

Here, Av is voltage gain. Furthermore, as the FET's have a symmetric structure, the parameters in (4) can be expressed by $Cgs0 = Cgd0 = Cg0$, $Cps = Cpd = Cp$. The toggle frequencies (f-$toggle$) were calculated by the following equation:

$$f\text{-}toggle = 1/2TPD. \quad (13)$$

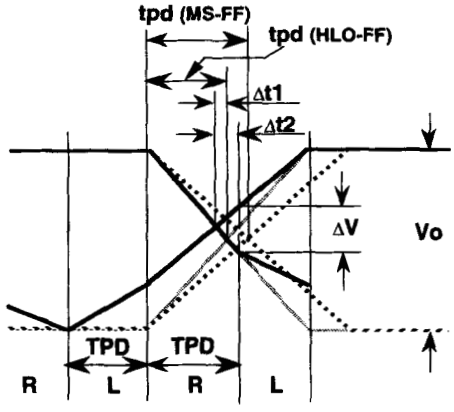


Fig. 7. Operating waveforms of MS-FF (dotted line) and HLO-FF (solid line). R: Reading Operation Period, L: Latching Operation Period, $\Delta t1$: Cross Point Forward Shift time, $\Delta t2$: Delay Time due to metastable transition width of Latching Circuit ΔV, tpd: Delay time of flip-flop circuit calculated from (6), TPD: Delay time of flip-flop circuit considering $\Delta t1$ and $\Delta t2$.

Fig. 9 shows the results from the SPICE simulation, (6) which considers propagation delay time, and (8) which considers the cross point forward shift effect. Toggle frequencies from proposed delay time expressions for MS-FF and HLO-FF agree with the SPICE simulation results within 10% error. This indicates that the high-speed operation of HLO-FF comes from not only the reduced parasitic capacitance due to transistor

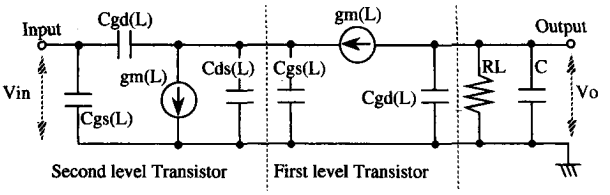


Fig. 8. Equivalent circuit of latching circuit for $Tdelay$ calculation.

TABLE I
DEVICE PARAMETERS (Wg = 10 μm)

Parameter	Value	Parameter	Value
gmmax	4.04 mS	ϕ	0.8 V
gds	0.3 mS	m	0.88
Cg0	6.5 fF	Cds	0.5 fF
Cp	1.0 fF	Rg	0.875 Ω

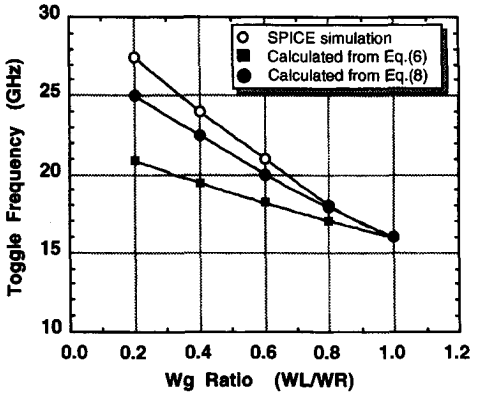


Fig. 9. Toggle frequency of the HLO T-FF with no load.

gate-width shortening in the latching circuit but also the cross point shift effect.

D. Circuit Design Methodology for MS-FF and HLO-FF

The MS-FF circuit design should optimize the two major parameters such as the product WR–RL and the ratio WR–RL. These parameters can be designed using the proposed analytical expressions with the following procedures. First of all, logic swing product WR–RL is designed to exceed the unity voltage gain of the differential circuit. The WR–RL ratio can then be optimized using (6). Fig. 10 shows the dependence of toggle frequencies on MS-FF gate-width calculated from (6) and a SPICE simulation. These results agree well, so the design methodology based on the proposed analytical delay time expressions are applicable to LSCFL MS-FF circuit design.

The HLO-FF circuit design should optimize one more parameter, the gate-width ratio of reading circuit and latching circuit (WL/WR) after MS-FF circuit design. This parameter impacts the maximum operating speed and minimum operating speed, which define HLO-FF operation as either dynamic or static. The maximum operating speed can be estimated using (8) as above mentioned. The minimum operating speed can be also estimated using (10) and ΔV with the assumption that minimum operation is realized when the logic swing of the latching circuit becomes less than ΔV.

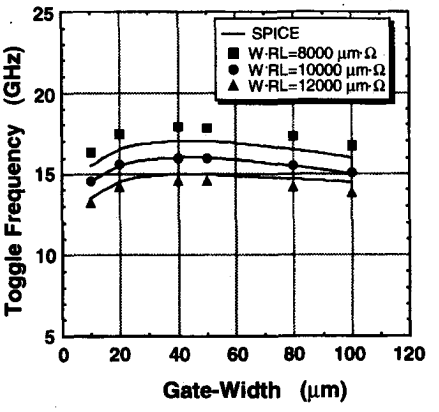


Fig. 10. Toggle frequencies of MS-FF from SPICE and (6).

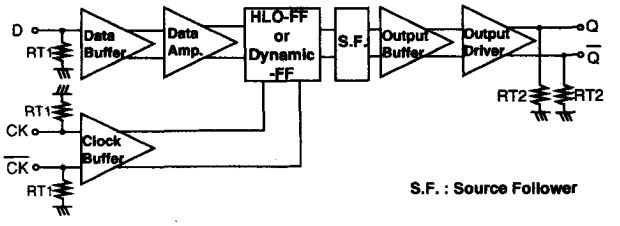


Fig. 11. Block diagram of decision circuit.

IV. CIRCUIT DESIGN AND FABRICATION

In order to confirm the proposed design methodology and the performance of the HLO-FF decision circuit, we fabricated a dynamic decision IC and a HLO-FF decision IC. The block diagram of the decision circuit is shown in Fig. 11. It consists of a data buffer, a data amplifier, a clock buffer, a flip-flop circuit, an output buffer, and an output driver. The difference between the dynamic decision IC and the static one is only the flip-flop circuit. Inputs and outputs were terminated to ground with 50 and 100 Ω on-chip resistors, respectively. The SCFL interface [8] was adopted for receiving clean waveforms and transmitting waveforms with fast rise/fall times. The power supply voltage was −3.5 V. The product $Wg-RL$ is designed for 10 000 μm·Ω to achieve proper switching with efficient voltage margin. The gate-width of the reading circuit was set at 50 μm from Fig. 10. The gate-width ratios of the dyanamic flip-flop and HLO-FF were 0.0 and 0.4, respectively.

These IC's were fabricated using the 0.2-μm gate length SAINT (Self-aligned Implantation for N^+ layer Technology) process [9] based on conventional optical lithography and ion implantation for easy implementation as commercial products. The typical cutoff frequency f_T for the 0.2-μm FET was 50 GHz, and the transconductance was 400 mS/mm. A microphotograph of the HLO-FF decision IC is shown in Fig. 12. The chip size is 2 mm × 2 mm.

V. EXPERIMENTAL RESULTS

These IC's were tested on-wafer with RF probes with a single phase clock signal fed to the clock input. A pulse pattern generator and an error detector were used for testing up to 10 Gb/s. Over 10 Gb/s, we used a GaAs MESFET selector module [10] for input data signal generation and a GaAs MESFET D-

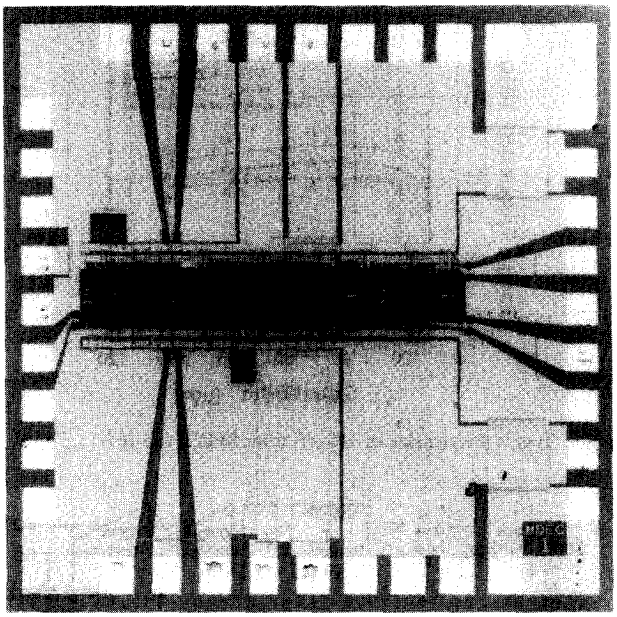


Fig. 12. A microphotograph of the HLO-FF decision IC.

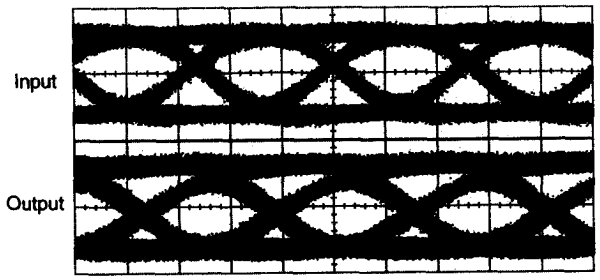


Fig. 13. Operating wave forms at 19 Gb/s.

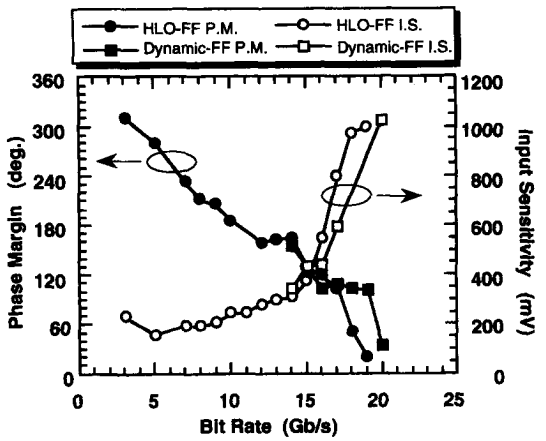


Fig. 14. Input sensitivity and phase margin of the decision IC's.

FF IC [11] for demultiplexing the output signal of the device under test. For these measurements, we adopted a word length of $2^{31} - 1$ PRBS signal and a bit error rate of less than 1×10^{-9}.

The dynamic decision IC and the HLO-FF decision IC stably operated from 14 Gb/s to 20 Gb/s and from 3 Gb/s to 19 Gb/s, respectively. These operating speeds were approximately 45% faster than the D-FF IC based on conventional MS-FF with the same MESFET's [11]. Fig. 13 shows operating waveforms of the HLO-FF decision circuit at 19 Gb/s. Good eye opening was obtained. Fig. 14 shows input sensitivity and phase margin of these IC's. The dynamic and static decision IC's dissipated 1.4 and 1.5 W, respectively.

Fig. 3 also shows experimental values and SPICE simulation results of decision circuit operating speed. The SPICE simulation results agree well with the experimental results. It indicates that our analytical method well models HLO-FF circuit operation.

VI. Conclusion

The high-speed operation mechanism of the HLO-FF is revealed by newly proposed analytical propagation delay time expressions for GaAs LSCFL MS-FF and HLO-FF. Its high-speed operation comes from not only reduced parasitic capacitance due to transistor gate-width shortening (latching circuit), but also the cross point shift effect. We also proposed a design methodology for MS-FF and HLO-FF using these delay expressions. The fabrication and testing of two types of decision circuit confirmed that our design methodology is applicable to flip-flop circuit design. In order to realize a high-speed decision circuit, we applied HLO-FF to the decision circuit. The static HLO-FF decision circuit using 0.2-μm GaAs MESFET's operated up to 19 Gb/s, which is approximately 45% faster than conventional static MS-FF with the same process. The HLO-FF is applicable to high bit rate decision IC's.

Appendix

From Fig. 6(a), circuit equations for the switch part are given by following equations:

$$vgs - vin + s \cdot Rg(C) \cdot Cgs(C) \cdot vgs + s \cdot Rg(C) \cdot Cgd(C) \cdot (vgs - vout) = 0. \quad \text{(A-1)}$$

$$vout + gm(C) \cdot RL \cdot vgs + [gds(C) + gds(L)] \cdot RL \cdot vout + s \cdot RL \cdot [Cds(C) + Cgd(L) + Cds(L)] \cdot vout + s \cdot RL \cdot Cgd(C) \cdot (vout - vgs) = 0. \quad \text{(A-2)}$$

From these equations, the transfer function $A(s)$ for the switch part is introduced as the following equation:

$$A(s) = \{gm(C) - s \cdot Cgd(C)\} \Big/ \Big(\{1 + s \cdot [Cgd(C) + Cgs(C)] \cdot Rg(C)\}$$

$$\cdot \left\{ gds(C) + gds(L) + \frac{1}{RL} + s \cdot [Cgd(C) + Cds(C) + Cgd(L) + Cds(L)] \right\} + s \cdot Cgd(C) \cdot Rg(C) \cdot gm(C) - s^2 \cdot Cgd(C)^2 \cdot Rg(C) \Big). \quad \text{(A-3)}$$

The transfer function $B(s)$ for the source follower part is introduced by the same procedure as for the switch part transfer function $A(s)$. Here, output voltage of the switch part is considered as a Thevenin voltage source with an internal resistance RL to the source follower part as shown in Fig. 6(b). $B(s)$ is expressed by the following equation:

$$B(s) = \{-gm(F) - s \cdot Cgs(F)\} \Big/ \left(\left\{ gm(F) + gds(L) + \frac{1}{RS} + s \cdot [Cgs(F) + Cds(F) + CL] \right\} \cdot \{1 + s \cdot [Cgs(F) + Cgd(F)] \cdot [Rg(F) + RL]\} - s \cdot Cgs(F) \cdot [Rg(F) + RL] \cdot gm(F) - s^2 \cdot Cgs(F)^2 \cdot [Rg(F) + RL] \right). \quad \text{(A-4)}$$

ACKNOWLEDGMENT

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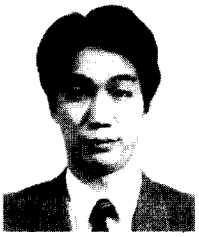

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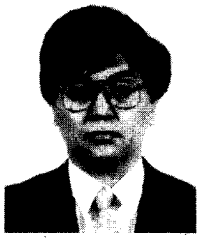

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