# Fully Electrical 40Gb/s TDM System Prototype Based on InP HEMT Digital IC Technologies


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# Fully Electrical 40-Gb/s TDM System Prototype Based on InP HEMT Digital IC Technologies

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***Abstract*—This paper presents a fully electrical 40-Gb/s time-division-multiplexing (TDM) system prototype transmitter and receiver. The input and output interface of the prototype are four-channel 10-Gb/s signals. The prototype can be mounted on a 300-mm-height rack and offers stable 40-Gb/s operation with a single power supply voltage. InP high-electron mobility transistor (HEMT) digital IC's perform 40-Gb/s multiplexing/demultiplexing and regeneration. In the receiver prototype, unitraveling-carrier photodiode (UTC-PD) generates 1 $V_{PP}$ output and directly drives the InP HEMT decision circuit (DEC) without any need for an electronic amplifier. A clock recovery circuit recovers a 40-GHz clock with jitter of 220 $fs_{PP}$ from a 40-Gb/s nonreturn-to-zero (NRZ) optical input. The tolerable dispersion range of the prototype within a 1-dB penalty from the receiver sensitivity at zero-dispersion is as wide as 95 ps/nm, and the clock phase margin is wider than 70° over almost all the tolerable dispersion range. A 100-km-long transmission experiment was performed using the prototype. A high receiver sensitivity [−25.1 dBm for NRZ ($2^7 - 1$) pseudorandom binary sequence (PRBS)] was obtained after the transmission. The 40-Gb/s regeneration of the InP DEC suppressed the deviation in sensitivity among output channels to only 0.3 dB. In addition, four-channel 40-Gb/s wavelength-division-multiplexing (WDM) transmission was successfully performed.**

***Index Terms*—Optical communication, optical communication equipment, time-division multiplexing (TDM).**

## I. Introduction

THE recent explosive growth of the internet indicates that a multimedia communication era is near at hand. Very-large-capacity backbone networks are a step toward the establishment of multimedia networks. The development of Er-doped fiber amplifier (EDFA) has made for a rapid increase of transmission bit rates and led to the implementation of the time-division-multiplexing (TDM) 10-Gb/s transmission system (FA-10G system) in 1996 [1]. As a result of the broadband characteristics of EDFA's, progress in optical multiplexing techniques such as optical TDM (OTDM) and wavelength-division multiplexing (WDM) drastically increased transmission bit rates beyond 1 Tb/s [2]–[5]. These techniques will make greater use of the ultrabroad bandwidth of optical fibers. For realizing very-large backbone networks, high-speed TDM systems, which offer a basic bit rate of optical multiplexing, are quite important. High-speed TDM systems based on digital integrated circuit (IC) technology have great advantages in terms of ease of operation, administration, and maintenance (OAM), compact size while increasing the single channel bit rate, and low cost. Furthermore, high-speed TDM systems can also effectively enhance the spectral efficiency in dense WDM systems. All these advantages are strong motivation to investigate 40-Gb/s TDM systems. To date, we have presented and demonstrated the transmission techniques for 40-Gb/s systems [6], [7]. Some promising techniques, automatic dispersion equalization [8], [9], high-dispersion tolerant transmission codes [10]–[13] have been presented to overcome the problems of high-speed TDM systems, such as the dispersion limit of optical fiber. The base of the 40-Gb/s system will be consolidated through several system experiments that employ these techniques. For such experiments, a stable 40-Gb/s transmitter and receiver are indispensable.

In this paper, we present a 40-Gb/s TDM system prototype, transmitter and receiver circuits, based on InP high-electron mobility transistor (HEMT) digital IC technologies. The input and output interface of the prototype are four-channel 10-Gb/s signals. The prototype can be mounted on a 300-mm-height rack and offers stable 40-Gb/s operation with a single power supply voltage. In the transmitter and receiver, an InP HEMT decision circuit (DEC) performs 40-Gb/s regeneration by using a 40-GHz clock. In the receiver prototype, high-output power photodiode, a unitraveling-carrier photodiode (UTC-PD), [14] generates an output pulse with an amplitude of 1.0 $V_{PP}$ and directly drives the InP HEMT DEC. This simple receiver configuration [15] relaxes the gain flatness problems in equalization and achieves a high-receiver sensitivity of −25.1 dBm after a 100-km-long dispersion shifted fiber (DSF) transmission. The relationship between the receiver sensitivity and the input data sensitivity of the DEC is also discussed. The tolerable dispersion range, clock phase margin and root-mean-square (rms) jitter of the prototype are also described in detail. In addition, a four-channel 40-Gb/s (160 Gb/s) WDM transmission is demonstrated.

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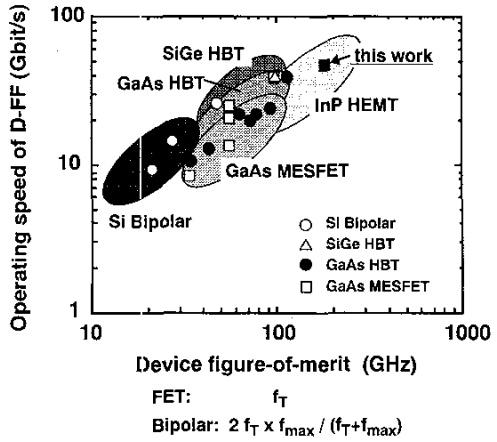


Fig. 1. Empirical relationship between D-FF speed and a device figure-of-merit.

## II. InP HEMT Digital IC Technology

Ultrahigh-speed digital integrated circuits (IC's) are indispensable to the creation of 40-Gb/s TDM systems. In particular, D-type flip-flop (D-FF) or DEC, which performs the regeneration at 40 Gb/s, is quite important. To date, many D-FF's designed for high-speed operation (Si bipolar [16], SiGe HBT [17], GaAs HBT [18], and GaAs MESFET [19]) have been reported. Fig. 1 shows the empirical relationship between the operating speed of the D-FF and a device figure-of-merit. InP HEMT offers the highest cutoff frequency ($f_T$) and maximum frequency of oscillation ($f_{max}$) of all semiconductor devices [20], [21] and has the potential to achieve 40-Gb/s digital IC's. The InP HEMT has another advantage in that it can be integrated with photonic devices such as photodiodes for a wavelength range from 1.3 to 1.55 μm [22], [23]. The integration reduces the number of electronic parts and high-speed interconnection paths and will realize compact and low-cost packages. We fabricate a super-dynamic type DEC [24] using InP HEMT's [25] that was capable of 40-Gb/s operation. The DEC IC is configured with the super-dynamic D-FF core, data/clock input buffers, and a data output buffer/driver. The super-dynamic D-FF is characterized by a source-coupled negative feedback pair (SCNFP) inserted in the first-level latching differential pair in a cascode manner. The SCNFP drastically reduces the effective logic swing and increases FF operating speed. Wideband data and clock buffers were used to increase the DEC IC's speed to the core D-FF speed limit. The data buffers consist of a capacitive feedback differential buffer [26] with a source follower employing capacitive peaking. The clock buffer consists of a capacitively coupled inductor-peaking differential buffer. The maximum operating speed of the DEC that could achieve error-free operation was 46 Gb/s. Error-free operation at higher rates has not been confirmed yet due to the limitations of the experimental setup. Fig. 2 shows the measured input data sensitivity and clock phase margin of the DEC at data rates from 26–40 Gb/s. As the signal source, pseudorandom binary sequence (PRBS) with an amplitude of 800 $mV_{pp}$ generated by a 4 : 1 multiplexer was used [27]. To measure the sensitivity, the amplitude of the PRBS was attenuated. The input data sensitivity was measured by the difference between the centers of the "1" and "0" levels for a bit error rate (BER) of better than $1 \times 10^{-11}$. For the clock phase margin, the edge drift of the output eye diagram of the DEC for a BER of better than $1 \times 10^{-9}$ when the clock timing was shifted was measured. A high input sensitivity of less than 104 $mV_{pp}$ and a wide phase margin of 212° were obtained for 40-Gb/s $(2^7 - 1)$ PRBS. Degradation of the sensitivity and phase margin was observed for the data lengths longer than $(2^7 - 1)$. However, the sensitivity was still higher than 250 $mV_{pp}$, and the phase margin was as wide as 164° for $(2^{31} - 1)$ PRBS. The degradation of the sensitivity and phase margin for PRBS's longer than $(2^7 - 1)$ may be caused by the bandwidth limit and unflat frequency characteristics of the input buffers.

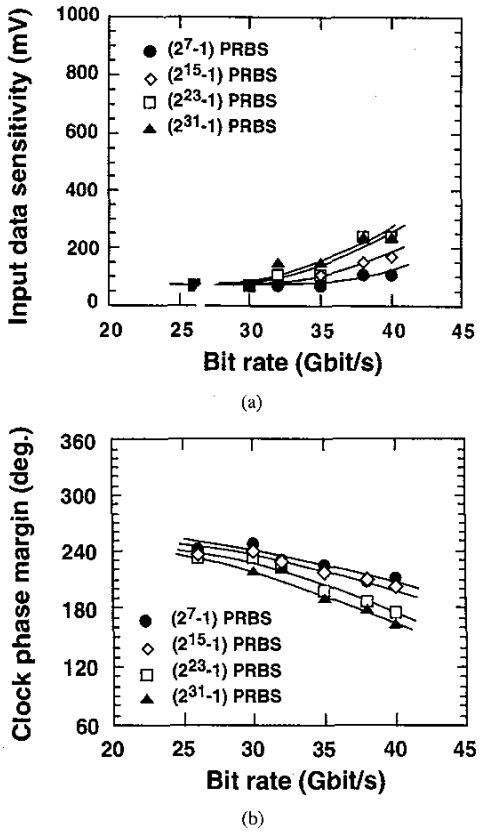


Fig. 2. DEC performance: (a) input data sensitivity and (b) clock phase margin.

## III. Circuit Configuration of System Prototype

A 40-Gb/s TDM system prototype based on InP HEMT digital IC's [27] was fabricated. Fig. 3 is a block diagram of the prototype. The transmitter consists of a 10-G/20-G 4 : 2 multiplexer (10/20-G MUX) unit, a 20-G/40-G multiplexer and transmitter (40-G Tx) unit, and a clock distribution (CLK DIST) unit. The 10/20-G MUX unit consists of two GaAs MESFET 2 : 1 selectors (SEL) and a GaAs MESFET clock distributor IC's, which are mounted in a 84-pin RF package by using a multichip module technique. The MUX unit multiplexes the four 10-Gb/s data streams to two 20-Gb/s data streams. In the

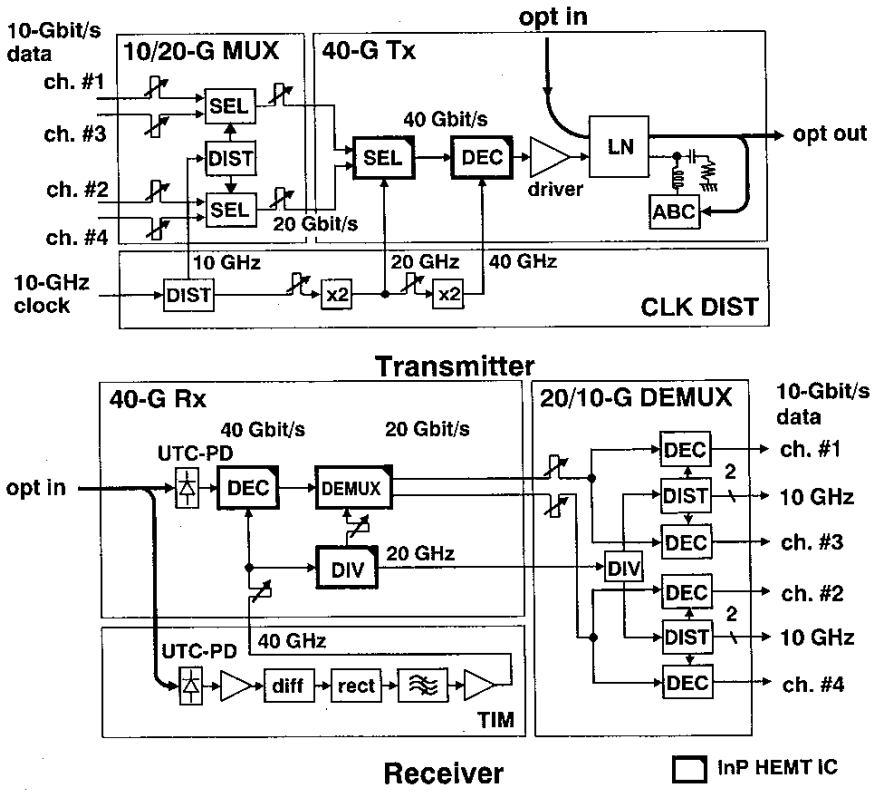


Fig. 3. Block diagram of the 40-Gb/s system prototype.

40-G Tx unit, the two 20-Gb/s data streams are multiplexed to a 40-Gb/s data stream by an InP HEMT SEL [28]. Regeneration of the InP HEMT DEC eliminates the asymmetry between the even and odd channel eye opening. External continuous-wave light is modulated by a $LiNbO_3$ (LN) Mach–Zehnder modulator with a low-driving voltage of 3.0 V [29]. An automatic bias controller (ABC) is used to compensate for the DC drift of the LN modulator. The CLK DIST unit generates 20 and 40-GHz clock signals by using frequency doublers and distributes the signals to other units.

The receiver consists of a 40-Gb/s receiver (40-G Rx) unit, a 20-G/10-G 2 : 4 demultiplexer (20/10-G DEMUX) unit, and a clock recovery (TIM) unit. The 40-G Rx consists of a UTC-PD, an InP HEMT DEC, a 1 : 2 demultiplexer (DEMUX) and 1 : 2 frequency divider (DIV) [2]. The optical input is divided into two by a 3-dB optical coupler. One input is received by the UTC-PD, and the other one is introduced to the TIM unit. The UTC-PD generates 1.0 $V_{pp}$ output and directly drives the DEC [30]. This direct driving reduces the number of electronic parts and relaxes the gain flatness problems in equalization. The UTC-PD module has a 3-dB bandwidth of higher than 35 GHz with a response flatness less than 1 dB. The DEC regenerates a 40-Gb/s signal using a 40-GHz clock signal recovered at the TIM unit. The output of the DEC is demultiplexed to two 20-Gb/s data streams by the DEMUX. The 20/10-G DEMUX unit consists of four Si bipolar DEC's, a GaAs MESFET DIV and a clock distributor (DIST). Each 20-Gb/s data stream from the 40 G-Rx unit is divided into two by using power dividers and demultiplexed to four-channel 10-Gb/s data by the DEC's using 10-GHz clock signal. The maximum data skew among four output channels was only 12 ps. The TIM unit recovers the 40-GHz clock signal by using a differentiator and a half-wave rectifier. The differentiator is a microstrip line $\lambda/4$ short stub formed on an $Al_2O_3$ substrate. An impedance matching circuit with a 50-$\Omega$ resistor is placed in front of the short stub to restrict the reflection at the short stub. The bandpass filter is a waveguide-type cavity resonator. The measured $Q$ value of the filter is 700. The amplifier following the filter is a commercially available and is not a limiting amplifier.

All the electrical input and output of the transmitter and receiver units use the source-coupled FET logic (SCFL) interface. The K-connector-type panel adapters are used for the data and clock interface above 20 Gb/s and 20 GHz. Fig. 4 shows photographs of the 40-G Tx and Rx units. These units can be mounted on a 300-mm height rack and operated under a fan-cooling condition. Fig. 5 is a photograph of the system prototype mounted on the half-size standard racks.

## IV. Experimental Results and Discussion

### A. Clock Recovery

In the TIM unit, a 40-GHz clock was recovered by a differentiator and a half-wave rectifier. This configuration offers reliable clock recovery. The differentiator was a $\lambda/4$ short stub vertically connected to a 50-$\Omega$ microstrip line formed on an $Al_2O_3$ substrate. The short stub differentiates the input NRZ signal propagated on the microstrip line by eliminating the dc and low-frequency spectra of the signal. However, the short stub causes se-

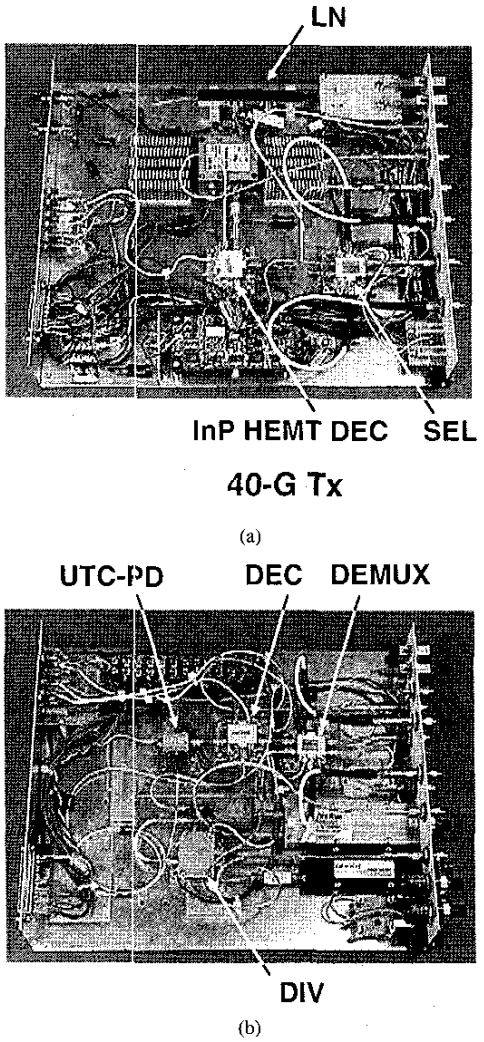


Fig. 4. Photographs of (a) 40-G Tx and (b) 40-G Rx.

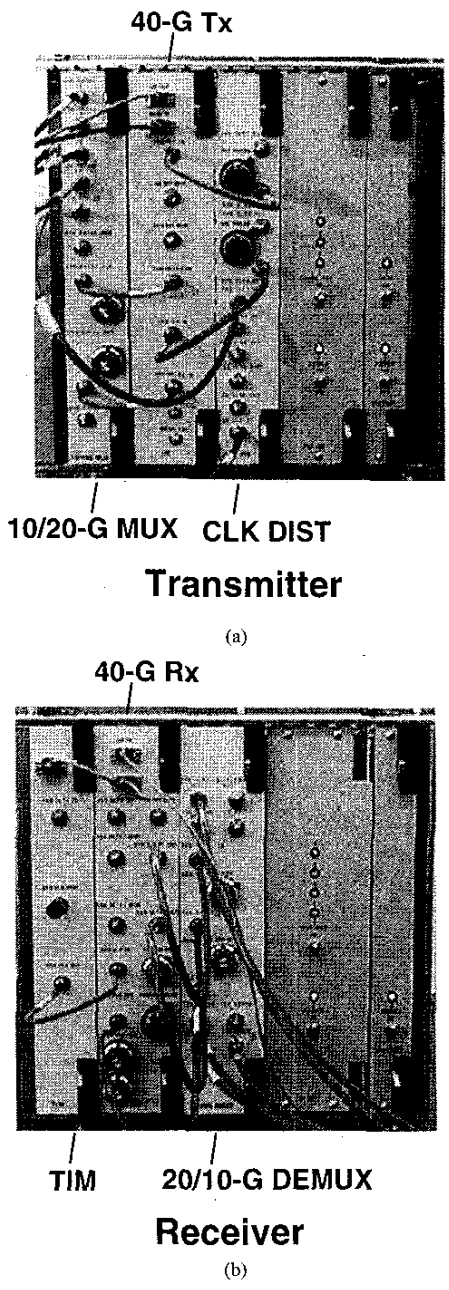


Fig. 5. Photograph of the 40-Gb/s system prototype.

rious reflections because its input impedance matches 50 Ω at only 40 GHz. To suppress the reflection, an impedance matching circuit using a high-impedance microstrip line and a thin-film 50-Ω resistor were formed in front of the short stub; as a result, the return loss was restricted to less than 9 dB up to 40-GHz. To confirm the effect of the matching circuit, the reflection at the differentiator was monitored. The experimental setup is shown in Fig. 6(a). The input 40-Gb/s signal was divided into two. One was introduced to the differentiator, and the other one was monitored by a sampling oscilloscope. The reflection from the differentiator distorted the monitored signal. The monitored eye diagram of the differentiator is shown in Fig. 6(b). For comparison, the eye diagram of a differentiator without the matching circuit is shown in Fig. 6(c). The reflection from the differentiator without matching circuit seriously distorted the monitored signal. The serious reflection could cause clock jitter, and it narrowed the operating margin of the prototype. On the other hand, the differentiator with the matching circuit restricted the reflection, and the monitored eye diagram was clear. The low-reflection differentiator with 50 Ω resistor enables the direct connection to electronic IC's such as data distributor having an SCFL interface. Fig. 7 shows the output eye diagrams of the differentiator and the rectifier. Good eye openings were obtained at a data rate of 40 Gb/s.

The output of the rectifier, via the bandpass filter, was amplified by a narrowband amplifier. The mark ratio dependence and input amplitude dependence of the output clock amplitude of the TIM unit are shown in Fig. 8(a) and (b), respectively. Here, a 40-Gb/s $(2^{31} - 1)$ PRBS generated by the InP SEL was introduced to the differentiator. The clock amplitude was normalized by the output amplitude for the 1-$V_{pp}$ input with a mark ratio of 1/2. No significant decrease of the clock amplitude was observed when the mark ratio was changed from 1/2 to 1/8. The amplitude decreased as the decrease of the input amplitude. This

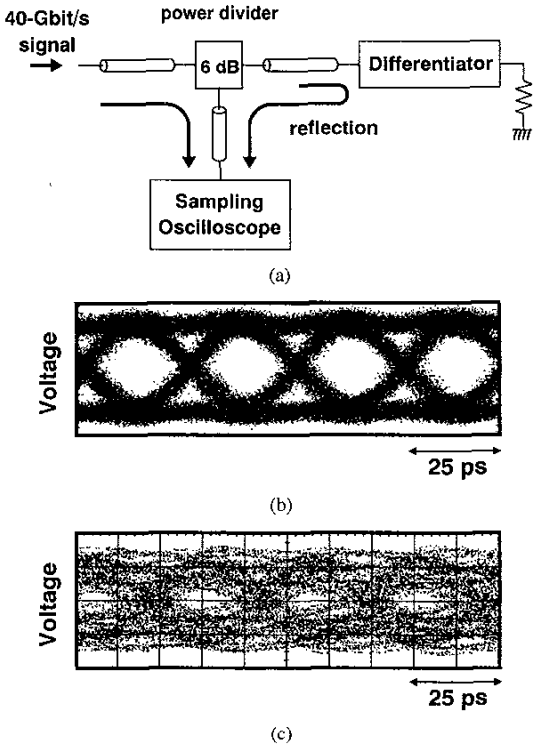


Fig. 6. Monitored waveforms distortion due to reflection from differentiator: (a) experimental setup, (b) with matching circuit, and (c) without matching circuit.

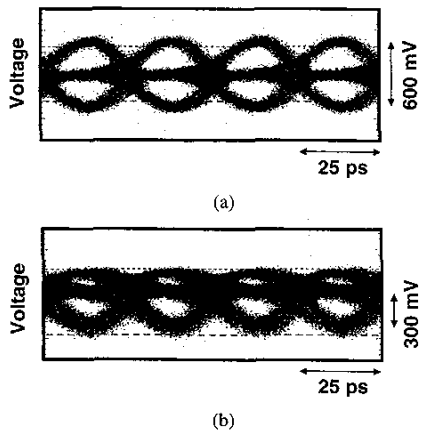


Fig. 7. 40-Gb/s output eye diagrams: (a) differentiator and (b) rectifier.

is because the rectifier does not work as the input amplitude decreases. In an actual transmission system, the input amplitude is varied by pulse compression or broadening due to dispersion. To prevent input amplitude fluctuation, an amplifier was inserted between the UTC-PD and the differentiator. The phase deviation of the recovered clock was large against the change of the mark ratio because the phase deviation of the amplifier strongly depended on the input power. A limiting amplifier is needed to suppress the phase deviation. A full-wave rectifier is also required to relax the dynamic range requirements of the limiting amplifier. The use of an exclusive-OR circuit as a differentiator

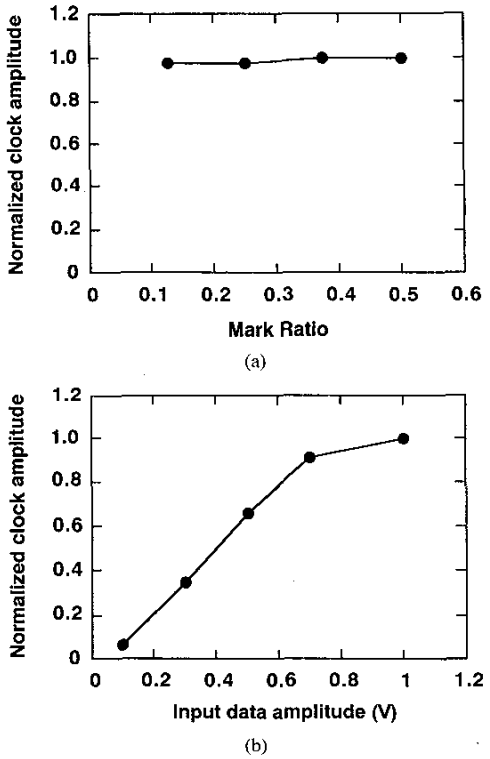


Fig. 8. Normalized clock amplitude of the TIM unit: (a) mark density dependency and (b) input data amplitude dependency.

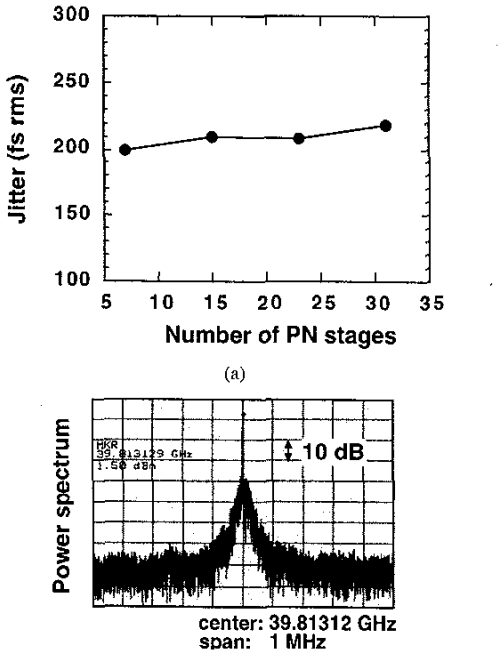


Fig. 9. Measured rms jitter and power spectrum of the TIM unit: (a) data length dependent of the jitter and (b) power spectrum.

and full-wave rectifier effectively recovers the clock signal and relaxes the dynamic range requirements of the limiting amplifier [31].

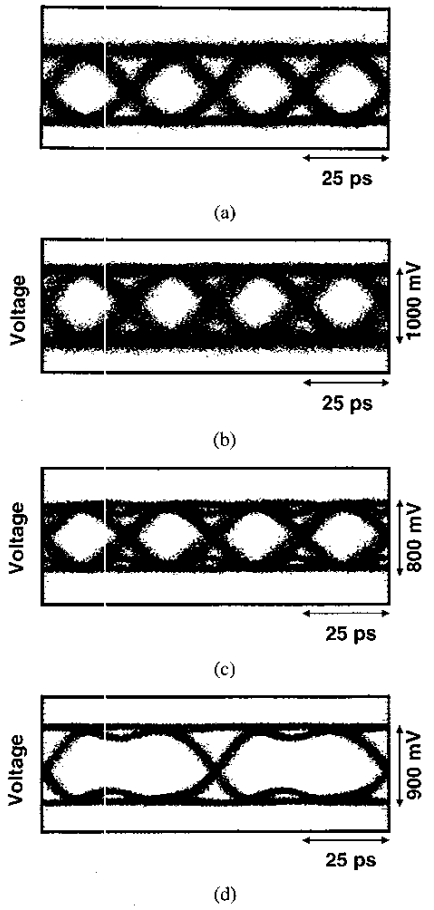


Fig. 10. Output eye diagrams: (a) 40-G Tx, (b) UTC-PD module, (c) InP HEMT DEC in the 40-G Rx, and (d) InP HEMT DEMUX.

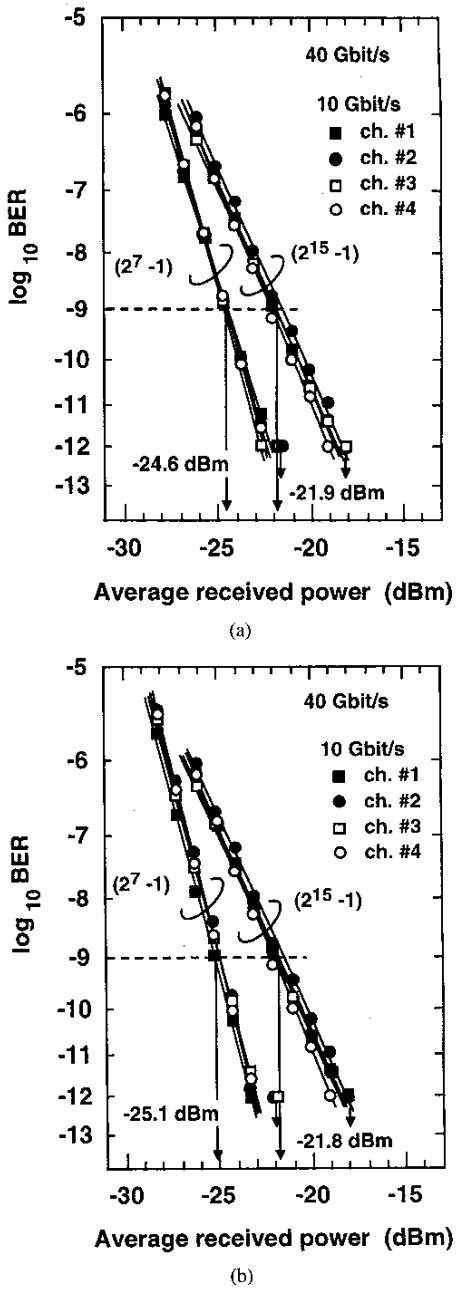


Fig. 11. Bit-error-rate performance: (a) 0 km and (b) after 100-km-long DSF transmission.

The rms jitter of the clock signals recovered from optical PRBS signals ranging in length from $(2^7 - 1)$ to $(2^{31} - 1)$ [the number of pseudo-random noise (PN) stages from 7 to 31] was measured by a jitter measurement system (EUROPTEST PN9000 series) and is shown in Fig. 9(a). Here, the rms jitter of the 40-GHz clock for the InP DEC in the 40-G Tx was 150 $fs_{rms}$. Measured jitter did not depend on the data length and was as small as 220 $fs_{rms}$. Fig. 9(b) shows the spectrum of the clock signal measured by a spectrum analyzer. A high signal-to-noise ratio (SNR) was obtained.

### *B. Single-Carrier 40-Gb/s Transmission*

The 40-Gb/s transmission experiments that used the system prototype were performed. A four-channel 10-Gb/s NRZ PRBS from a pulse pattern generator (PPG), in which the relative delay against each channel was exactly adjusted to a quarter of the data period, was used as the signal source. These input signals were multiplexed up to 40 Gb/s PRBS and regenerated by the InP HEMT DEC in the transmitter. Continuous-wave light from a DFB-LD with a wavelength of 1552 nm was modulated with the 40-Gb/s NRZ PRBS. The output of the transmitter was amplified by an EDFA and was launched into a 100-km-long transmission fiber that had a zero-dispersion wavelength of 1552 nm. The input power for the transmission line was 10 dBm. After the 100-km-long transmission, the 40-Gb/s optical data was amplified by using another EDFA followed by 5-nm optical bandpass filter (OBPF) and then was received by the receiver. In the receiver, the transmitted signal was regenerated and was demultiplexed to four-channel 10-Gb/s signals by the clock signal recovered from the optical input at the TIM unit. Fig. 10 shows the eye diagrams obtained by a sampling oscilloscope. The 40-G Tx generated clear 40-Gb/s optical data [Fig. 10(a)]. The UTC-PD generated a clear eye diagram with an output amplitude of 1 $V_{pp}$ [Fig. 10(b)] and directly drove the following InP HEMT

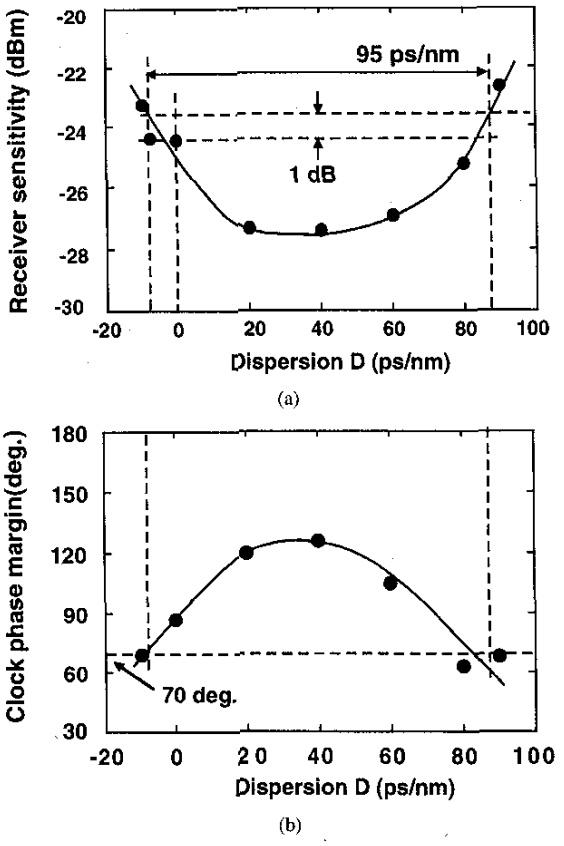


Fig. 12. Dispersion dependence of (a) receiver sensitivity and (b) clock phase margin.

DEC. The average input power for the UTC-PD was 16 dBm. Fig. 10(c) and (d) show the output eye diagrams of the InP DEC and DEMUX modules observed at the monitor ports. These modules successfully performed the 40-Gb/s regeneration and demultiplexing operation by using the recovered clock signal.

Bit-error-rates before and after transmission were measured by using error detectors (ED's) and are shown in Fig. 11. For the $(2^7-1)$ PRBS, the prototype showed a high-receiver sensitivity: $-24.6$ dBm before transmission and $-25.1$ dBm after transmission. Small anomalous dispersion in the fiber improved the sensitivity after transmission. When the data length increased to $(2^{15}-1)$, a penalty of about 3 dB was observed. However, the sensitivity was still high: $-21.9$ dBm before transmission and $-21.8$ dBm after transmission, and no error floor was observed in all channels down to a BER of better than $10^{-12}$. The DEC regeneration in the 40-G Tx achieved the small deviation in sensitivity among the four 10-Gb/s channels after transmission: 0.3 and 0.6 dB for $(2^7-1)$ and $(2^{15}-1)$ PRBS, respectively.

Back-to-back receiver sensitivity and clock phase margin of the prototype were measured for various dispersions induced by standard side-mode fibers (SMF's) or dispersion compensation fibers (DCF's). Fig. 12 shows the measured receiver sensitivity and clock phase margin for a BER of $10^{-9}$. The input data was NRZ $(2^7-1)$ PRBS with a wavelength of 1552 nm. The average input power for the EDFA was set to be $-20$ dBm when the clock phase margin was measured. The clock phase margin was estimated by a counting dial shift of the 40-GHz clock phase shifter (Anritsu G5N1) attached to the front panel. The receiver sensitivity without dispersion was $-24.5$ dBm. Note that this sensitivity was in good agreement with the back-to-back sensitivity ($-24.6$ dBm) shown in Fig. 11(a). This result shows a stable 40-Gb/s operation of the prototype. As the dispersion shifted into the anomalous region, the sensitivity was improved due to the pulse compression, and the prototype achieved its highest sensitivity: $-27.4$ dBm for a dispersion of 40 ps/nm. The pulse compression in the anomalous dispersion region was due to the negative chirp of the LN modulator. The tolerable dispersion range within 1-dB power penalty from the receiver sensitivity at zero-dispersion was 95 ps/nm. The clock phase margin was wider than 70° over the tolerable dispersion range.

As shown in Figs. 11 and 12, the prototype achieved high receiver sensitivity. The issue is the penalty against the longer data length. To reduce the penalty, further improvements to the components in the prototype in terms of their speed are required. In particular, the input sensitivity of the DEC is quite important. The sensitivity at 40 Gb/s degraded from 104 to 166 $mV_{pp}$ with the data length became longer from $(2^7-1)$ to $(2^{15}-1)$ [Fig. 2(a)]. This degradation is one of the causes of the power penalty. A higher sensitivity that does not depend on the data length will reduce the penalty and will achieve higher receiver sensitivity. For this, broadening the bandwidth of the data buffer using analog techniques and optimizing the circuit parameters are quite important. Accumulation of pattern jitter and intersymbol interference in the process of electrical-to-optical (E/O) conversion in the transmitter and optical-to-electrical (O/E) conversion in the receiver seems to be another cause of the penalty because the clock phase margin after the E/O and O/E conversion [Fig. 12(b)] was less than half that without the conversion [Fig. 2(b)]. Therefore, broadening the bandwidth of the transmitter and front-end in the receiver is also important.

### C. 160-Gb/s WDM Transmission

Four-channel 40-Gb/s WDM transmission was performed. The experimental setup is shown in Fig. 13. Four 200-GHz spacing optical carriers [1552 nm ($\lambda 1$), 1553.6 nm ($\lambda 2$), 1555.2 nm ($\lambda 3$), 1556.8 nm ($\lambda 4$)] were simultaneously modulated with 40-Gb/s NRZ $(2^7-1)$ PRBS. The output of the transmitter was amplified to +16 dBm by an EDFA and was launched into a 100-km long-transmission fiber with a zero-dispersion wavelength of 1540 nm. To reduce the total dispersion, a DCF (–60 ps/nm) was connected to the end of the transmission fiber. The wide tolerable dispersion range (95 ps/nm) of the receiver (Fig. 12) achieved the simultaneous dispersion compensation. After the transmission, the WDM wavelength channel was selected by a 1-nm OBPF and was received by the receiver. Fig. 14 shows the measured BER before and after transmission. Here, the BER of each wavelength channel was the average of the four 10-Gb/s data channels. High receiver sensitivities, from –25.7 to –24.6 dBm before transmission and from –27.2 to –25.3 dBm after transmission, were obtained at a BER of $1 \times 10^{-9}$. The improvement in the sensitivity after transmission was caused by pulse compression due to the anomalous dispersion.

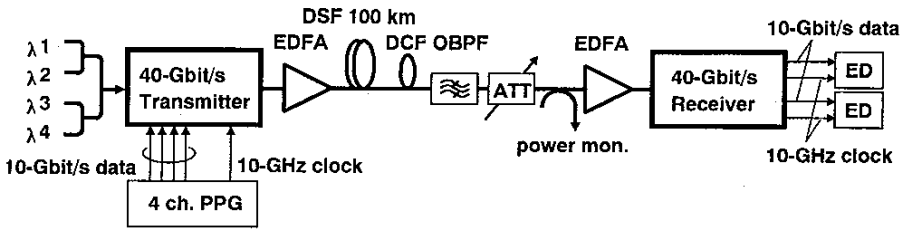


Fig. 13. Experimental setup for 160-Gb/s WDM transmission.

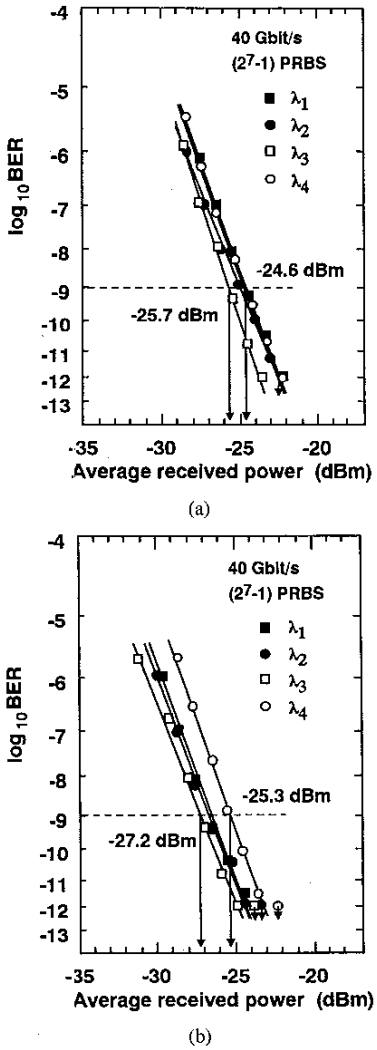


Fig. 14. BER performance of 160-Gb/s WDM transmission: (a) 0 km and (b) after 100-km-long DSF transmission.

## V. Conclusion

We fabricated a fully electrical 40-Gb/s TDM system prototype based on InP HEMT digital IC technologies for 40-Gb/s system experiments. The prototype transmitter and receiver units were mounted on a 300-mm-height rack and operated with a single power supply voltage. In the transmitter unit, four-channel 10-Gb/s input signals were multiplexed to 40-Gb/s signal and were regenerated by the InP HEMT DEC to eliminate the asymmetry between the even and odd channel's eye openings. In the receiver unit, the UTC-PD module generated 40-Gb/s input with an amplitude of 1.0 $V_{pp}$ and directly drove the following InP HEMT DEC without any need for electronic amplifiers. The DEC regenerated the 40-Gb/s signal by using the 40-GHz clock recovered at the clock recovery unit. The regenerated signal was demultiplexed to four-channel 10-Gb/s signals by the InP HEMT DEMUX and Si bipolar DEC's. The rms jitter of the recovered clock did not depend on data length and was as small as 220 $fs_{rms}$. The tolerable dispersion range of the prototype within 1-dB penalty from the receiver sensitivity at zero-dispersion was 95 ps/nm, and the clock phase margin was wider than 70° over almost all the tolerable dispersion range.

A 100-km-long DSF transmission experiment that used the prototype was performed. A high receiver sensitivity, −25.1 dBm for $(2^7-1)$ PRBS and −21.8 dBm for $(2^{15}-1)$ PRBS, was obtained. The 40-Gb/s regeneration in the transmitter successfully suppressed the deviations in sensitivity among the four 10-Gb/s channels: 0.3 dB for $(2^7-1)$ PRBS and 0.6 dB for $(2^{15}-1)$ PRBS. The power penalty for longer data length is caused by the sensitivity degradation of the DEC and an accumulation of pattern jitter and intersymbol interference in the process of the E/O and O/E conversion. Four-channel 40-Gb/s WDM transmission was also performed using the prototype, and a high receiver sensitivity (from −27.2 to −25.3 dBm) was obtained after 100-km-long DSF transmission.

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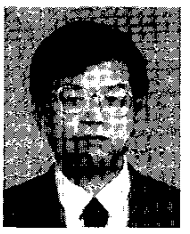

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