# Analysis and application of a novel model for estimating power dissipation of optical interconnections as a function of transmission bit error rate


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# Analysis and Application of a Novel Model for Estimating Power Dissipation of Optical Interconnections as a Function of Transmission Bit Error Rate

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***Abstract*— This paper proposes a novel model for estimating power dissipation of optical/electrical interconnections as a function of transmission bit error rate. This model is applied to a simplified optoelectronic transmitter and receiver configuration in which a photodetector is directly connected to the decision circuit. It is analytically verified that this configuration can achieve error-free operation with low power under practical operating conditions. A comparison between optical and electrical interconnections based on this simplified configuration is performed. This result shows the interconnection length and bit rate at which optical interconnection is superior in terms of power dissipation to electrical interconnection. Only optical interconnections achieve error-free operation with 40 mW power dissipation at a transmission bit rate of 10 Gb/s and an interconnection length over 7 m.**

## NOMENCLATURE

| | | |
|---|---|---|
| $I_{\mathrm{LD1}}$ | = | Drive current of laser diode at logic level "1" |
| $\sigma_{\mathrm{LD1}}$ | = | Process standard deviation of $I_{\mathrm{LD1}}$ |
| $I_{\mathrm{LD0}}$ | = | Drive current of laser diode at logic level "0" |
| $\sigma_{\mathrm{LD0}}$ | = | Process standard deviation of $I_{\mathrm{LD0}}$ |
| $\eta_{\mathrm{LD}}$ | = | Slope efficiency of laser diode |
| $\eta_t$ | = | Total coupling efficiency in optical interconnection |
| $\sigma_{\mathrm{LD}}$ | = | Process standard deviation of $\eta_{\mathrm{LD}}$ |
| $I_{\mathrm{th}}$ | = | Threshold current of laser diode |
| $\Delta I_{\mathrm{th}}$ | = | Temperature fluctuation of $I_{\mathrm{th}}$ |
| $T_o$ | = | Characteristic temperature of laser diode |
| $\alpha$ | = | Coupling efficiency of optical fiber |
| $\eta_{\mathrm{PD}}$ | = | Sensitivity of photo diode |
| $\sigma_{\mathrm{PD}}$ | = | Process standard deviation of $\eta_{\mathrm{PD}}$ |
| $R$ | = | Load resistance of photo diode |
| $\sigma_R$ | = | Process standard deviation of $R$ |
| $Z_t$ | = | Transimpedance of preamplifier |
| $\sigma_{Zt}$ | = | Process standard deviation of $Z_t$ |
| $\sigma_{n0}, \sigma_{n1}$ | = | Noise amplitude at logic levels "1" and "0" |
| $V_{sen}$ | = | Decision sensitivity |
| $V_{\mathrm{ref}}$ | = | Reference level of decision circuit |
| $\sigma_{\mathrm{ref}}$ | = | Process standard deviation of $V_{\mathrm{ref}}$ |
| $I_1$ | = | Drive current of coaxial cable at logic level "1" |
| $\sigma_{I1}$ | = | Process standard deviation of $I_1$ |
| $I_0$ | = | Drive current of coaxial cable at logic level "0" |
| $\sigma_{I0}$ | = | Process standard deviation of $I_0$ |
| $L$ | = | Coaxial cable length |
| $\rho$ | = | Reflection coefficient in electrical interconnections |
| $R_m$ | = | Matching resistance |
| $\sigma_{Rm}$ | = | Process standard deviation of $R_m$ |
| $\alpha_o$ | = | Extra loss due to clock skew in optical interconnections |
| $\alpha_e$ | = | Attenuation coefficient in electrical interconnections |

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## I. INTRODUCTION

AS SYSTEM data rates and complexities increase, faster and denser signal interconnections at all levels of systems, boards, and LSI's are required. Electrical interconnections require coaxial cables with higher transmission bit rates. However, it has been generally recognized that systems will become impracticably huge with multiple interconnections using coaxial cables and that the connections will approach their length and density limits due to crosstalk and the skin effect.

On the other hand, optical transmission techniques have matured with advances in low-loss optical fibers and photonic and electronic device technology, especially in the telecommunications field. Recently, optical transmission techniques have been applied to signal interconnections [1]–[4]. All the advantages, such as highly dense connections, no signal distortion, no crosstalk, high coherence, and ultrawide bandwidth, provide strong motivation to further study optical interconnections. Some unique optical interconnection techniques such as wavelength-division multiplexing (WDM) [5]–[7] and three-dimensional integration have been proposed [8]–[10], and

many attempts at optical interconnection based on both system levels and device levels have been reported [11]–[14]. These optical interconnections will greatly increase the speed and density of connections. To accelerate the progress in optical interconnection techniques, consensus at all levels of systems and devices is needed. Therefore, methodology to quantitatively evaluate the performance of interconnection systems is very important. In this case, power dissipation should be considered because it is the major target in improving optical interconnections. Several performance estimation methods and comparisons between optical and electrical interconnections have been reported [15]–[19]. However, only a few studies have considered temperature fluctuation factors [18], and no attempt has been made to estimate power dissipation as a way to achieve error-free operation under practical operating conditions.

In this paper we first propose a novel model for estimating the power dissipation of optical interconnections as a function of transmission bit error rate. We apply this model to a simplified optical transmitter and receiver in which a photodetector (PD) is directly connected to the decision circuit (DEC) [20], [21]. An analysis shows that this configuration can achieve error-free operation under practical operating conditions with low power dissipation. Second, we compare optical and electrical interconnections based on power considerations, confirming superior transmission bit rates and interconnection lengths for optical interconnections. Reduction of power dissipation owing to improvements in device characteristics is also quantitatively discussed.

## II. PD-DEC Direct Connection for Optical Interconnections

The basic configuration of a transmitter and receiver which is widely used in optical fiber telecommunications systems is shown in Fig. 1(a). To achieve error-free operation, a preamplifier, an auto temperature controller (ATC), an auto power controller (APC), and an auto offset controller (AOC) are required to compensate for signal loss and temperature fluctuations by long-haul transmission of over several 10 km. On the other hand, when optical techniques are applied to inter-board and/or inter-LSI connections, such a complex configuration would not be acceptable because power dissipation, connection density, and cost become major concerns. Recently, a simplified interconnection system has been proposed [20], [21] in which a PD is directly connected to a DEC, as shown in Fig. 1(b). T. Z. Tsang demonstrated a 1 Gb/s direct free space interconnection of digital circuits [20]. Y. Uematsu *et al.* reported a 1.25 Gb/s four-channel optical connection with bit error rate performance [21]. For both cases, a transimpedance preamplifier was replaced with a load resistance and no compensation circuits were used. We call the simplified configuration shown in Fig. 1(b) the "PD-DEC." This PD-DEC is very attractive in terms of power dissipation and cost and will be applicable to interconnection systems. The threshold current and distinction ratio of the laser diode (LD) are the largest fluctuation factors in these systems. However, an excess bias and modulation current for the LD may compensate for temperature fluctuations because the signal loss of optical fiber, including coupling loss, is only a few dB around 100 m transmission. To adopt this configuration in actual systems, the following issues must be addressed.

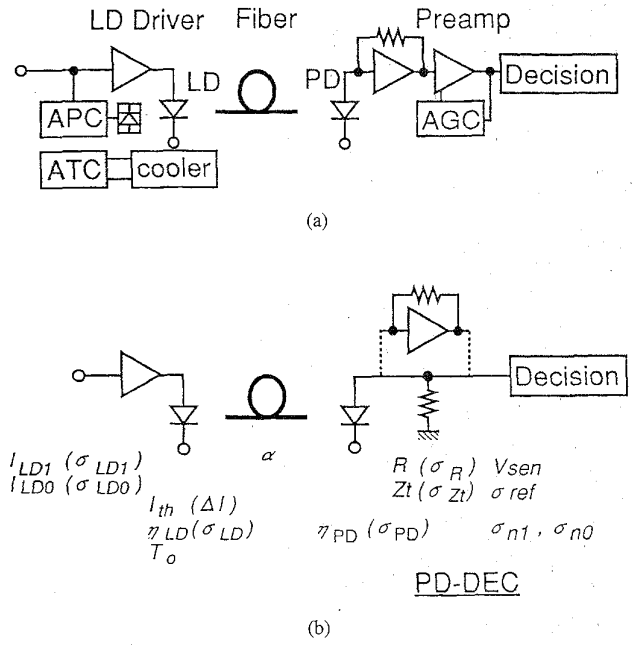


Fig. 1. Schematic diagram of optical-fiber communication systems: (a) Basic configuration of telecommunication systems and (b) PD-DEC and principal parameters.

1) Can the PD-DEC achieve error-free operation under practical operating conditions, such as process-dependent deviation of device characteristics (process deviation), temperature fluctuation, and noise?
2) Can the PD-DEC achieve error-free operation with lower power dissipation than in the long-haul transmitter and receiver configuration?
3) Can the PD-DEC compete with the configuration commonly used in electrical interconnections in terms of power dissipation?

Each of these issues are discussed in detail.

## III. Analysis of Power Dissipation for the PD-DEC

### A. Modeling for Optical Interconnections

In this section, we propose a model for optical interconnections used to analyze the power dissipation of the PD-DEC. This model can calculate the power dissipation and thus lead to error-free operation under practical operating conditions, such as the process-dependent deviation of device characteristics, temperature fluctuation, and noise.

As shown in Fig. 1(b), active devices, such as a LD driver and a PD, dominate the total power dissipation of the transmitter and receiver. The power dissipation of the PD depends on the optical output power from the LD. Therefore, when the power of the LD driver is given, we can estimate the

total power dissipation of the PD-DEC. The power dissipation of the LD driver is estimated by calculating the LD drive current $I_{\mathrm{LD1}}$. We calculate the $I_{\mathrm{LD1}}$ to achieve error-free operation. Parameters considered in the PD-DEC are shown in Fig. 1(b). For comparison, a configuration using a preamplifier and its parameters are also shown in this figure. For simplicity, we assume the following.

1) We are treating only single fan-in/fan-out interconnections.
2) The bandwidth of each device is much wider than the bit rate.
3) The transfer characteristics of each device have no signal-pattern dependence.
4) Crosstalk is negligible.
5) Clock signal is distributed to each decision circuit.
6) Temperature-dependent deviation is regarded only for the LD threshold current $I_{\mathrm{th}}$ and is introduced as $I_{\mathrm{th}} = I_0 \exp(T/T_0)$.
7) The bias current for the LD is set at a level higher by $I_{\mathrm{LD0}}$ than $I_{\mathrm{th}}$ at the highest temperature and remains above $I_{\mathrm{th}}$ at any temperature.
8) Total noise energy follows a Gaussian distribution and noise amplitudes at logic levels '1' and '0' are equal ($\sigma_{n1} = \sigma_{n0}$). Shot noise, one of the noise sources, is proportional to optical power detected at a receiver. However, we consider shot noise for the maximum optical power at both logic levels for the worst case estimation.
9) Process-dependent deviation in each process parameter is approximated by a Gaussian distribution. These deviations include effects from both process-inherent and operating condition-dependent variations.
10) Process-dependent standard deviations are simplified to be equal among all the parameters, and we introduce a single parameter $b$

$$\frac{b}{100} = \frac{\sigma_{\mathrm{LD}}}{\eta_{\mathrm{LD}}} = \frac{\sigma_{\mathrm{PD}}}{\eta_{\mathrm{PD}}} = \frac{\sigma_R}{R} = \frac{\sigma_{I_{\mathrm{LD1}}}}{I_{\mathrm{LD1}}} = \frac{\sigma_{I_{\mathrm{LD0}}}}{I_{\mathrm{LD0}} + \Delta I_{\mathrm{th}}}. \quad (1)$$

The maximum process-dependent deviation can be determined by screening.

In order to judge error-free conditions, we calculate bit error rates (BER's) at the decision circuit. We define a BER below a specific allowable value as an error-free condition. The BER can be calculated from decision sensitivity and signal and noise amplitude at the input node of the decision circuit. Fig. 2 shows the relation between these parameters at the input node of the decision circuit. The BER is defined as the probability that the noise distribution will penetrate the opposite side of $V_{\mathrm{ref}}$. When a signal amplitude is sufficiently larger than the noise amplitude, the BER becomes smaller than the allowable value. However, we generally cannot ignore the signal deviation, decision sensitivity $V_{\mathrm{sen}}$, or deviations in the reference level $\sigma_{\mathrm{ref}}$. Therefore, the signal amplitude from which the penalty due to deviation factors and the decision sensitivity are subtracted should be considered. When this effective signal amplitude is sufficiently larger than the effective decision sensitivity and noise amplitude, error-free operation is achieved. The values for effective signal amplitude, coupling efficiency, and individual device efficiency give the LD drive current $I_{\mathrm{LD1}}$. We analyze the total power dissipation of the PD-DEC using the $I_{\mathrm{LD1}}$ in the next section.

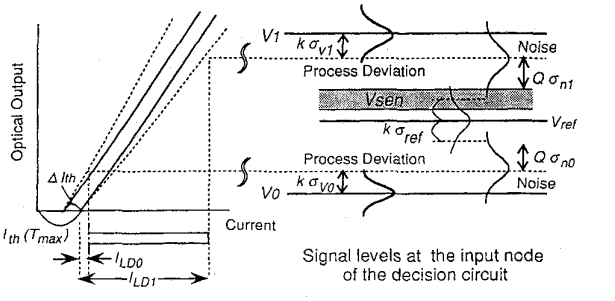


Fig. 2. Relation between signal levels in front of the decision circuit, noise, and sensitivity of the decision circuit.

### B. Analysis

The optical output levels from the LD deviate and the extinction ratio decreases with increasing temperature. Therefore, we must consider $V_1 = \alpha\eta_{\mathrm{LD}}\eta_{\mathrm{PD}}RI_{\mathrm{LD1}}$ and $V_0 = \alpha\eta_{\mathrm{LD}}\eta_{\mathrm{PD}}R(\Delta I_{\mathrm{th}} + I_{\mathrm{LD0}})$ to be the logic levels "1" and "0". Here, $V_1$ means the effective logic level "1" at the highest temperature and $V_0$ means the effective logic level "0" at the lowest temperature. Process-dependent deviations in these levels, $\sigma_{V1}$ and $\sigma_{V0}$, related to all process-dependent deviations, can also be approximated by a Gaussian distribution, and are given by (2-1) and (2-2) shown at the bottom of the page (see Appendix) where $\eta_t$ is the total efficiency: $\eta_t = \alpha\eta_{\mathrm{LD}}\eta_{\mathrm{PD}}$. When these process-dependent deviations are restricted by screening within $k$ times of each standard deviation, the effective signal amplitude $V_{O\mathrm{eff}}$ is expressed as

$$V_{O\mathrm{eff}} = (V_1 - k\sigma_{V1}) - (V_0 + k\sigma_{V0}). \quad (3)$$

For error-free operation, the effective signal amplitude $V_{O\mathrm{eff}}$ must be sufficiently larger than the effective decision sensitiv-

$$\sigma_{V1} = \eta_t I_{\mathrm{LD1}} R \left\{ \left(\frac{\sigma_{\mathrm{LD}}}{\eta_{\mathrm{LD}}}\right)^2 + \left(\frac{\sigma_{\mathrm{PD}}}{\eta_{\mathrm{PD}}}\right)^2 + \left(\frac{\sigma_R}{R}\right)^2 + \left(\frac{\sigma_{I_{\mathrm{LD1}}}}{I_{\mathrm{LD1}}}\right)^2 \right\}^{\frac{1}{2}}, \quad (2\text{-}1)$$

$$\sigma_{V0} = \eta_t (I_{\mathrm{LD0}} + \Delta I_{\mathrm{th}})\, R \times \left\{ \left(\frac{\sigma_{\mathrm{LD}}}{\eta_{\mathrm{LD}}}\right)^2 + \left(\frac{\sigma_{\mathrm{PD}}}{\eta_{\mathrm{PD}}}\right)^2 + \left(\frac{\sigma_R}{R}\right)^2 + \left(\frac{\sigma_{I_{\mathrm{LD0}}}}{I_{\mathrm{LD0}} + \Delta I_{\mathrm{th}}}\right)^2 \right\}^{\frac{1}{2}} \quad (2\text{-}2)$$

ity and noise amplitude. $V_{\mathrm{Oeff}}$ must satisfy (4)

$$V_{\mathrm{Oeff}} \geq V_{\mathrm{sen}} + 2k\sigma_{\mathrm{ref}} + Q(\sigma_{n1} + \sigma_{n0}). \tag{4}$$

The first and second terms on the right-hand side represent the effective sensitivity of the decision circuit. The third term is the noise contribution. The parameter $Q$ represents the relation between a BER and a signal-to-noise ratio. The relation between $Q$ and the BER is represented by BER $= 1/2\ \mathrm{Erfc}[Q/\sqrt{2}]$ and $Q \approx 8.5$ when BER $= 10^{-17}$. In this paper, we define a BER of $<10^{-17}$ as the error-free condition. From (1) to (4) the relation between the LD drive current $I_{\mathrm{LD1}}$ and load resistance of PD, $R$, is obtained as

$$I_{\mathrm{LD1}} \geq \frac{50+kb}{50-kb}(I_{\mathrm{LD0}} + \Delta I_{\mathrm{th}}) + \frac{2QI_n}{\eta_t\left(1-\frac{kb}{50}\right)} + \frac{V_{\mathrm{sen}} + 2k\sigma_{\mathrm{ref}}}{\eta_t\left(1-\frac{kb}{50}\right)R} \tag{5}$$

where $I_n$ is the equivalent input noise current when $\sigma_{n1} = \sigma_{n0}$ is assumed. This gives the minimum LD drive current required for error-free operation. The first term on the right-hand side represents the decrease in the extinction ratio due to process deviations and $\Delta I_{\mathrm{th}}$, the second term is the noise contribution, and the third term represents the effective sensitivity of the decision circuit. If a transimpedance amplifier is adopted, $R$ is replaced by the transimpedance gain $Z_t$.

In the PD-DEC, the LD driver and PD dominate the total power dissipation of the transmitter and receiver. The total power dissipation can be obtained by summing the power dissipation of the two. Power dissipation of the transmitter $P_t$ is obtained as

$$P_t = V_{\mathrm{dr}}(I_{\mathrm{th}}(80^{\circ}\mathrm{C}) + I_{\mathrm{LD1}}) \tag{6}$$

where $V_{\mathrm{dr}}$ is the bias voltage for the driver. The total power dissipation of the receiver $P_r$ is obtained as

$$P_r = 0.5\eta_t V_{\mathrm{PD}}(I_{\mathrm{LD0}} + I_{\mathrm{LD1}}) \tag{7}$$

where $V_{\mathrm{PD}}$ is the bias voltage for the PD. Therefore, power dissipation of the transmitter and receiver required for error-free operation is calculated using (5) to (7). In the preamplifier configuration, the total power dissipation can be determined by adding the power dissipation of the preamplifier to (7).

### C. Power Dissipation Versus Transmission Bit Rate

The PD-DEC was compared to the amplifier configuration taking power and bandwidth into consideration. The parameters we used are listed in Table I, which were determined by referring to devices operating in 10 Gb/s transmission systems and typical optical devices for long wavelength transmission. The $\eta_t$ is a product of an $\eta_{\mathrm{LD}}$ of 0.2 W/A, an $\alpha$ of 70%, and an $\eta_{\mathrm{PD}}$ of 0.7 A/W. Each process-deviation is restricted within 9% $(= 3k)$ from the mean value. The results are shown in Fig. 3. The bandwidth of the PD-DEC was calculated from the time constant determined by the parasitic capacitance of the PD ($C_{\mathrm{PD}}$: including the gate capacitance of the DEC) and the load resistance $R$. The maximum transmission bit rate is defined as

TABLE I

| parameter | | | value |
|---|---|---|---|
| Total Efficiency | $\eta_t$ | - | 0.1 |
| Process Std. Deviation | $b$ | % | 3 |
| | $k$ | - | 3 |
| Total Noise Current | $I_n$ | μA | 5 [22] |
| Decision Sensitivity | $V_{sen}$ | mV | 40 [23] |
| Vref Std. Deviation | $\sigma_{ref}$ | mV | 10 |
| LD Drive Current | $I_{LD0}$ | mA | 1.0 |
| LD Threshold Current | $I_{th}$ | mA | 10 @30℃ |
| Characteristic Temperature | $T$ | K | 50 [24] |
| Temperature | $T_o$ | ℃ | 0~80 |
| Bias Voltage for Driver | $V_{dr}$ | V | 3 |
| Bias Voltage for PD | $V_{PD}$ | V | 2 |

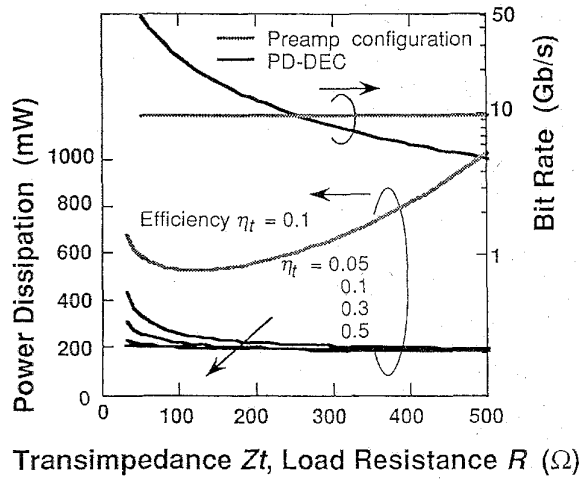


Fig. 3. Comparison between the PD-DEC and the preamplifier configuration.

$(4C_{\mathrm{PD}}R)^{-1}$. A $C_{\mathrm{PD}}$ of 0.1 pF was assumed (A PD with 20 μm diameter and 2 μm thickness, and a MESFET with 50 μm gate width at the input node of the DEC were assumed). The power dissipation of the preamplifier was estimated by SPICE simulation for a GaAs preamplifier [17] at a fixed bandwidth of 10 GHz. The minimum dissipated power required for error-free operation is plotted as a function of transmission bit rate using total efficiency as a parameter. The PD-DEC reduces power dissipation to below 350 mW in the region of $R > 50$ Ω, which is less than half that of the amplifier configuration. The value of $I_{\mathrm{LD1}}$ for $R = 100$ Ω was below 60 mA in the efficiency range from 0.05 to 0.5 as shown in Fig. 3. This $I_{\mathrm{LD1}}$ value is practicable by using an actual driver IC, thus error-free operation in the PD-DEC is confirmed.

The LD drive current $I_{\mathrm{LD1}}$ can be reduced by increasing the load resistance $R$ because the output level is product of $I_{\mathrm{LD1}}$, total efficiency $\eta_t$, and $R$. On the other hand, increasing the total efficiency $\eta_t$ to 0.3 effectively contributes to reducing the power in the lower $R$ region which is suitable for high-speed operation. In the case where $\eta_t$ is higher than 0.3, the contribution of $\Delta I_{\mathrm{th}}$, the first term on the right-hand side in (5), becomes dominant. Therefore, in adding to improving $\eta_t$, reducing the temperature-dependent deviation in the threshold current $\Delta I_{\mathrm{th}}$ is also effective in reducing the power dissipation. To reduce the $\Delta I_{\mathrm{th}}$, reduction of $I_{\mathrm{th}}$ is

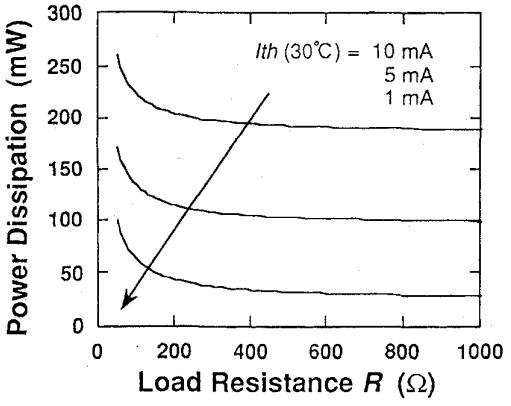


Fig. 4. Power dissipation of the PD-DEC versus load resistance $R$. Power dissipation can be reduced by decreasing $I_{\rm th}$.

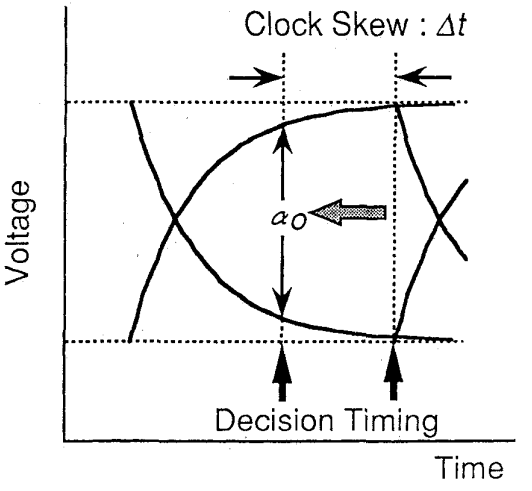


Fig. 5. Schematic diagram of the attenuation coefficient $\alpha_o$ and clock skew.

important. The dependence of the power dissipation of the PD-DEC on $I_{\rm th}$ which is a dominant factor of $\Delta I_{\rm th}$ is shown in Fig. 4. The total efficiency $n_t$ was 0.1 and the other parameters were all the same as those in the analysis in Fig. 3. The power dissipation can be reduced to 1/5 by reducing $I_{\rm th}$ to $1/10$.

From this analysis, it is evident that the PD-DEC, one of the simplest configurations based on the excess bias/drive operation, can achieve error-free operation in commercially available devices. Furthermore, power dissipation of the PD-DEC is lower than that of the preamplifier configuration. This means the PD-DEC has the advantage of lower power dissipation than other optical configurations including compensation circuits.

### *D. Extra Power Dissipation Due to Clock Skew*

Clock skew is a serious problem in cases where the clock signal is distributed to each decision circuit. Deviation in optical-fiber length causes clock skew. Clock skew reflects decreases in the level margin with fluctuations in decision timing as shown in Fig. 5. This extra loss $\alpha_o$ is introduced into the efficiency parameter $\eta_t$ which is rewritten as $\eta_t = \alpha\alpha_o\eta_{\rm LD}\eta_{\rm PD}$. Fig. 5 shows the relation between $\alpha_o$ and clock skew. In optical interconnections, signal distortions caused by wavelength dispersion in optical fibers are negligible. Therefore, the signal rise and fall times of the PD-DEC do not depend on interconnection lengths. They are determined solely by the CR time constant of the parasitic capacitance $C_{\rm PD}$ and load resistance $R$. The $\alpha_o$ is given by

$$\alpha_o = 1 - 2\exp\left(\frac{\Delta t}{C_{\rm PD}R} - 4\right) \tag{8}$$

where $\Delta t$ is the clock skew. The extra power dissipation due to the clock skew of the PD-DEC can be calculated by using (5) to (8).

The extra power dissipation of the PD-DEC related to clock skew is shown in Fig. 6. In this figure, clock skew is normalized by a clock period $T_p$ of $4C_{\rm PD}R$. The power penalty is very small, below 0.5 dB, even with a large clock skew of up to $0.5T_p$.

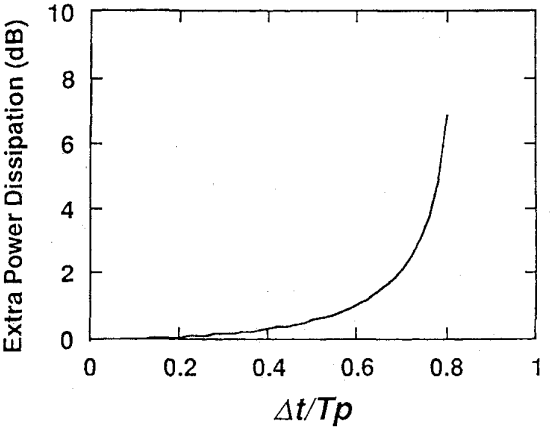


Fig. 6. Power penalty of the PD-DEC due to clock skew.

### *E. Verification of the Model*

To quantitatively verify this model-based analysis, a mixed photonic/electronic circuit simulator [26] was used. This simulator can simulate the combination optical devices, for example, LD's, PD's, and optical fibers with electronic devices. Therefore, analysis reflecting device physics, such as the relaxation oscillation of the LD, can be performed. The photonic/electronic simulator can also perform noise analysis in time domain by using transient-noise-current sources. In noise analysis, the bit error rate is estimated by calculating the distribution of sampled signal levels from simulated eye diagrams.

We spbimulated time-domain response for the PD-DEC shown in Fig. 1(b) for several values of $I_{\rm LD1}$ using the photonic/electronic simulator. A LD was directly modulated by a driver circuit with an NRZ pseudo-random bit stream of $2^7 - 1$. An attenuated optical signal was received by the PD with a parasitic capacitance of 0.1 pF. The photocurrent was converted into a voltage signal by a load resistance. Simulated incident-light and transmitted-voltage eye diagrams

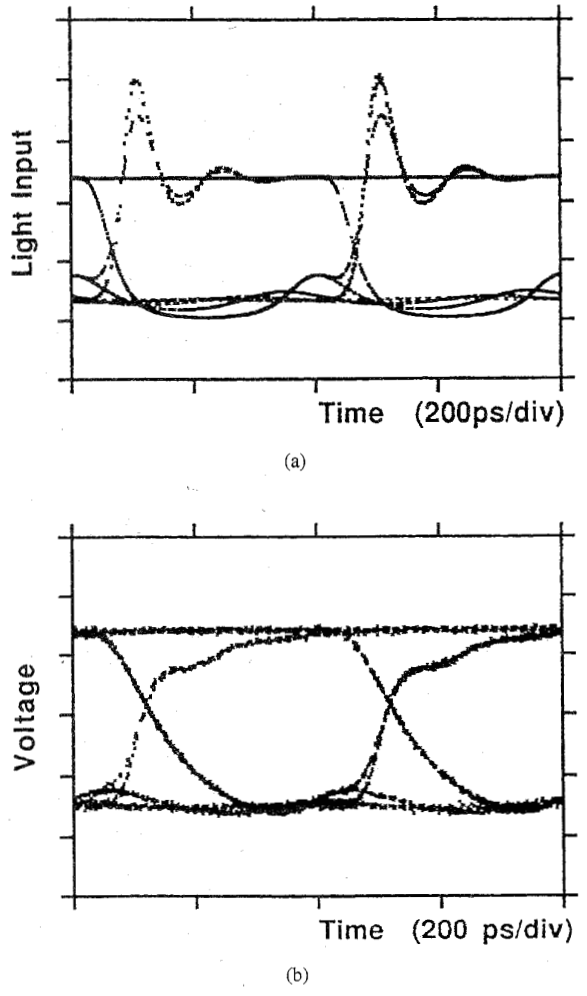


Fig. 7. Simulated eye diagrams for a 2.5 Gb/s input pseudo random NRZ data stream: a) Light input for the PD-DEC, and b) Voltage signals converted by the load resistance $R$. $R = 1000\ \Omega$, $C_{\rm PD} = 0.1$ pF, $I_{\rm th}(30°{\rm C}) = 1$ mA, and $T = 80°{\rm C}$ are assumed.

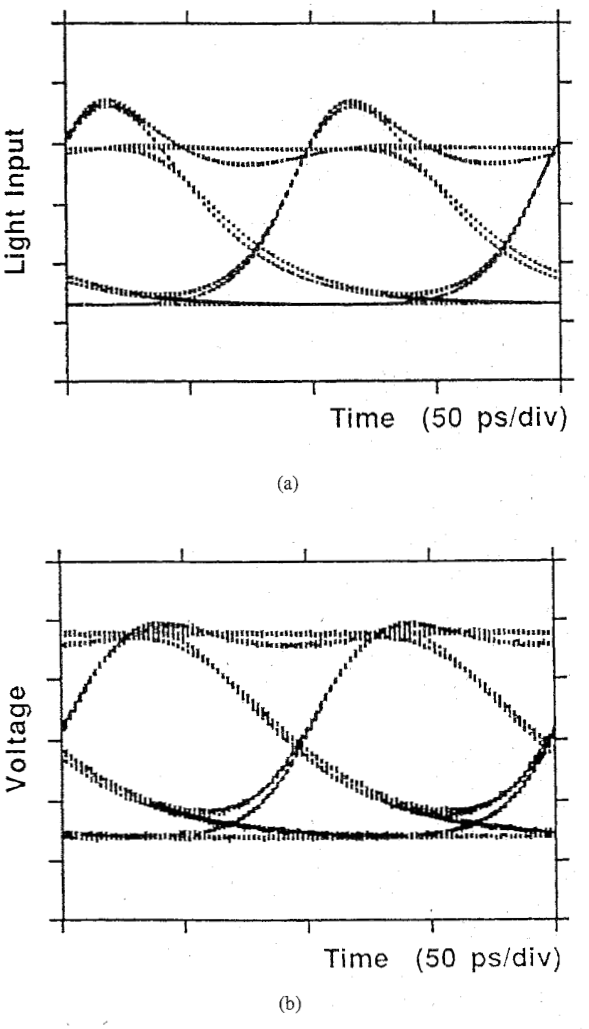


Fig. 8. Simulated eye diagrams for 10 Gb/s input pseudo random NRZ data stream: a) Light input for the PD-DEC, and b) Voltage signals converted by the load resistance $R$. $R = 250\ \Omega$, $C_{\rm PD} = 0.1$ pF, $I_{\rm th}(30°{\rm C}) = 1$ mA, and $T = 80°{\rm C}$ are assumed.

for the PD-DEC at 2.5 Gb/s are shown in Fig. 7(a) and (b), respectively. In this case, where the transmission bit rate is lower than the modulation bandwidth of the LD, the influence of the LD relaxation oscillation is negligible. Simulated incident-light and transmitted-voltage eye diagrams for the PD-DEC at 10 Gb/s are shown in Fig. 8(a) and (b), respectively. It is clear that the pattern jitter grows as the bit rate approaches the relaxation oscillation frequency of the LD. However, the eye is still clearly open for the 10-Gb/s signals.

By using these simulated eye diagrams, the bit error rates of the PD-DEC under process deviation, temperature fluctuation, noise, and pattern jitters were calculated. Fig. 9 compares the results with those obtained by the model-based analysis. For 2.5 Gb/s signals, there is good agreement, within an 8% error, in the power dissipation of transmitters. The slightly higher power dissipation calculated by photonic/electronic simulation was due to pattern jitters of the LD. The results for 10 Gb/s signals show this tendency becomes stronger with increasing bit rate: the error grows to 15%. In this paper, we assume the bandwidth of each device is much wider than the bit rate. This simplified model can evaluate system performance near the performance limits of devices within a 15% error. If the bit rate is close to the relaxation oscillation frequency, the power penalty due to pattern jitters must be considered.

## IV. Comparison Between Optical and Electrical Interconnections

### A. Modeling for Electrical Interconnections

As with optical interconnections, we used our model in electrical interconnections. We ignored ECL interface and calculated the minimum power dissipation to achieve error-free operation. The model and parameters used for electrical interconnections with coaxial cable are shown in Fig. 10. This model is basically the same as the one used for optical

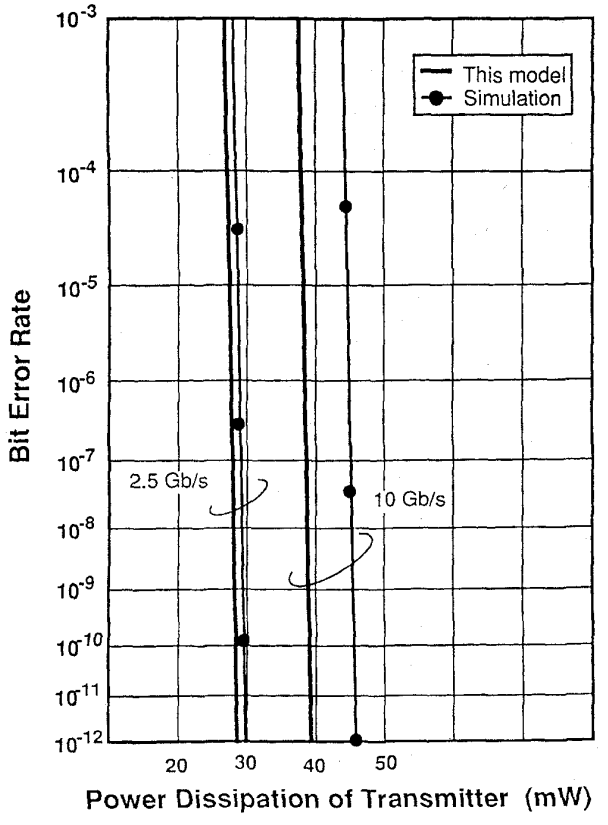


Fig. 9. Estimated bit-error-rate performance for the PD-DEC using this model and photonic/electronic simulator.

interconnections. The parameters for distribution and noise are the same as those used before.

Some parameters, however, are different. The temperature fluctuation factors were ignored because the temperature fluctuation is not as large as the threshold current of the LD. The matching resistance $R_m$ was fixed at 50 Ω and the return loss was considered. The effect of the return loss was represented by the reflection coefficient $\rho$, assumed to be 0.1. Signal distortion due to the skin effect cannot be considered negligible in electrical interconnections using coaxial cables, so this was also considered in estimating the power dissipation.

The power dissipation of the driver dominates the total power dissipation of the transmitter and receiver shown in Fig. 10. Again, we calculate the power dissipation of the driver required to achieve error-free operation.

Signal deviations at the input node of the decision circuit $\sigma_{Ve1}$ and $\sigma_{Ve0}$ resulting from all the deviation factors can be approximated by a Gaussian distribution and their standard deviations are given by

$$\sigma_{Ve1} = I_1 R_m \left\{ \left( \frac{\sigma_{Rm}}{R_m} \right)^2 + \left( \frac{\sigma_{I1}}{I_1} \right)^2 \right\}^{\frac{1}{2}}, \quad (9\text{-}1)$$

$$\sigma_{Ve0} = I_0 R_m \left\{ \left( \frac{\sigma_{Rm}}{R_m} \right)^2 + \left( \frac{\sigma_{I0}}{I_0} \right)^2 \right\}^{\frac{1}{2}}. \quad (9\text{-}2)$$

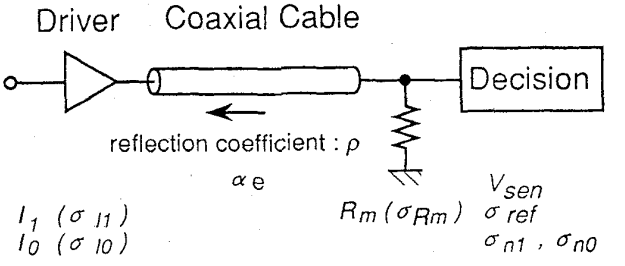


Fig. 10. Schematic diagram of electrical interconnections with coaxial cable.

When the signal deviation is restricted by screening, within $k$ times of each standard deviation, the effective signal amplitude $V_{E\text{eff}}$ can be represented by

$$V_{E\text{eff}} = \alpha_e[\{I_1 R_m(1-\rho) - k\sigma_{Ve1}\} - \{I_0 R_m(1+\rho) + k\sigma_{Ve0}\}]. \quad (10)$$

The attenuation coefficient $\alpha_e$ gives the influence of the signal distortion caused by the skin effect and clock skew. Contribution of the skin effect will be discussed later. The effective signal amplitude must satisfy

$$V_{E\text{eff}} \geq V_{\text{sen}} + 2k\sigma_{\text{ref}} + Q(\sigma_{n1} + \sigma_{n0}). \quad (11)$$

The drive current $I_1$ for coaxial cables can be obtained from (9) to (11) as

$$I_1 \geq \frac{1 + \frac{\sqrt{2}kb}{100} + \rho}{1 - \frac{\sqrt{2}kb}{100} - \rho} I_0 + \frac{2xI_n}{\alpha_e\left(1 - \frac{\sqrt{2}kb}{100} - \rho\right)} + \frac{V_{\text{sen}} + 2k\sigma_{\text{ref}}}{\alpha_e\left(1 - \frac{\sqrt{2}kb}{100} - \rho\right)R_m}. \quad (12)$$

The first term on the right-hand side represents the influence of process standard deviations, the second term is the noise contribution, and the third term represents the effective sensitivity of the decision circuit. The power dissipation of electrical interconnections is obtained as the product of $I_1$ and the bias voltage for driver $V_{\text{dr}}$.

The signal distortion due to the skin effect seriously restricts transmission bit rates and interconnection lengths. The penalty due to signal distortion gives the attenuation coefficient $\alpha_e$. $\alpha_e$ means loss in the pulse-response waveform of a coaxial cable with fluctuations in decision timing. This waveform can be calculated from the transfer function of a coaxial cable considering the skin effect [27]. The transmission parameters of the transfer function can be determined from catalogued data of $\sqrt{f}$ characteristics of typical coaxial cables. For 3 mm-diameter cable, $\alpha_e$ becomes 6.4 dB for 2 Gb/s and 10 m interconnections.

### *B. Transmission Bit Rates and Interconnection Lengths Where Optical Interconnections are Superior*

The power dissipation of optical and electrical interconnections was calculated using the proposed models. The results are

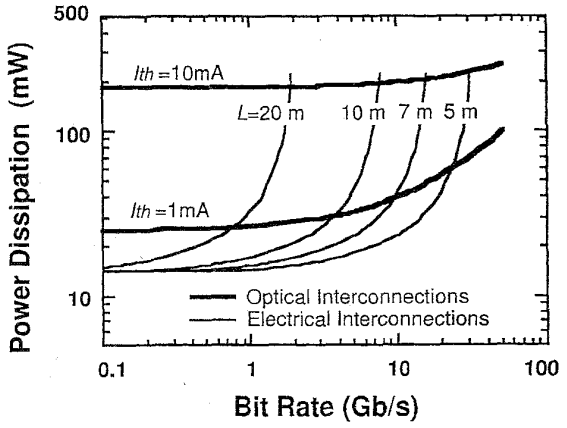


Fig. 11. Power dissipation of optical and electrical interconnections versus bit rate. The coaxial cable was 3 mm in diameter.

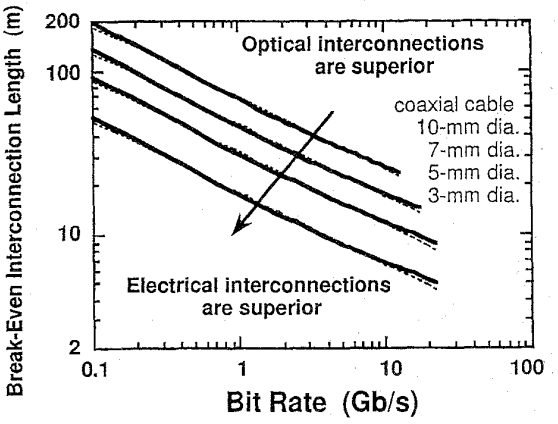


Fig. 12. BEIL versus bit rate. Solid lines are calculated by this model. Dotted lines are calculated by using (13).

shown in Fig. 11. An $I_{\rm th}$ of 1 mA and $C_{\rm PD}$ of 0.1 pF were assumed. Clock skew was ignored because the extra power dissipation of the PD-DEC due to clock skew is negligible.

It can be seen that the power dissipation in electrical interconnections is lower than in optical interconnections for lower bit rates and shorter interconnection lengths. However, electrical interconnections show a drastic increase in power due to the skin effect at higher bit rates. Therefore, the power dissipation in electrical interconnections becomes larger than that in optical interconnections. In this comparison, signal rise time does not depend on signal amplitude. However, increases in power dissipation in electrical interconnections will generally be more significant because the signal slew rate degrades with increasing amplitude.

We define the interconnection length at which optical and electrical interconnections have the same power dissipation as the break-even interconnection length (BEIL). BEIL versus the bit rate is shown in Fig. 12 with solid lines. The power dissipation was calculated for a $I_{\rm th}$ of 1 mA and $C_{\rm PD}$ of 0.1 pF. At lengths longer than the BEIL, optical interconnections have smaller power dissipation than electrical interconnections. In the case of 10 Gb/s signal transmission, optical interconnections are superior in terms of power dissipation to electrical interconnections, exhibiting a power dissipation of about 40 mW at a 7 m length. From Fig. 12, it is found that the relation between BEIL and bit rate is approximated by

$$\text{BEIL} = L_0(\text{bit rate})^{-m} \tag{13}$$

where $m$ is a fitting parameter and $L_0$ is a BEIL at 1 Gb/s transmission. The parameter $m$ has a value of near 0.5 because signal loss due to the skin effect has $\sqrt{f}$ characteristics. In this analysis, $m$ had a value of 0.44. $L_0$ depends on diameter of coaxial cables, and is 18.3 m for a cable with a diameter of 3 mm. The dotted lines in Fig. 12 are calculated by using (13). They have good agreement with the results of solid lines.

Practical systems often require multiple fan-in/fan-out interconnections. Several unique methods such as WDM transmission have been proposed for multiple fan-in/fan-out optical interconnections [5]–[7]. In these interconnections, several outputs of optical transmitters are multiplexed in one optical path then divided into several inputs for optical receivers. The model proposed in this paper can be easily extended to handle multiple fan-in/fan-out interconnections. Power dissipation of such interconnections ($N$-fold fan-in and/or fan-out) can be estimated by multiplying the power dissipation of a transmitter and/or receiver by $N$ because the power penalty due to crosstalk and impedance mismatching are negligible in optical interconnections. In the case where $N$-fold fan-out in an optical path is required, the power dissipation of the transmitter and the receiver can be obtained by replacing the total efficiency $\eta_t$ in (4) with $\eta_t/N$.

## V. Conclusion

We have proposed a novel model considering practical operating conditions to analyze the power dissipation related to the transmission bit error rate of the interconnection systems. We have analyzed the power dissipation for both optical and electrical interconnections using the parameters in Table I. The following results were obtained.

1) The PD-DEC can achieve error-free operation under practical operating conditions including process deviation, temperature fluctuation, and noise.
2) The PD-DEC is superior in terms of power dissipation to the configurations using preamplifier and/or compensation circuits.
3) The break-even interconnection length is proportional to $(\text{bit rate})^{-0.44}$.
4) The PD-DEC configuration is superior in terms of power dissipation to electrical interconnections at 10 Gb/s for lengths beyond 7 m.
5) Power dissipation of the PD-DEC can be reduced to 1/5 by improving total efficiency up to 0.3 and reducing $I_{\rm th}$ to 1 mA.

These results are based on simplified cases excluding pattern jitters and crosstalk. However, the extra power dissipation related to pattern jitters and bandwidth limits of each device

will become increasingly important as the bit rate becomes higher. The crosstalk will become a serious problem as the density of an interconnect array becomes higher. These are subjects for further study.

## APPENDIX

Output levels of the PD-DEC are given as the product of each device parameter. Therefore, process-dependent output-level deviation is given as the product of each process-standard deviation $\sigma$. Let us consider two parameters, $x$ and $y$, whose distributions are assumed to be Gaussian. The means and standard deviations of $x$ and $y$ are defined by $x_o$, $y_o$ and $\sigma_x$, $\sigma_y$, respectively. In this paper, we approximate the mean and standard deviation of a product of $x$ and $y$ as follows

$$\text{Mean} = x_o y_o,$$

$$\text{Standard Deviation} = \{(x_o\sigma_y)^2 + (y_o\sigma_x)^2\}^{1/2} = x_o y_o \left\{ \left(\frac{\sigma_x}{x_o}\right)^2 + \left(\frac{\sigma_y}{y_o}\right)^2 \right\}^{1/2}.$$

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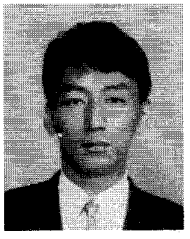

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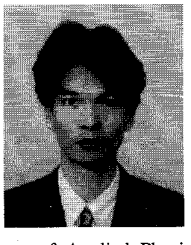

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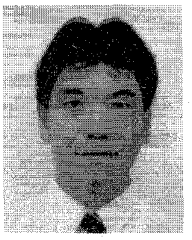

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