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High-Speed and Low-Power Operation of a Resonant Tunneling Logic Gate MOBILE

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***Abstract*— High-speed operations up to 35 Gb/s were demonstrated for a resonant tunneling (RT) logic gate monostable-bistable transition logic element (MOBILE). The test circuit consisted of a MOBILE and a DCFL-type output buffer, and it was fabricated using InP-based resonant tunneling diode/HEMT integration technology. This operation bit rate is close to the cutoff frequency of the 0.7-μm gate HEMT's used in the circuit, and was obtained after improvement of the output buffer design. This result indicates the high-speed potential of the MOBILE, though the speed is still limited by the buffer. The power dissipation of the MOBILE was also discussed based on a simple equivalent circuit model of RTD's. This revealed that the power dissipation is as small as 2 mW/gate over a wide range of operation bit rates.**

I. Introduction

RECENTLY, a variety of circuit applications for resonant tunneling diodes (RTD's) have been reported, which exploit functions arising from their negative differential resistance (NDR) [1]–[4]. We introduced a highly functional logic gate, called a MOBILE (monostable-bistable transition logic element) [5], and demonstrated several circuit applications [6], [7]. Along with functionality, one of the most significant features that makes the MOBILE attractive is its potential for high-speed operation. We recently demonstrated an 18-Gb/s operation in a MOBILE flip-flop [8] fabricated with InP-based RTD/HEMT integration technology [9]. This bit rate was restricted by the bandwidth of the output buffer circuit, and the intrinsic operation speed close to the cutoff frequency (f_T) of the HEMT used was expected for the MOBILE itself [10]. In this letter, we demonstrated a high-frequency operation of a MOBILE up to 35 Gb/s, which is close to the f_T of the 0.7-μm gate length HEMT used in the circuit. The power dissipation of the MOBILE is also discussed based on simple calculation.

II. Devices and Test Circuit

Details of the operating principles of MOBILE's have previously been reported [5]. The key point is that they employ the monostable-to-bistable transition of a circuit consisting of two serially connected NDR devices, and this circuit is driven by oscillating the bias voltage to produce the transition. It should be emphasized here that the MOBILE switches its state only at the rising edge of the bias voltage (it works as a clock) and maintains its state while the bias voltage is high. The NDR devices must have the mechanism to modulate its peak current according to the input. We used an RTD and HEMT parallel circuit for this NDR device [9].

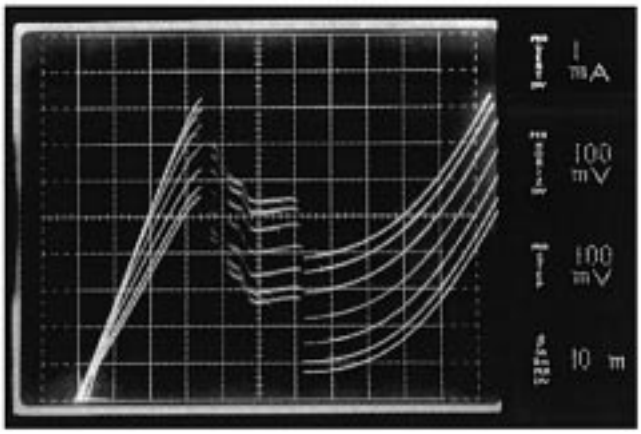

Fig. 1. The I–V characteristics of the RTD/HEMT parallel circuit at room temperature. The size of the RTD is 2×3 μm^2. The maximum gate voltage is 0.6 V with a 0.1 V step. The gate length and width are, respectively, 0.7 and 10 μm.

The devices were fabricated on MBE-grown epitaxial layers on an InP substrate. These layers had an RTD structure on an HEMT structure. The structures were similar to those reported in [9] except that the etch stop layer is made up of AlAs. The RTD structure had 1.6-nm strained AlAs barriers and an 1.8-nm InAs strained subwell at the center of $In_{0.53}Ga_{0.47}As$ well. The total well thickness was 4.4 nm, and the emitter/collector doping concentration was 1×10^{18} cm^{-3}. Undoped spacer layers of 1.5-nm thickness were grown outside the barriers. The devices were fabricated with the conventional wet etching and lift-off process. The buried Pt-gate process was used to obtain near enhancement mode HEMT's [11]. Fig. 1 shows the I–V characteristics of the RTD/HEMT parallel circuit we fabricated. The peak current can effectively be modulated by the input voltage. The gate length and width of the HEMT used were 0.7 μm and 10 μm, respectively, and the area of the RTD was 2×3 μm^2. The peak current density and peak-to-valley ratio of the RTD were 9.3×10^4 A/cm^2 and 9, respectively. The f_T of the HEMT measured with a 100-μm gate width device was about 40 GHz.

Fig. 2 shows the configuration of the fabricated circuit. It consists of a MOBILE core and a DCFL-type output buffer. Although this is a simple circuit to test the high-speed

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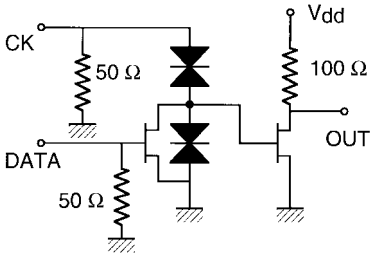

Fig. 2. Circuit configuration for the fabricated test circuit. The areas of upper and lower RTD's are 2×3.7 and 2×3 μm^2, respectively.

operations of a MOBILE, it does have a practical use. The MOBILE core works as a delayed flip-flop (D-FF) with a return-to-zero (RZ) mode complement output. Therefore this circuit can be regarded as a "return-to-one" (RO) mode D-FF. The output buffer is indispensable in minimizing the influence of the measuring system on MOBILE operation, because the measuring system is 50 Ω-terminated. The output buffer was changed from that reported in [8], where the buffer limited the speed, so that the intrinsic speed of the MOBILE could be tested at the expense of output amplitude. The areas of the RTD's were 6 μm^2 and 7.4 μm^2 for lower and upper devices, respectively.

III. Results and Discussion

A data stream and a clock pulse up to 35 Gb/s (GHz) were fed into the circuit to test high-speed operation. Two multiplexers were used to obtain a data stream with a bit rate higher than 20 Gb/s, because the bit rate of commercially available pulse pattern generators is limited to around 10 Gb/s. A complementary pair of data streams from a pulse pattern generator was delayed and fed into the first multiplexer, then, its outputs were again delayed and fed into the second multiplexer, which was comprised of InP-based HEMT's and was capable of 40 Gb/s operation [12].

Fig. 3(a) shows the results of operation with the input of a pseudo-random bit stream at 35 Gb/s. Clear RO mode eye-patterns were obtained at this bit rate. The relatively small output amplitude of about 50 mV is due to the design of the output buffer circuit. The inner logic swing is estimated to be around 0.6 V. Fig. 3(b) shows the result at 35 Gb/s with an input bit pattern of (0 111 010 000 101 110). (The upper trace is the complement of the input data stream.) This figure confirms proper operation. This operation speed is close to the f_T of the HEMT used in the circuit.

As this circuit uses a clock pulse as an oscillating bias voltage for the MOBILE, measuring power dissipation is not straightforward. The power dissipation of the MOBILE was therefore estimated from a simple equivalent circuit calculation. In this calculation the RTD's were modeled as a parallel circuit of voltage dependent capacitance and a voltage dependent current source. Schulman's model [13] was used for the current source, and it was fitted to the experimental I–V curve. The capacitance of the RTD was modeled with a simple approximation that all collector voltage drops in the collector layers. This was about 4 fF/μm^2 around the peak voltage. Fig. 4 shows the calculated power dissipation of the core

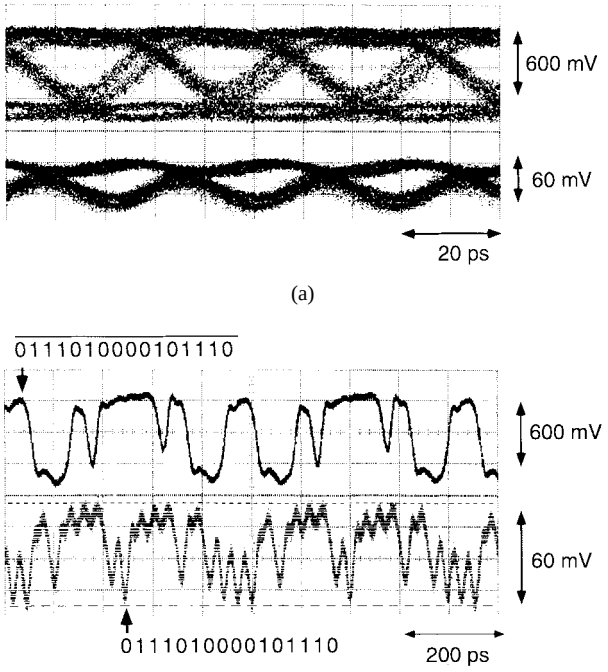

Fig. 3. The complement of the input data stream (upper trace) and the output (lower trace) signal of the fabricated circuit: (a) response to the input of pseudo random bit stream and (b) response to the input bit pattern (0 111 010 000 101 110).

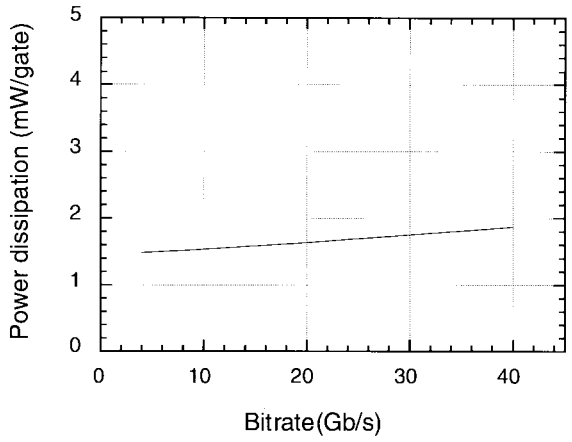

Fig. 4. The estimated power dissipation of the core circuit as a function of bit rate.

circuit, which consists of a MOBILE and the input capacitance of the next stage, as a function of the operation frequency. In this calculation, the clock amplitude was set to be 0.7 $V_{\text{p-p}}$ with a dc bias of 0.55 V. We think this is close to the experimental condition, though the exact value could not be determined due to the impedance mismatching. The power dissipation is less than 2 mW/gate. This is extremely small compared to a few tens of mW for a high-speed SCFL logic gate [14]. Moreover, this difference extends several times if one compares it to the core circuit of an SCFL D-FF. This small power dissipation results from the small valley current as well as the small supply voltage. In fact, the large current corresponding to the peak current of the RTD flows only at the rising and falling edge

of the clock, and the small current corresponding to the valley flows while the clock is high. Furthermore, this figure shows that the power dissipation has only limited dependence on the bit rate. This is because the capacitance of the RTD's is so small that, in this frequency range, the dynamic current is much smaller than the static current.

IV. Summary

A resonant tunneling logic circuit employing a MOBILE was fabricated with RTD/HEMT integration technology on an InP substrate. High-speed operations up to 35 Gb/s were demonstrated in HEMT's having a relatively large gate length of 0.7 μm. Moreover, simple simulation revealed small power dissipation in the MOBILE over a wide range of operation frequencies.

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