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Static Frequency Divider Featuring Reduced Circuit Complexity by Utilizing Resonant Tunneling Diodes in Combination with HEMT's

Kunihiro Arai, Hideaki Matsuzaki, Koichi Maezawa, *Member, IEEE,*
Taiichi Otsuji, and Masafumi Yamamoto, *Member, IEEE*

Abstract— A static frequency divider constructed with resonant tunneling diodes (RTD's) in combination with HEMT's is proposed and demonstrated. The circuit complexity is reduced drastically. The proposed circuit is fabricated using InP-based RTD/HEMT monolithic integration technology. Proper operation is demonstrated at room temperature by a quasi-static test pattern.

The circuit includes two sub-circuits which behave like D-latches. Each sub-circuit consists of only three components. This number of components is one fifth of that required to construct a D-latch using conventional SCFL technology. The strong nonlinear I−V characteristics of RTD's are fully utilized for this reduction.

I. INTRODUCTION

HIGH-SPEED digital IC's have recently reached 40 GHz operation in static binary frequency dividers using In-AlAs/InGaAs HEMT's with 0.1-mm gate length [1], [2]. The inherent problem with these circuits is the relative increase in the transmission delay time caused by the interconnection. One of the approaches to overcome this problem is to reduce circuit complexity and interconnection line length. We propose, and demonstrate here, the use of resonant tunneling diodes (RTD's). Static frequency dividers are constructed by RTD's in combination with HEMT's. The circuit complexity is reduced and the interconnection line length is shortened. The basic operation mechanism of the present circuit is confirmed.

II. CIRCUITS AND OPERATION MECHANISM

The circuit diagram of the proposed static binary frequency divider is shown in Fig. 1(a). The divider consists of two sub-circuits for the first and second logic stages and a conventional HEMT inverter for the third stage. The output of the third stage is fed to the first stage. The essential part of the sub-circuit is composed of a load and driver element as shown in Fig. 1(b). The load element is an RTD. The driver element is a parallel connection of an RTD and a HEMT. The driver current of the sub-circuit can be modulated by the input bias, V_{in}. The sub-circuit is a monostable-bistable transition logic element, or MOBILE, which has been applied as a logic gate [3], [4]. The sub-circuit, with only three components, effectively functions
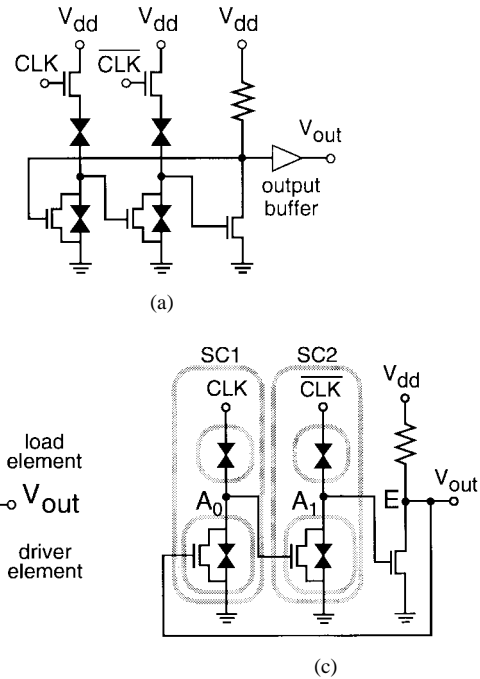
Fig. 1.   Circuit diagrams: (a) present circuit, (b) sub-circuit, and (c) simplified circuit.

as a D-latch in the circuit. Three components are far fewer than the fifteen required to construct a D-latch using conventional SCFL technology [1], [2].

The sub-circuit operates as follows. The peak of the driver current is designed to be smaller (larger) than that of the load current when V_{in} is in the logic low (high) level, L (H). For V'_{dd} appropriately chosen like V'_{dd1} in Fig. 2(a), two stable operating points appear for a given V_{in}: for $V_{in} = H$, V_1 and V_3, and for $V_{in} = L$, V_2 and V_4. The logic low and high levels are then assigned to the voltage region around V_1 and V_2, and that around V_3 and V_4. In contrast, when V'_{dd} is L, i.e., for example $V'_{dd} = V'_{dd2}$, only one operating point appears for a given V_{in}: for $V_{in} = H, V_5$ and for $V_{in} = L, V_6$. The sub-circuit operation is summarized by the three principles listed below, provided that V_{in} is in the range between L and H.
1) While V'_{dd} is H, the logic level of V_{out} remains unchanged.
2) When V'_{dd} is L, V_{out} is L. 3) The inverse of V_{in} appears at V_{out} when V'_{dd} changes from L to H.
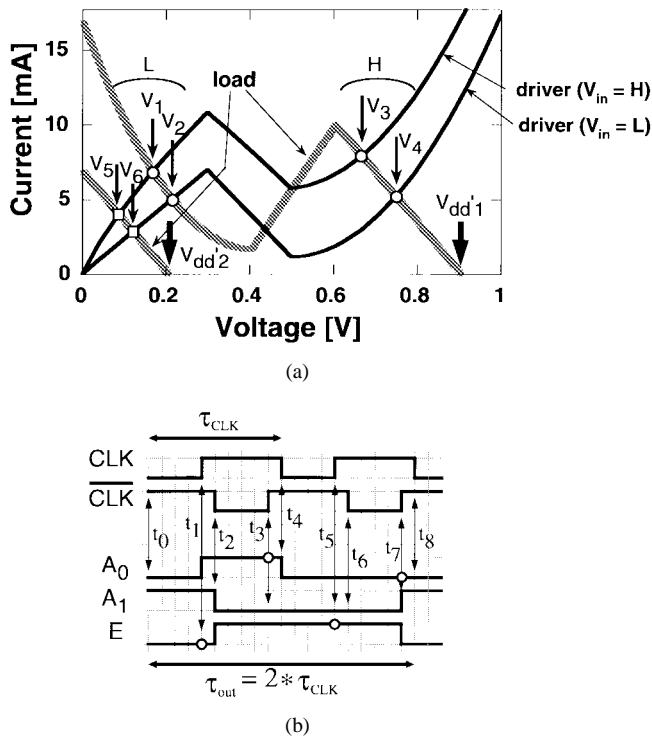
(a)

(b)

Fig. 2. Operation mechanism. (a) Load diagram for the sub-circuit: Two driver characteristics are plotted corresponding to $V_{in} = H$ and L. The two load curves correspond to the applied biases of V'_{dd1} and V'_{dd2}. For a given V_{in}, there are two stable points when $V'_{dd} = V'_{dd1}$. In contrast, only one stable point exists when $V'_{dd} = V'_{dd2}$. (b) Timing diagram for the simplified circuit [Fig. 1(c)] with definitions of CLK and $\overline{\text{CLK}}$. The period of CLK is τ_{CLK}. The times $t_1, t_2, \cdots t_8$ are the rising edges or falling edges of CLK or $\overline{\text{CLK}}$ pulses, and are important for understanding the circuit behavior. A_0, A_1 and E are node potentials derived by principles 1), 2), and 3) in the text. The period of double τ_{CLK} shows the static binary frequency divider operation of the simplified circuit.

While V'_{dd} is H, transitions between the logic low and high levels never occur. This is because the variation of the driver characteristics is limited to the range between the two curves for $V_{in} = L$ and $V_{in} = H$ in Fig. 2(a). Thus, principle 1) is reasonable. Principle 2) is obvious. When V'_{dd} is in the logic low level like V'_{dd2}, the operating points are always between zero and V'_{dd2}, i.e., in the logic low level. For principle 3), assume V_{in} is H (L). Then, the peak current of the driver element is larger (smaller) than that of the load element. During the V'_{dd} sweep, the potential drop across the driver (load) element is smaller than the peak voltage of that element. Thus, after the V'_{dd} change, the operating point becomes $V_1(V_4)$ in the logic low (high) level.

Next, the timing diagram of a simplified circuit [Fig. 1(c)] is discussed. Here, the input signals to the sub-circuits, CLK and $\overline{\text{CLK}}$, are assumed as in Fig. 2(b) with a period of τ_{CLK}. Notice that there are overlapping periods between CLK and $\overline{\text{CLK}}$ pulses like the period between t_1 and t_2. The nodes which play the roles of V'_{dd}, V_{in}, and V_{out} in the sub-circuit, SC1, are CLK, E (the inverse of A_1), and A_0. Those for SC2, are $\overline{\text{CLK}}, A_0$, and A_1. Initially, i.e., at t_0, A_0, and A_1 are assumed to be L and H, respectively. The diagram [Fig. 2(b)] is derived by applying the above principles to the times when CLK or $\overline{\text{CLK}}$ varies like $t_1, t_2, \cdots$, etc.
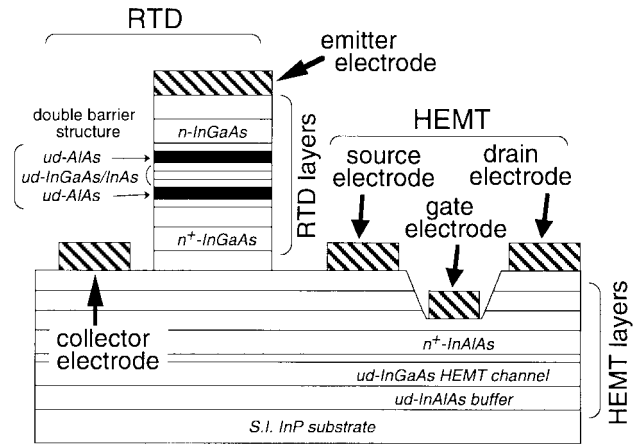

Fig. 3. Schematic cross section of the present device. InGaAs/InAs/AlAs resonant tunneling diodes and InAlAs/InGaAs HEMT's are monolithically integrated on a semi-insulating InP substrate. Epitaxial layers are grown by a molecular beam epitaxy method. The RTD junction area is 2×5 μm^2 and the gate length of the HEMT's is 0.7 μm. The RTD exhibited a high peak current density of 1.2×10^5 A/cm^2 with a good peak-to-valley current ratio of 12. The peak voltage was 0.35 V. The HEMT also exhibited a high transconductance of 900 mS/mm with a threshold voltage of -0.1 V.

At t_1, CLK rises from L to H. This means V'_{dd} for SC1 rises. Because V_{in} for SC1, i.e., the inverse of A_1, is L at this moment, V_{out} for SC1, i.e., A_0 becomes H (principle 3). This means the input of SC2 changes, because A_0 is the input for SC2 as well. However, the SC2 output, i.e., A_1, keeps the initial value, H (principle 1). Thus, principle 1) guarantees proper circuit operation by protecting A_1 against being affected by the change A_1 itself brings about. At $t_2, \overline{\text{CLK}}$, i.e., V'_{dd} for SC2, falls from H to L. Then, SC2 output, i.e., A_1 becomes L (principle 2), changing the SC1 input from L to H. Again, principle 1) forbids SC1 output to change and guarantees stable circuit operation. The behaviors at $t_3, t_4, \cdots t_8$ can be understood similarly on the basis of the three principles. At t8, the simplified circuit recovers the initial state at t_0, showing the period of the circuit is double τ_{CLK}. Thus, the circuit is a 1/2 frequency divider. In the present circuit [Fig. 1(a)], the CLK is connected to the gate of a HEMT inserted between the power supply, V_{dd}, and the sub-circuit. However, this difference is not essential if the voltage drop between the source and drain electrodes of the HEMT is sufficiently large (small) for CLK $= L$ (H).

III. EXPERIMENTS AND RESULTS

The circuits were fabricated using InP-based RTD and HEMT integrated device technology [4]. A schematic cross section is shown in Fig. 3. The double barrier structure for the RTD's consists of an InGaAs (1.2 nm)/InAs (2.2 nm)/InGaAs (1.2 nm) strained well and two AlAs (1.7 nm) barriers sandwiching the well. The HEMT structure includes an undoped InGaAs channel layer. The gate length of the HEMT is 0.7 μm. Fig. 4 shows a proper quasi-static test pattern for a fabricated static binary frequency divider measured at room temperature. The present circuit consists of only ten devices. This is in stark contrast to the up to 30 devices found in a conventional SCFL
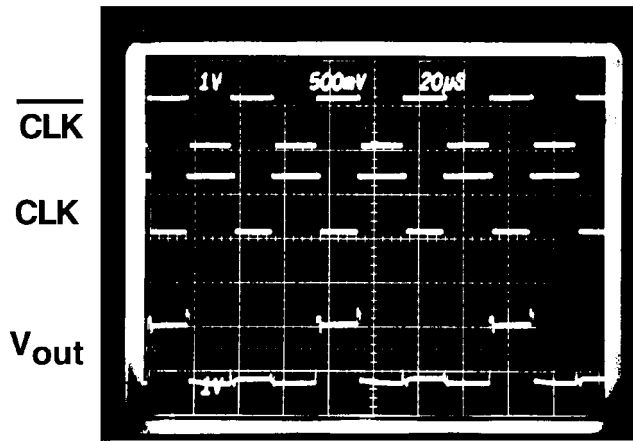
Fig. 4. A quasi-static test pattern demonstrating proper operation for a fabricated static binary frequency divider. Measurements were preformed at room temperature. Here, V_{out} is an inverse of E in Fig. 1(c), because the output buffer [Fig. 1(a)] inverts the signal.

circuit [1], [2]. This reduction could lead not only to higher-frequency operation but also to reduced power consumption.

A detailed estimation of the toggle frequency is beyond the scope of this letter. Here, as a preliminary, we briefly discuss a switching process at t_1 in Fig. 2(b). The A_0 behavior is described as a charging process of three capacitances, C_d, C_l, and C_f by currents through the two elements, where C_d, C_l, and C_f are the driver element capacitance between its emitter and collector electrodes, the load element capacitance, and the gate capacitance of the next stage HEMT, respectively. The charging time τ is approximately given by

$$\tau = (C_d + C_l + C_f)/(I_{\text{pd}}/V_{\text{pd}} + I_{\text{pl}}/V_{\text{pl}})$$

where I_{pd} and I_{pl} are the peak currents for the driver and load elements, respectively, and V_{pd} and V_{pl} are the peak voltages for these elements. The formula gives a value of around 1 ps, indicating the potentially high switching speed of this circuit. The high-speed operation -up to 18 Gb/s—of a flip-flop circuit including RTD's has recently been demonstrated [5]. In the present circuit, V_{dd} is about 1.9 V and static current per sub-circuit is about 5 mA. Thus the static power consumption for the two sub-circuits is about 20 mW. The inverter consumes 5 mW, so, the total static power consumption is about 25 mW. We expect the circuit to lead to reduced power at high frequencies.

IV. CONCLUSIONS

We have described a static binary frequency divider with a simplified circuit configuration achieved by utilizing the functionality of two series-connected resonant tunneling diodes in combination with HEMT's. The proposed circuit was fabricated using InP-based RTD/HEMT monolithic integration technology, and proper operation was confirmed experimentally at room temperature. The results indicate the circuit configuration utilizing RTD's in combination with HEMT's is a candidate for extending the frequency range of electron devices.

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