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Source/Drain Contact Resistance of Silicided Thin-Film SOI MOSFET's

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Abstract—**We developed a source/drain contact (S/D) resistance model for silicided thin-film SOI MOSFET's, and analyzed its dependence on device parameters considering the variation in the thickness of the silicide and residual SOI layers due to silicidation. The S/D resistance is insensitive to the silicide thickness over a wide range of thicknesses; however, it increases significantly when the silicide thickness is less than one hundredth of initial SOI thickness, and when almost all the SOI layer is silicided. To obtain a low S/D resistance, the specific contact resistance must be reduced, that is, the doping concentration at the silicide-SOI interface must be more than 10^{20} cm^{-3}.**

I. Introduction

THIN-film SOI MOSFET's are free from the scaling limits of bulk MOSFET's [1]–[5]. Furthermore, the gate tightly controls the potential in the channel region, leading to the high transconductance and large subthreshold slope, which are verified with theoretical and experimental analysis [6]–[12].

The above superb characteristics of SOI MOSFET's are enhanced when the SOI is thin, however this increases parasitic source/drain (S/D) resistance. Silicidation of the source and drain is required to compensate for the increased resistance.

The silicidation of the source/drain regions is also invoked with bulk MOSFET's because a shallow junction is required to suppress short channel effects as the gate length decreases. Berger *et al.* modeled the contact resistance in the source/drain contact regions as a transmission line [13], and Scott developed the transmission line model (TLM) for a silicided source/drain structure and analyzed the characteristics thoroughly [14].

Although Scott's model is also applicable to SOI MOSFET's (Fig. 1), the SOI device has its unique subjects: the consumed silicon layer is limited by the initial SOI thickness; a side contact source/drain structure (Fig. 2) is also possible, unlike bulk MOSFET's. Furthermore, Scott's TML model assumes that the resistance of side contact region R_{cf} (Fig. 1(b)) is infinite, and overestimates the S/D resistance in some cases as shown later.

We developed Scott's TML model so that it includes a finite side contact resistance and is applicable to the side contact structure, and then systematically analyzed the dependence of the parasitic S/D resistance on device parameters relevant to thin-film SOI MOSFET's.

In this paper, we call the structure I (Fig. 1) surface contact, and the structure II (Fig. 2) side contact.

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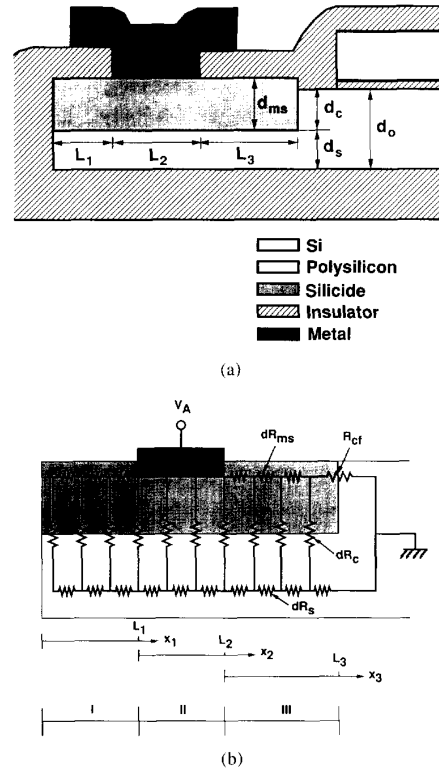
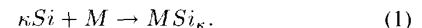


Fig. 1. Structure I (a) Structure of surface contact source/drain, and (b) its equivalent circuit.

II. Contact Resistance Model

We considered a source/drain silicidation process in which metal M is deposited on silicon, and then silicide MSi_κ is formed, which is expressed by a chemical reactive equation as



$$\kappa Si + M \rightarrow MSi_\kappa. \quad (1)$$

The silicide thickness, d_{ms}, and the consumed SOI thickness, d_c, are related as follows (Fig. 1(a)):

$$d_{ms} = \frac{n_{si}}{\kappa n_{ms}} d_c \quad (2)$$

where n_{Si} and n_{ms} are the density of silicon and silicide. The residual SOI thickness d_s is

$$d_s = d_0 - d_c. \quad (3)$$

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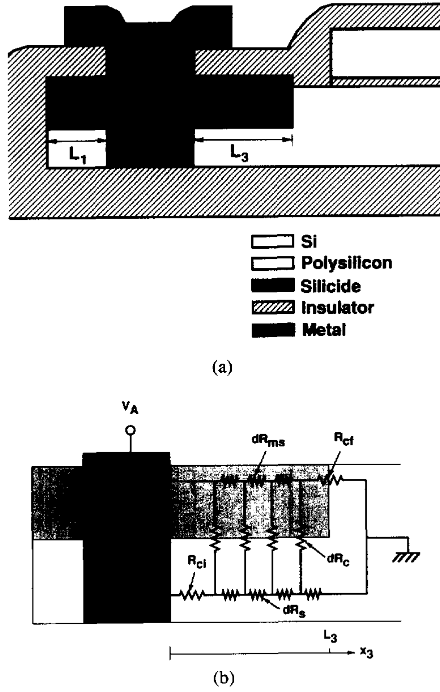

Fig. 2. Structure II (a) Structure of side contact source/drain, and (b) its equivalent circuit.

We defined the following resistances to clarify the derivation:

$$R_{ms} = \frac{\rho_{ms}}{W d_{ms}}; \quad R_s = \frac{\rho_s}{W d_s}; \quad R_c = \frac{\rho_c}{W};$$
$$R_{ci} = \frac{\rho_{ci}}{W d_s}; \quad R_{cf} = \frac{\rho_{cf}}{W d_c} \tag{4}$$

where W is the device width, ρ_{ms} and ρ_s are the resistivity of the silicide and SOI layers, and ρ_c, ρ_{ci}, and ρ_{cf} are the specific contact resistances of the regions shown in Figs. 1(b) and 2(b). We assume that the resisitivities are constant, which means that the doping concentration in the SOI region is uniform. Although this is a good approximation for thin-film SOI devices, it is obviously invalid for thick-film SOI devices and bulk MOSFET's. We focused on thin-film SOI MOSFET's, but will show later how to modify the treatment for nonuniform doping profiles.

We studied $TiSi_2$ which is the most commonly used material in modern VLSI technology, and shows the nominal value of the physical parameters in Table I [15]. For simplicity, we assumed that ρ_{ci} and ρ_{cf} equal to ρ_c. Although ρ_s and ρ_c are functions of the doping concentration, N_D, we used a ρ_s of $10^{-3}\,\Omega$ cm and a ρ_c of between 10^{-7} and $10^{-6}\,\Omega\,\mathrm{cm}^2$ which

TABLE I
NOMINAL PHYSICAL PARAMETERS

κ	2
n_{ms}	$2.34 \times 10^{22}\ \mathrm{cm}^{-3}$
n_s	$5.00 \times 10^{22}\ \mathrm{cm}^{-3}$
ρ_{ms}	$15\,\mu\Omega\mathrm{cm}$
ρ_s	$10^{-3}\,\Omega\mathrm{cm}$
ρ_c	10^{-7} to $10^{-6}\,\Omega\mathrm{cm}^2$

are typical values for practical high doping concentration regions.

In the equivalent circuit for the surface contact structure (Fig. 1(b)),

$$dR_{ms} = R_{ms}\Delta x; \quad dR_s = R_s\Delta x; \quad dR_c = \frac{R_c}{\Delta x}. \tag{5}$$

As stated by Berger and Scott [13], [14], the use of a transmission line model requires the following assumptions:

1) the current through the interface between the two layers is vertical,
2) the thicknesses of the silicide and residual SOI layers are both enough infinetesimally small so that we can assume parallel one-dimensional current flow in each layer, and
3) the contact is ohmic.

We derived differential equations and the boundary conditions similar to those in [14], but with different boundary conditions at $x_3 = L_3$ and different notations (Appendix). We obtained (see bottom of page) where

$$\alpha^2 = \frac{R_{ms} + R_s}{R_c}; \quad \beta^2 = \frac{R_s}{R_c}, \tag{7}$$
$$\gamma_{ms} = \frac{R_{ms}}{R_{ms} + R_s}; \quad \gamma_s = \frac{R_s}{R_{ms} + R_s} \tag{8}$$

and

$$R_0 = \frac{L_3}{\dfrac{1}{R_{ms}} + \dfrac{1}{R_s}}; \quad R_1 = \frac{R_{ms} + R_s}{\alpha \tanh(\alpha L_1)};$$
$$R_2 = \frac{R_s}{\beta} \frac{\beta \dfrac{R_1}{R_s}\cosh(\beta L_2) + \sinh(\beta L_2)}{\beta \dfrac{R_1}{R_s}\sinh(\beta L_2) + \cosh(\beta L_2)}. \tag{9}$$

When R_{cf} is infinite, (6) reduces to (see bottom of the following page) which is Scott's TLM model [14] as expected. Furthermore, when R_{ms} is zero, (10) reduces to

$$R_T = \frac{R_s}{\beta \tanh[\beta(L_1 + L_2 + L_3)]} \tag{11}$$

which is the Berger's TML model [13] with a contact length of $L_1 + L_2 + L_3$ instead of L_2.

$$R_T = R_0 \cdot \left\{ 1 + \frac{2\alpha\gamma_{ms}\gamma_s + \alpha(\gamma_{ms}^2 + \gamma_s^2)\cosh(\alpha L_3) + \left(\gamma_{ms}\dfrac{R_m}{R_{cf}} + \gamma_s\dfrac{R_s}{R_2}\right)\sinh(\alpha L_3)}{L_3\left[\left(\alpha^2\gamma_{ms}\gamma_s + \dfrac{R_{ms}R_s}{R_{cf}R_2}\right)\sinh(\alpha L_3) + \alpha\left(\gamma_{ms}\dfrac{R_s}{R_2} + \gamma_s\dfrac{R_{ms}}{R_{cf}}\right)\cosh(\alpha L_3)\right]} \right\} \tag{6}$$

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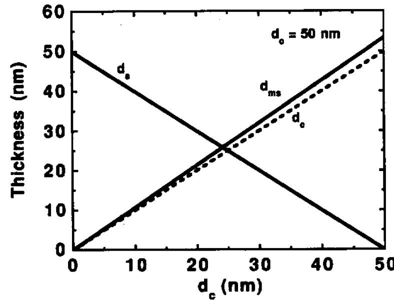

Fig. 3. Relationship between silicide, consumed SOI, and residual SOI thicknesses.

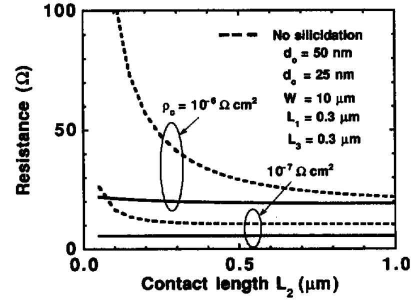

Fig. 4. Dependence of S/D resistance on L_2.

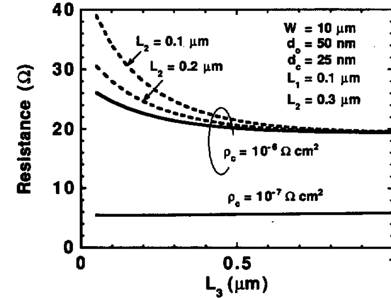

Fig. 5. Dependence of S/D resistance on L_3.

As the SOI thickness decreases, the process for opening the contact hole may unintentionally etch away the SOI layer, and form the side contact structure (Fig. 2). SOI devices, however, unlike bulk SOI MOSFET's, readily operate with the side contact structure since there are no junction under the S/D regions. We therefore evaluated the S/D resistance of the side contact device structure (Fig. 2).

The equivalent circuit model relevant to the side contact structure as shown in Fig. 2(b) leads to (see bottom of page). When R_{ci} and R_{cf} are infinite and R_{ms} is zero, (12) also reduces to Berger's TML model with the contact length of L_3 as

$$R_T = \frac{R_s}{\beta \tanh(\beta L_3)}. \tag{13}$$

III. Results and Discussion

For $TiSi_2$ d_{ms} is almost the same as d_c (Fig. 3), that is, the volume expansion during the silicidation is quite small.

When the source/drain regions are silicided, the S/D resistance is insensitive to L_2 (Fig. 4) because the effective contact length is $L_1+L_2+L_3$ instead of L_2. L_2 should, therefore, be as short as possible in bulk MOSFET's to reduce the source/drain capacitance. However, since increasing L_2 does not increase the capacitance of SOI MOSFET's, L_2 should be chosen to improve the process reliability.

When source/drain regions are not silicided, the S/D resistance depends on L_2 (Fig. 4). The critical length, L_{2c}, at which the S/D resistance begins to increase is given by $1/\beta$ [13]. L_{2c} indicates how the current spreads to reduce the resistance and is the point at which the resistance is $(e^2+1)/(e^2-1)$, that is, 1.3 times the resistance with infinite L_2. L_{2c} is 0.71 μm for $\rho_c = 10^{-6}\,\Omega\text{cm}^2$, and 0.22 μm for $\rho_c = 10^{-7}\,\Omega\text{cm}^2$.

When the source/drain regions are silicided, the S/D resistance does not depend on L_3 for $\rho_c = 10^{-7}\,\Omega\text{cm}^2$, but it does on L_3 for $\rho_c = 10^{-6}\Omega\text{cm}^2$ (Fig. 5). The structure approximately can be regarded as the contact length of $L = L_1 + L_2 + L_3$, and the critical length, L_c, at which the S/D resistance begins to increase is given by $1/\alpha$. L_c is 0.5 μm for $\rho_c = 10^{-6}\,\Omega\text{cm}^2$, and 0.16 μm for $\rho_c = 10^{-7}\,\Omega\text{cm}^2$. Since $L_1 + L_2$ is larger than L_c for $\rho_c = 10^{-7}\,\Omega\text{cm}^2$, the S/D resistance is insensitive to L_3. The S/D resistance increases when $L_1 + L_2 + L_3$ is smaller than L_c for $\rho_c = 10^{-6}\,\Omega\text{cm}^2$. Consequently, the structure should be designed with $L_2 > 1/\beta$ for devices without silicidation, and $L_1 + L_2 + L_3 > 1/\alpha$ for devices with silicidation.

The S/D resistance decreases rapidly when the silicide thickness increases from zero to a certain thickness, and then rather insensitive to the silicide thickness over a wide range

$$R_T = R_0 \left\{ 1 + \frac{2\alpha\gamma_{ms}\gamma_s + \alpha(\gamma_{ms}^2 + \gamma_s^2)\cosh(\alpha L_3) + \gamma_s \frac{R_s}{R_2}\sinh(\alpha L_3)}{L_3\left[\alpha^2\gamma_{ms}\gamma_s \sinh(\alpha L_3) + \alpha\gamma_{ms}\frac{R_s}{R_2}\cosh(\alpha L_3)\right]} \right\}, \tag{10}$$

$$R_T = R_0 \left\{ 1 + \frac{2\alpha\gamma_{ms}\gamma_s + \alpha(\gamma_{ms}^2 + \gamma_s^2)\cosh(\alpha L_3) + \left(\gamma_{ms}\frac{R_{ms}}{R_{cf}} + \gamma_s\frac{R_s}{R_{ci}}\right)\sinh(\alpha L_3)}{L_3\left[\left(\alpha^2\gamma_{ms}\gamma_s + \frac{R_{ms}R_s}{R_{cf}R_{ci}}\right)\sinh(\alpha L_3) + \alpha\left(\gamma_{ms}\frac{R_s}{R_{ci}} + \gamma_s\frac{R_{ms}}{R_{cf}}\right)\cosh(\alpha L_3)\right]} \right\}. \tag{12}$$

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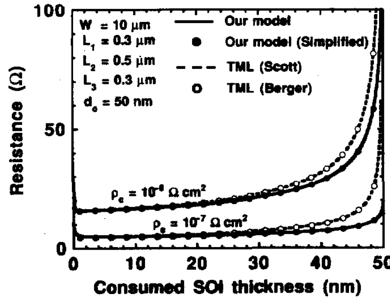

Fig. 6. Dependence of S/D resistance on consumed SOI thickness.

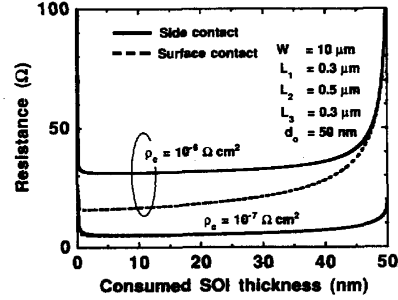

Fig. 8. Dependence of S/D resistance on device structure.

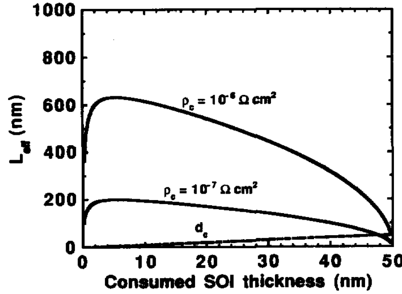

Fig. 7. Dependence of effective contact length on consumed SOI thickness.

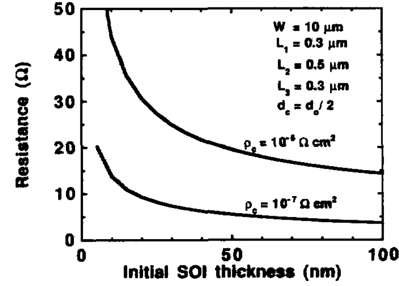

Fig. 9. Dependence of S/D resistance on initial SOI thickness.

thicknesses, and increases rapidly when almost all the SOI layer is silicided (Fig. 6).

When the silicide thickness increases, the sheet resistance of residual SOI layer increases, current flows long in the silicide to reduce the total resistance, and the effective contact length, L_{eff}, which is given by $1/\alpha$ [13], decreases (Fig. 7). L_{eff} becomes comparable to d_c when almost all the SOI layer is silicided, and then the total resistance increases significantly.

When the silicide layer is quite thin, the sheet resistance of the silicide layer cannot be negligible compared with that of residual SOI layer. The critical silicide thickness at which both sheet resistances become comparable is given by

$$d_{cc} = \frac{\rho_{ms}}{\rho_s} d_s. \tag{14}$$

Since ρ_{ms} is smaller than ρ_s by about two orders of magnitude, the critical thickness is about one hundredth of the initial SOI thickness. This is why the S/D resistance decreases significantly with a thin silicide layer.

Berger's and Scott's TML models give almost the same S/D resistance (Fig. 6), which means that the sheet resistance of the silicide layer does not contribute to the total S/D resistance. Both TML models overestimate the S/D resistance when the silicide thickness is comparable to the initial SOI thickness where the current flow through the side contact region (R_{cf}) must be considered. Consequently, when the silicide is thin compared to the initial SOI thickness, Berger's simple TML model is sufficiently accurate, but when most of the SOI layer is silicided, our model must be used.

From the above results, assuming that $R_{ms} = 0$, (6) is further simplified as

$$R_T = \frac{1}{\dfrac{\beta \tanh\left[\beta(L_1 + L_2 + L_3)\right]}{R_s} + \dfrac{1}{R_{cf}}} \tag{15}$$

which does not lose accuracy (Fig. 6).

The S/D resistance of side contact structure is almost the same as that of surface contact structure for $\rho_c = 10^{-7}\,\Omega\text{cm}^2$ (Fig. 8) because L_{eff} is smaller than L_3 (Fig. 7). L_{eff} is, however, larger than L_3 for $\rho_c = 10^{-6}\,\Omega\text{cm}^2$, and hence the S/D resistance of side contact structure is larger than that of surface contact structure. When consumed SOI thickness increases, L_{eff} decreases, and then the S/D resistance of side contact structure is almost the same as that of surface contact structure even for $\rho_c = 10^{-6}\,\Omega\text{cm}^2$.

The S/D resistance increases with decreasing initial SOI thickness (Fig. 9) because large R_s decreases L_{eff}. Therefore, increasing L_1, L_2, or L_3, does not suppress the S/D resistance increase. To reduce the resistance of such thin SOI devices, a stacked structure must be developed.

So far, we have treated ρ_c and ρ_s independently. However, both are functions of the doping concentration and are, therefore, related. Although the relationship depends on the process and hence is not well established, we used the values reported in [16] and [17] (Fig. 10). The dependence of the S/D resistance on the doping concentration is similar to that of ρ_c, that is, the contact resistance dominates the S/D resistance (Fig. 11). Since the S/D resistance increases significantly with decreasing N_D, N_D should be as high as possible which may be upper limited by the solid solubility.

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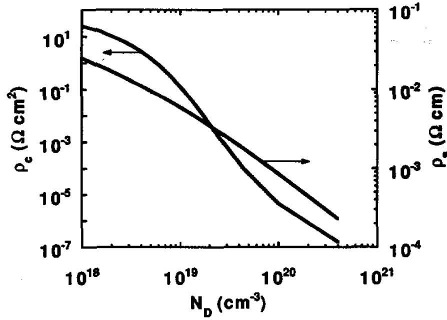

Fig. 10. Dependence of ρ_c and ρ_s on doping concentration.

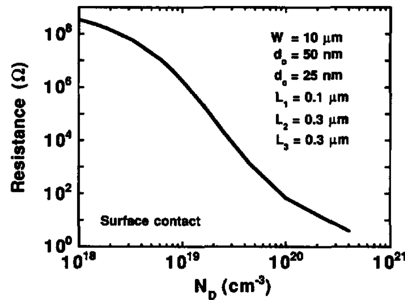

Fig. 11. Dependence of S/D resistance on doping concentration.

We also assumed a uniform doping concentration in the SOI layer. We can extend our model to nonuniform concentrations by replacing (4) with

$$R_{ms} = \frac{\rho_{ms}}{W d_{ms}}; \quad R_s = \left[W \int_0^{d_s} \frac{dx}{\rho_s(x)}\right]^{-1};$$
$$R_c = \frac{\rho_c}{W}; \quad R_{ci} = \left[W \int_0^{d_s} \frac{dx}{\rho_c(x)}\right]^{-1};$$
$$R_{cf} = \left[W \int_0^{d_c} \frac{dx}{\rho_c(x)}\right]^{-1}. \tag{16}$$

IV. Conclusion

We developed a source/drain contact (S/D) resistance model for silicided thin-film SOI MOSFET's, and analyzed its dependence on the device parameters relevant to thin-film SOI MOSFET's. Our model includes the existing TML models as special cases. The existing TML models overestimate the S/D resistance when the consumed SOI thickness approaches the initial SOI thickness. We also simplified our model without losing accuracy.

The S/D resistance is insensitive to the silicide layer length when the length exceeds $1/\alpha$, and is also insensitive to the silicide thickness except when the SOI layer is fully silicided and the resistance increases significantly. The S/D resistance also increases significantly when the silicide thickness is less than one hundreth of the initial SOI thickness. To obtain a low S/D resistance the specific contact resistance must be reduced, that is, the doping concentration at the silicide-SOI interface must be high.

V. Appendix

We solved the differential equations and boundary conditions for our model using conventional methods. We assumed that a voltage V_A is applied to the electrode, and the potential for $x_3 = L_3$ is zero (Figs. 1 and 2).

A. Differential Equations

For regions I and III in Fig. 1, the differential equations for the voltage in the silicide region V_{ms} and SOI region V_s, and the current in silicide region I_{ms} and SOI region I_s are

$$\frac{d^2 V_{msj}}{dx_j^2} = \frac{R_{ms}}{R_c}(V_{msj} - V_{sj}) \tag{A-1}$$
$$\frac{d^2 V_{sj}}{dx_j^2} = -\frac{R_s}{R_c}(V_{msj} - V_{sj}) \tag{A-2}$$
$$I_{msj} = -\frac{1}{R_{ms}} \frac{dV_{msj}}{dx_j} \tag{A-3}$$
$$I_{sj} = -\frac{1}{R_s} \frac{dV_{sj}}{dx_j} \tag{A-4}$$

where subscript j denotes the region number. These differential equations are also valid for the side contact structure.

The differential equations in region II are

$$V_{ms2} = V_A \tag{A-5}$$
$$\frac{d^2 V_{s2}}{dx_2^2} = -\frac{R_s}{R_c}(V_A - V_{s2}) \tag{A-6}$$
$$I_{s2} = -\frac{1}{R_s} \frac{dV_{s2}}{dx_2}. \tag{A-7}$$

B. Boundary Conditions

1) Surface contact structure Region I

$$I_{ms1}(x_1) = -I_{s1}(x_1) \tag{A-8}$$
$$I_{ms1}(0) = I_{s1}(0) = 0 \tag{A-9}$$
$$R_1 \equiv \frac{V_{ms1}(L_1) - V_{s1}(L_1)}{I_{s1}(L_1)}. \tag{A-10}$$

Region II

$$R_1 = \frac{V_A - V_{s2}(0)}{I_{s2}(0)} \tag{A-11}$$
$$R_2 \equiv \frac{V_A - V_{s2}(L_2)}{I_{s2}(L_2)}. \tag{A-12}$$

Region III

$$V_{ms3}(0) = V_A \tag{A-13}$$
$$R_2 = \frac{V_A - V_{s3}(0)}{I_{s3}(0)} \tag{A-14}$$
$$V_{s3}(L_3) = 0 \tag{A-15}$$
$$I_{ms3}(L_3) = \frac{1}{R_{cf}} V_{ms3}(L_3). \tag{A-16}$$

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2) Side contact structure Region III

$$V_{ms3}(0) = V_A \quad \text{(A-17)}$$

$$R_{ci} = \frac{V_A - V_{s3}(0)}{I_{s3}(0)} \quad \text{(A-18)}$$

$$V_{s3}(L_3) = 0 \quad \text{(A-19)}$$

$$I_{ms3}(L_3) = \frac{1}{R_{cf}} V_{ms3}(L_3). \quad \text{(A-20)}$$

In both device structures, the S/D resistance is

$$R_T = \frac{V_A}{I_{ms}(L_3) + I_s(L_3)}. \quad \text{(A-21)}$$

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