Scaling theory for double-gate SOI MOSFET's

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Scaling Theory for Double-Gate SOI MOSFET's

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***Abstract*—We established a scaling theory for double-gate SOI MOSFET's, which gives a guidance for the device design (silicon thickness t_{si}; gate oxide thickness t_{ox}) so that maintaining a subthreshold factor for a given gate length L_G. According to our theory, a device can be designed with a gate length of less than 0.1 μm while maintaining the ideal subthreshold factor, which is verified numerically with a two-dimensional device simulator.**

I. Introduction

According to the Brew's scaling theory [1], the channel doping concentration in bulk MOSFET's should be increased to alleviate the short-channel effects, leading to more than 10^{18} cm^{-3} for a gate length of less than 0.1 μm [2]. This high-doping concentration degrades device performance due to decreased mobility and increased junction capacitance.

A double-gate SOI MOSFET, in which the potential is controlled by front and back gates as shown in Fig. 1, is proposed to circumvent the scaling limitations of bulk MOSFET's. The characteristics of this device have been studied [2]–[11], revealing its ideal subthreshold factor, high transconductance, and short-channel effect immunity.

Since the potential distribution in double-gate SOI MOSFET's differs greatly from that in bulk and single-gate SOI MOSFET's because of symmetrical device structure with quite low channel doping concentration [4], [7], the scaling theory developed for bulk MOSFET's cannot be applied to double-gate SOI MOSFET's.

Yan *et al.* proposed a unique scaling theory for double-gate SOI MOSFET's [2]. According to their theory, the device should be designed maintaining

$$\alpha_1 = \frac{L_G}{2\lambda_1} \tag{1}$$

where λ_1 is the so-called natural length which characterizes the short-channel effect and is given by

$$\lambda_1 = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}} t_{si} t_{ox}} \tag{2}$$

where ϵ_{si} is the dielectric constant of silicon, ϵ_{ox} is the dielectric constant of silicon dioxide, t_{si} is the SOI silicon thickness, and t_{ox} is the gate oxide thickness. This natural length is an easy guide for choosing device parameters, and has simple physical meaning that a small natural length corresponds to superb short channel effect immunity. Although the authors showed that a small α gives a degraded S-factor, they did not show whether the same α with various device parameters gives the same S-factor.

Fig. 2(a) shows the dependence of S-factor on α_1 calculated using a two-dimensional device simulator [12]. Although a smaller α_1 gives a larger S-factor, the same α_1 with various combinations of device parameters does not give the same S-factor, that is, the theory does not provide the same guideline for different gate lengths.

The onset point where the S-factor degrades does not depend on the drain voltage, V_D, although the value of the S-factor after degradation strongly depends on V_D. Since the purpose of our analysis is to clarify the onset point, we restricted our analysis to $V_D = 0.05$ V unless specified.

Yan *et al.* [2] assumed that the punchthrough current flows along the surface, which is invalid for a double-gate SOI MOSFET for the following reasons.

The maximum potential at the SOI center, ϕ_c, is more sensitive to gate length than that at the surface, ϕ_s, and, furthermore, the absolute value of ϕ_c is smaller than that of ϕ_s (Fig. 3), meaning that the punchthrough current dominantly flows at the SOI center.

In this paper, we derive a scaling theory relevant to ϕ_c, and show that our scaling theory acts as a guide to design devices that hold proper S-factors.

II. Theory

The Poisson equation of potential, ϕ, is [13]

$$\frac{d^2\phi(x, y)}{dx^2} + \frac{d^2\phi(x, y)}{dy^2} = \frac{qN_A}{\epsilon_{si}} \tag{3}$$

where N_A is the channel doping concentration, and the y-axis is perpendicular and the x-axis is parallel to the channel (Fig. 1).

Using the same parabolic potential profile in the vertical direction as Young used [13] and applying the boundary condition of $d\phi/dy = 0$ for $y = t_{si}/2$, we obtained the same $\phi(x, y)$ as that in [2] given by

$$\phi(x, y) = \phi_s(x) + \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_s(x) - (V_G - V_{FB})}{t_{ox}} y - \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\phi_s(x) - (V_G - V_{FB})}{t_{ox} t_{si}} y^2 \tag{4}$$

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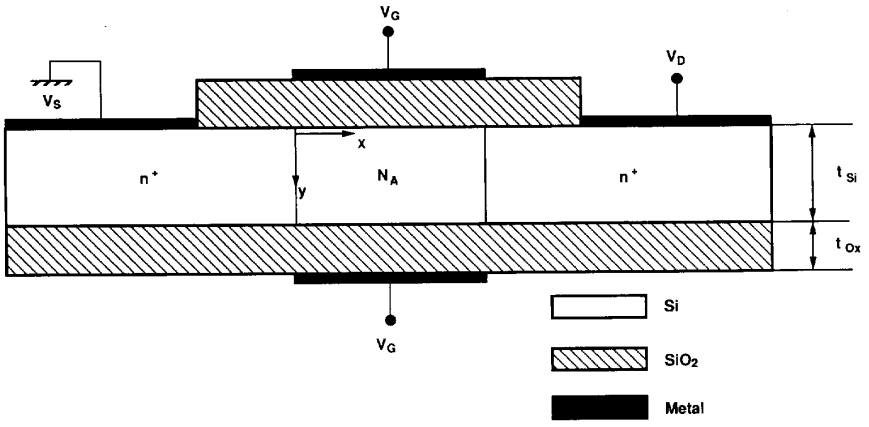
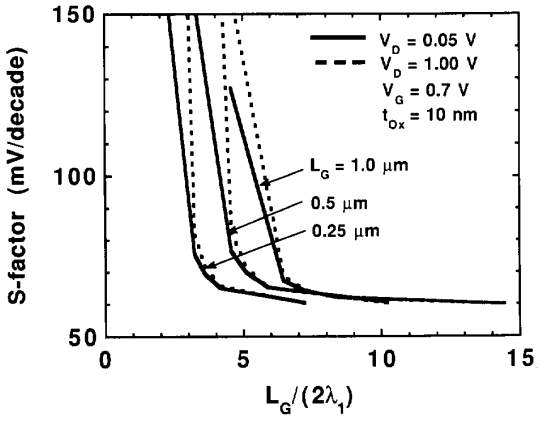


Fig. 1. Double-gate MOSFET.



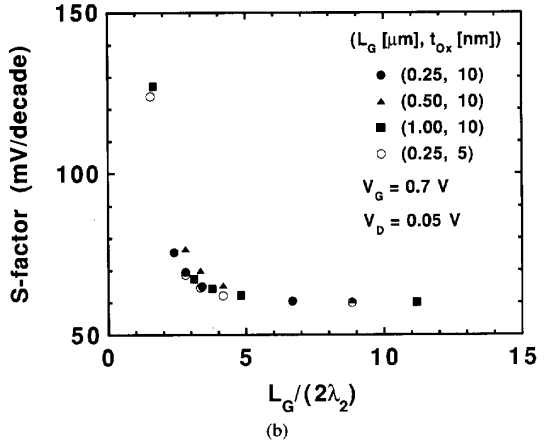


Fig. 2. Dependence of subthreshold factor on the scaling parameter: (a) former model; (b) proposed model.

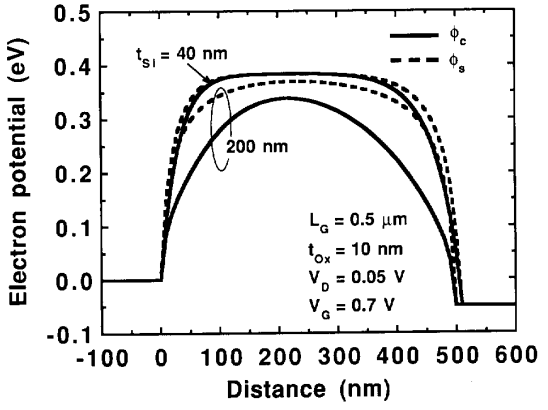


Fig. 3. Potential distribution along channel at the surface, ϕ_s, and at the center of SOI, ϕ_c.

where V_G is the gate voltage and V_{FB} is the flatband voltage.

Since ϕ_c should be relevant to the punchthrough current, we obtained the relation between ϕ_s and ϕ_c from (4) by substituting $y = t_{si}/2$ as

$$\phi_s(x) = \frac{1}{1 + \frac{\epsilon_{ox}}{4\epsilon_{si}}\frac{t_{si}}{t_{ox}}}\left[\phi_c(x) + \frac{\epsilon_{ox}}{4\epsilon_{si}}\frac{t_{si}}{t_{ox}}(V_G - V_{FB})\right], \quad (5)$$

and then expressed $\phi(x, y)$ using ϕ_c as

$$\phi(x, y) = \left[1 + \frac{\epsilon_{ox}}{\epsilon_{si}}\frac{y}{t_{ox}} - \frac{\epsilon_{ox}}{\epsilon_{si}}\frac{y^2}{t_{ox}t_{si}}\right] \cdot \frac{\phi_c(x) + \frac{\epsilon_{ox}}{4\epsilon_{si}}\frac{t_{si}}{t_{ox}}(V_G - V_{FB})}{1 + \frac{\epsilon_{ox}}{4\epsilon_{si}}\frac{t_{si}}{t_{ox}}} - \frac{\epsilon_{ox}}{\epsilon_{si}}\frac{y}{t_{ox}}(V_G - V_{FB}) + \frac{\epsilon_{ox}}{\epsilon_{si}}\frac{y^2}{t_{ox}t_{si}}(V_G - V_{FB}). \quad (6)$$

Substituting (6) into (3), we obtain

$$\frac{d^2\phi_c(x)}{dx^2} + \frac{V_G - V_{FB} - \phi_c(x)}{\lambda_2^2} = \frac{qN_A}{\epsilon_{si}} \quad (7)$$

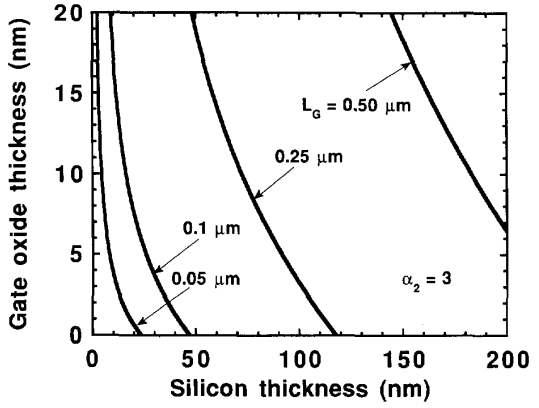


Fig. 4. Relationship between silicon thickness and gate oxide thickness with various gate lengths alleviating short channel effect.

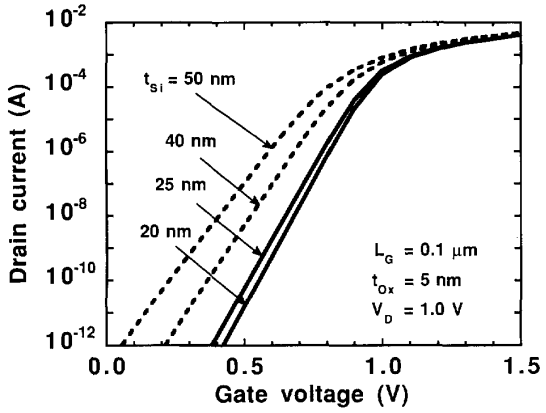


Fig. 5. Subthreshold characteristics with various silicon thickness. Solid lines correspond to the devices adhering to the scaling rule and dashed lines to those not doing so.

where λ_2 is the natural length having the same physical meaning as λ_1 and is

$$\lambda_2 = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}}\left(1 + \frac{\epsilon_{ox}}{4\epsilon_{si}}\frac{t_{si}}{t_{ox}}\right) t_{si}t_{ox}}. \tag{8}$$

Note that λ_2 is always larger than λ_1, that is, the double-gate SOI MOSFET suffers from the short-channel effect more than predicted by Yan's model [2].

Exactly the same analysis as in [2] is then followed. The key conclusion from this analysis is that the same α_2 leads to the same S-factor, where

$$\alpha_2 = \frac{L_G}{2\lambda_2}. \tag{9}$$

III. Results and Discussion

Throughout this analysis, we fixed N_A to 10^{15} cm^{-3} and V_{FB} to 0.29 V which corresponds to p^+ polysilicon gate. The threshold voltage is about 1.0 V independent of device parameters and the S-factor is also independent of V_G in the subthreshold region when it has almost ideal value [14]. We evaluated S-factor for $V_G = 0.7$ V.

Fig. 2(b) shows the dependence of the S-factor on α_2 calculated using a two-dimensional device simulator [12]. The same α_2 leads to the same value of S-factor with various combinations of device parameters, t_{ox}, t_{si}, and L_G. We found that an α_2 of less than 3 is needed to alleviate the punchthrough, that is, short-channel effect.

Once α_2 is determined from Fig. 2 (b), the relationship between t_{ox} and t_{si} is expressed from (9) as

$$t_{ox} = \frac{\epsilon_{ox}L_G^2}{2\alpha_2^2\epsilon_{si}t_{si}} - \frac{\epsilon_{ox}}{4\epsilon_{si}}t_{si}. \tag{10}$$

t_{ox} and t_{si} at a given L_G should be designed in the lower region of the corresponding L_G curve in Fig. 4. As L_G decreases, the allowable region decreases. When $L_G = 0.1$ μm with $t_{ox} = 5$ nm, t_{si} should be less than 25 nm, and when $L_G = 0.05$ μm with $t_{ox} = 3$ nm, t_{si} should be less than 10 nm.

Fig. 5 shows the subthreshold characteristics of the devices for $L_G = 0.1$ μm, where solid lines correspond to $\alpha_2 > 3$ and dashed lines to $\alpha_2 < 3$ and $V_D = 1.0$ V which may be the supply voltage for $L_G = 0.1$ μm. We can expect almost an ideal S-factor with the device if we design the devices so that α_2 is more than 3. We also verified the same numerical results with the device for $L_G = 0.05$ μm.

IV. Summary

We derived a natural length relevant to the scaling theory for double-gate SOI MOSFET's, and described how to design t_{ox} and t_{si} for a given gate length maintaining a proper S-factor. According to the theory, almost the ideal S-factor value can be expected even with L_G of less than 0.1 μm. The key factor that determines the shortest gate length device we can design is the thinnest t_{si} we can produce. A t_{si} of less than 10 nm is needed at $L_G = 0.05$ μm with $t_{ox} = 3$ nm.

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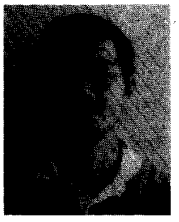

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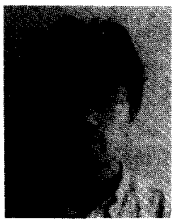

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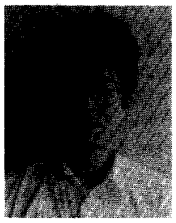

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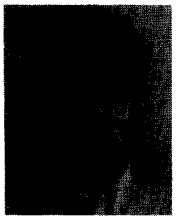

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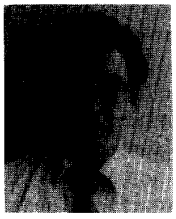

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