東北大学機関リポジトリ
TOUR
Tohoku University Repository

U-grooved SIT CMOS technology with 3 fJ and 49 ps (7 mW, 350 fJ) operation

著者	田中　徹
journal or publication title	IEEE Transactions on Electron Devices
volume	37
number	8
page range	1877-1883
year	1990
URL	http://hdl.handle.net/10097/47471

doi: 10.1109/16.57139

U-Grooved SIT CMOS Technology with 3 fJ and 49 ps (7 mW, 350 fJ) Operation

JUN-ICHI NISHIZAWA, FELLOW, IEEE, NOBUO TAKEDA, SOHBE SUZUKI, MEMBER, IEEE, TOSHIFUMI SUZUKI, AND TETSU TANAKA

Abstract—**In this paper Static Induction Transistor CMOS is analyzed by a circuit simulation method. According to the results, the propagation delay time of the SIT CMOS could be represented as the ratio of the load capacitance over the transconductance. The U-grooved structure plays an important role in the fabrication of MOS SIT with large transconductance and small parasitic capacitance. U-grooved SIT CMOS has been fabricated by anisotropic plasma etching, and its switching speed has been evaluated by a 31-stage ring oscillator. A minimum p–τ product of 3 fJ/gate has been obtained for a design rule of 1-μm channel length. A minimum propagation delay time of 49 ps/gate has also been obtained at a dissipation power of 7 mW/gate, which corresponds to a p–τ product of 350 fJ/gate.**

I. INTRODUCTION

THE static induction transistor (SIT), which has nonsaturating current versus voltage characteristics just like a vacuum triode tube, was invented by Nishizawa and Watanabe in 1950 [1]. The operating mechanism of the SIT is based upon the barrier height control of injecting carriers from the source to the channel by the electrostatic induction effect [2], [3]. The drain current of the SIT changes exponentially under the gate and drain voltages, in contrast to the "Analog Transistor" which was expected by Shockley in 1952 to follow the space-charge conduction law [4].

At first, the SIT was used in audio amplifiers, and the development of the SIT has led to other applications in electric power supplies, microwave communication [5], [6], and thyristors [7]–[9].

When integrated circuits are designed with SIT as an active device, they are able to operate with extremely high speed and low power. A type of SITL which is equivalent to integrated injection logic (I^2L) was realized in 1975 [10]. At present, the minimum p–τ product has been lowered to 0.2 fJ/gate [11], and a propagation delay time less than 1 ns has been achieved by a molybdenum Schottky gate SITL designed with 3 μm rule [12]. An SITL equivalent of current mode logic (CML) can be built as well [13].

Manuscript received January 5, 1989; revised February 20, 1990. The review of this paper was arranged by Associate Editor A. F. Tasch, Jr.

J. Nishizawa and T. Tanaka are with Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Sendai 980, Japan.

N. Takeda and S. Suzuki are with the Small Power Communication Systems Research Laboratories, Kawauchi, Sendai 980, Japan, on leave from the Semiconductor Research Institute, Kawauchi, Sendai 980, Japan.

T. Suzuki was with the Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Sendai 908, Japan. He is now with the Functional Device Research Laboratory, Nishizawa Terahertz Project, Research Development Corporation of Japan, c/o Semiconductor Research Institute, Kawauchi, Sendai 980, Japan.

IEEE Log Number 9036401.

In junction gate SITL's, the excess minority carrier injection limits the switching speed. In the metal–oxide–semiconductor (MOS) gate structure or the Schottky gate structure, there are no storage effects of minority carriers. Therefore, extremely high-speed operation is possible.

The MOS SIT has exponential I–V characteristics in contrast to the punch-through MOSFET of Richman which operates under the space-charge conduction law [14]. According to recent data from MOS SIT IC, a minimum propagation delay time of 75 ps/gate and a minimum p–τ product of 2 fJ/gate have already been achieved [15]. Moreover, a minimum p–τ product of 0.3 fJ/gate and a minimum dissipation power of 1.7 pW/gate have been obtained in planar SIT CMOS IC's [16]. To improve the switching speed of the SIT CMOS, the U-grooved structure is one of the appropriate structures [17].

In this paper, we present a circuit simulation method to analyze the operation of the SIT CMOS and then explain the preparation of the U-grooved SIT CMOS device.

II. CIRCUIT SIMULATION

In order to design the SIT CMOS IC for high-speed and low-power operation, it must be made clear as to what device parameters influence the propagation delay time of the device.

One of the useful methods for this purpose is circuit simulation by discrete devices and elements such as MOS SIT's, resistors, and capacitors. Of course, computer simulation is a popular method for analyzing circuits and devices, but accurate treatment for large signal operation is not so simple. Also, the results are dependent upon the accuracy of modeling. Therefore it is useful to allow the simulated circuits to be operated with large signals, even though the circuits have time constants greater than the fabricated devices. In these circuits, equivalent device parameters can easily be changed by resistors and capacitors externally connected to evaluate the dominant device parameter. Accordingly, we can design the integrated circuits by taking advantage of the results from circuit simulation in Section II-B.

A. Circuit Diagram

A basic SIT CMOS circuit composed of an n-channel MOS SIT and a p-channel MOS SIT is shown in Fig. 1(a). To vary device parameters, source resistors R_{nS}, R_{pS}; gate resistors R_{nG}, R_{pG}; and a load capacitor C_L can be connected externally as shown in Fig. 1(b).

0018-9383/90/0800-1877$01.00 © 1990 IEEE

Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on March 08,2010 at 00:46:18 EST from IEEE Xplore. Restrictions apply.

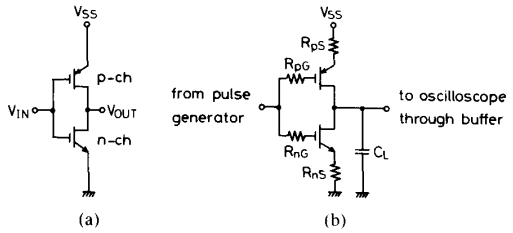


Fig. 1. Circuit diagram for simulation using discrete devices and elements.

These devices and elements are assembled on a teflon-glass substrate using microstrip lines to transmit electrical pulses. An input signal is supplied from a pulse generator through an impedance matching circuit and an output signal is observed by an oscilloscope through a source-follower buffer. The propagation delay time, the rise time, and the fall time are measured under various conditions.

B. Measurements

The relation between the propagation delay time and the external load capacitance C_L is given in Fig. 2. The propagation delay time increases with the external load capacitance. Thus the load capacitance, which is an input capacitance of the next stage in the integrated circuit, must be reduced for the fast operation. The extended value C_{L0} where the propagation delay time becomes zero means that the load capacitance C_L corresponds to the input capacitance of the source-follower buffer.

The propagation delay time related to the external source resistance is shown in Fig. 3. The propagation delay time that the n-channel transistor changes to its on-state is designated here as "n-on time." Similarly, the propagation delay time that the p-channel transistor changes to its on-state is designated as "p-on time." When the external source resistance R_{nS} is connected to the n-channel transistor, the n-on time increases as the resistance becomes larger (Fig. 3(a)). However, the p-on time remains unchanged. With the external source resistance R_{pS} connected to the p-channel transistor, the p-on time increases while the n-on time is constant (Fig. 3(b)).

A comparison between the above two figures shows that the transistor which changes from the off-state to the on-state dominates the propagation delay time of the CMOS circuit. The increase in the external source resistance decreases the effective transconductance of the transistor. The effective transconductance G'_m is expressed by

$$G'_m = \frac{G_m}{1 + G_m R_{nS}(\text{or } R_{pS})}$$

where G_m is the intrinsic transconductance of the transistor. When the value of R_{nS} (or R_{pS}) is much smaller than the value of $1/G_m$, G'_m is nearly equal to G_m. On the other hand, when the value of R_{nS} (or R_{pS}) becomes larger, G'_m approaches $1/R_{nS}$ (or R_{pS}). As the source resistance of the SIT is further reduced to a value lower than that of the regular FET, the former can be regarded as the operating condition of the SIT and the latter as that of the FET, as shown in Fig. 3.

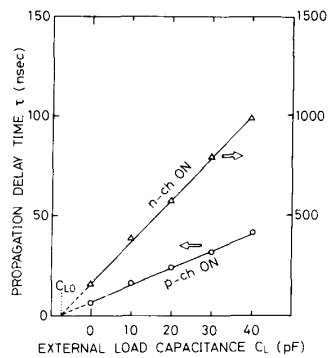


Fig. 2. Circuit simulation of propagation delay time versus external load capacitance.

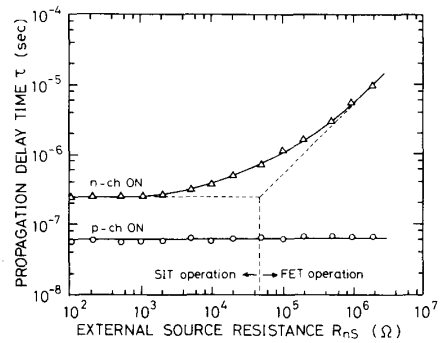


Fig. 3. Circuit simulation of propagation delay time versus external source resistance.

Fig. 4 shows the relation between the propagation delay time and $1/G_m$, where G_m is estimated from the I–V characteristics of the transistor. The dotted line which indicates the total load capacitance C_{L0} divided by the transconductance G_m shows good agreement with the measured values. Thus it becomes clear that the improvement of the transconductance is important for high-speed operation.

Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on March 08,2010 at 00:46:18 EST from IEEE Xplore. Restrictions apply.

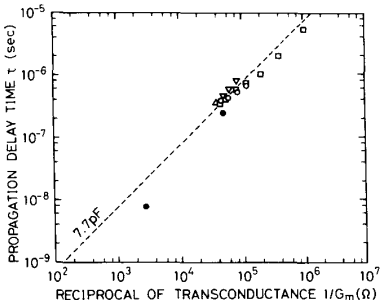


Fig. 4. Propagation delay time versus reciprocal of measured transconductance.

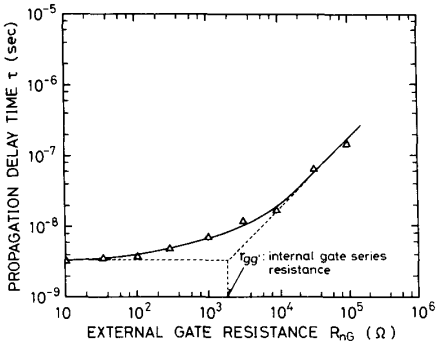


Fig. 5. Circuit simulation of propagation delay time versus external gate resistance.

Fig. 5 shows the relation of the propagation delay time versus the external gate resistance. As the gate resistance increases, the propagation delay time increases. The extended value r'_{gg}, where the two dotted lines are crossing, corresponds to the internal gate series resistance. Parasitic resistances such as the internal gate series resistance and the parasitic capacitances in the devices must be reduced for fast switching speed.

III. Preparation of the U-Grooved SIT CMOS

The U-grooved structure plays an important role in the fabrication of the MOS SIT with large transconductance and small parasitic capacitance [18]. This structure has not only small capacitance but also can be built with a very short channel, due to the fact that it is formed vertically. While submicrometer resolution is difficult by conventional photolithography using visible light, the precision of depth-wise processing can be determined by the deposition or the etching rate. Thus the submicrometer channel length can be realized reproducibly. There have been lately some other technologies to realize minute structures such as X-ray lithography or electron-beam lithography, but these approaches encounter some problems such as quality of the photoresist.

A. Device Structure

Fig. 6 shows a cross-sectional view of the U-grooved SIT CMOS inverter gate. The U grooves are formed on

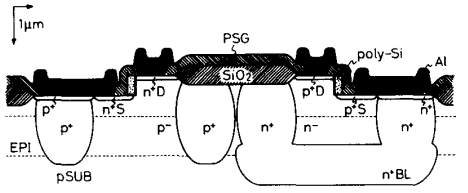


Fig. 6. Cross-sectional view of the U-grooved SIT CMOS.

the surface of the p (100) substrate along the ⟨100⟩ direction at an angle of 45° from the ⟨110⟩ orientation surface. In this structure, both surface of the substrate and the sidewall surfaces of the grooves are formed by (100) planes. It is easy to design the U-grooved MOS SIT and the planar MOS SIT (or FET) on the same chip. As the U-groove depth is 0.5 μm, the surface steps caused by the grooves are not so large compared with the steps caused by the deposited films such as oxide, poly-Si, and Al.

At the sidewall of the U groove, a gate oxide film 20 nm in thickness is formed and the formation of self-aligned poly-Si gate adjacent to it takes place.

The drain region is formed at the top of the surface, and the source region at the bottom of the U groove. There are no overlapped portions across the channel in these regions in order to reduce the bulk current which cannot be controlled by the gate electrode. Channels are formed in the epitaxial layer divided into two steps of growth to reduce the thermal treatment time for the formation of the deep channel stoppers. To isolate the n-channel transistor and the p-channel transistor from each other, an n^+ buried layer is formed in the substrate. This n^+ layer prevents latch-up.

Fig. 7 shows the surface SEM photograph of a U-grooved MOS SIT in which the Al wiring and the passivation oxide film are removed to clearly reveal the gate structure. It is seen that the gate poly-Si is just adjacent to the sidewall of the groove and the gate contact pad is formed on the field oxide film.

In the fabrication of this structure, the design rule F is chosen as 3, 2, 1.5, and 1 μm. As the mask alignment margin is taken to be $F/2$, one inverter gate occupies an area of $18F \times 6F$.

B. Fabrication Process

The fabrication process of the U-grooved SIT CMOS is as follows:

a) A p (100) substrate (resistivity = 8–12 $\Omega \cdot$ cm) is used. First, $^{75}As^+$ (does = 2×10^{15} cm^{-2}) is implanted for the formation of an n^+ buried layer. After annealing, an epitaxial layer (5×10^{13} cm^{-3}, 1 μm) is grown in a low-pressure $SiCl_4/H_2$ CVD system at 1100°C and 76 torr. The channel of the n-channel transistor (5×10^{12} cm^{-2}) and its surroundings for a channel stopper (5×10^{14} cm^{-2}) are implanted with $^{11}B^+$. In the case of the p-channel transistor, implantation of $^{31}P^+$ is performed. Afterwards, another 1 μm thick epitaxial layer is regrown (Fig. 8(a)).

Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on March 08,2010 at 00:46:18 EST from IEEE Xplore. Restrictions apply.

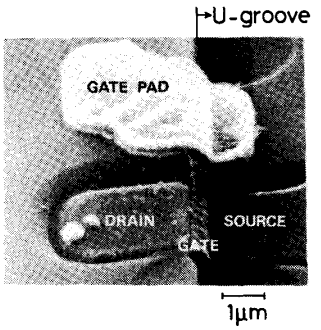


Fig. 7. Surface SEM photograph of the U-grooved MOS SIT.

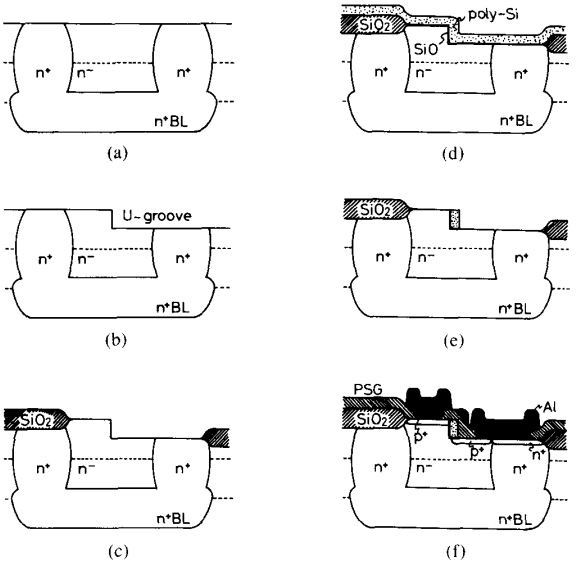


Fig. 8. Process sequence of the U-grooved SIT CMOS.

b) The U-shaped groove with a depth of 0.5 μm is etched by PCl_3 anisotropic plasma etching [19] at 0.05 torr (Fig. 8(b)).

c) An active area including the U groove is defined and the field oxide film is formed by the conventional LOCOS method (Fig. 8(c)).

d) The thin gate oxide film is formed by dry oxidation, and the poly-Si film for the gate electrode is deposited to a thickness of 350 nm using the SiH_4/H_2 CVD system. Impurities are deposited simultaneously by using PH_3 or B_2H_6, because the poly-Si adjacent to the sidewall of the U groove cannot be doped sufficiently by ion implantation. The sheet resistance of both n^+ and p^+ poly-Si are about 50 and 150 $\Omega/\square$, respectively (Fig. 8(d)).

e) The gate poly-Si film is etched by PCl_3 anisotropic plasma etching at 0.1 torr in such a way as to retain it on the sidewall of the U groove. To reduce the gate series resistance, silicide formation is effective [20]. W silicides or Ti silicides are formed by electron-beam evaporation and rapid thermal annealing. A sheet resistance of 15 $\Omega/\square$ in W silicide and 2 $\Omega/\square$ in Ti silicide is obtained (Fig. 8(e)).

f) The drain/source in both the n-channel transistor and the p-channel transistor (6×10^{15} cm^{-2}) are implanted with $^{31}P^+$ and $^{49}BF_2^+$, respectively, using the gate poly-Si as a self-aligned mask. Simultaneously, contact layers to the p substrate and the n^+ buried layer are formed.

A PSG/SiO_2 film with a thickness of 350 nm is deposited for passivation using a $SiH_4/O_2/PH_3$ CVD system. After opening the contact holes, Al–Si is evaporated to a thickness of 500 nm for metallization (Fig. 8(f)).

As mentioned above, the fabrication process of the U-grooved SIT CMOS is nearly identical to that of Bi-CMOS except for the U-groove etching process.

The problem that arises in the fabrication of the U-grooved structure is the damage and contamination during plasma etching. For example, n-type C–V characteristic occurs at the as-etched surface even if a p-type substrate is used. A combined use of slight plasma etching with $SiCl_4$, chemical oxidation with a HNO_3/HCl solution, and light etching of oxide is very effective for removing the layer contaminated by phosphorus, etc. Fig. 9 shows the C–V characteristics of the Al gate MOS diode after the above treatment. The solid line indicates the etched samples, and the dotted line indicates the control samples. A small amount of flat-band voltage shift and the tail characteristics are observed in the etched sample, but a surface-state density of about 1×10^{11} eV · cm^{-2} and a breakdown electric field of about 10 MV/cm are obtained. These values are sufficient to fabricate a MOS transistor at the etched surfaces.

C. Electrical Characteristics

Typical drain current versus drain voltage characteristics of the n-channel and p-channel transistors with 1-μm channel width are shown in Fig. 10. Up to the current scale of 10 μA per division in Fig. 10(a) and (b), the drain current does not saturate as with a vacuum triode tube. Over a wide current range, the drain current increases exponentially with increasing drain bias voltage. Thus it is considered that the current flow follows the mechanism of the barrier height control in the channel. At a current level of around 100 μA per division in Fig. 10(c) and (d), the drain current tends to saturate due to the effect of residual source series resistance.

Fig. 11 shows the typical drain current versus gate voltage characteristics related to the conductivity type of the poly-Si gate and the channel. The n-channel transistor with the n^+ poly-Si gate and the p-channel transistor with the p^+ poly-Si gate are the depletion/enhancement modes in which a small amount of drain current flows when the gate bias is equal to zero. This is due to the drain-induced barrier lowering (the so-called short-channel effect). These devices have large transconductance even at a relatively low gate bias of 2 V or less. In order to realize the enhancement mode in which no drain current flows when the gate bias is equal to zero, it is useful to apply the p^+

Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on March 08,2010 at 00:46:18 EST from IEEE Xplore. Restrictions apply.

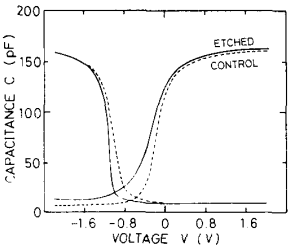
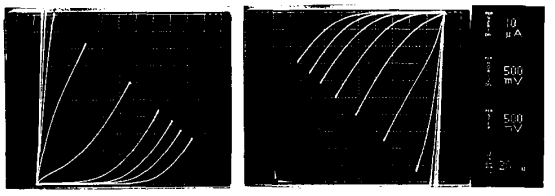
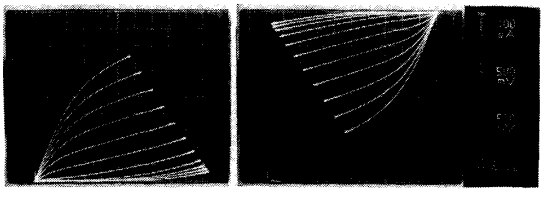


Fig. 9. C–V characteristics of the plasma-etched surface.



(a) n-channel (b) p-channel



(c) n-channel large current (d) p-channel large current

Fig. 10. Drain current versus drain voltage characteristics of the U-grooved MOS SIT.

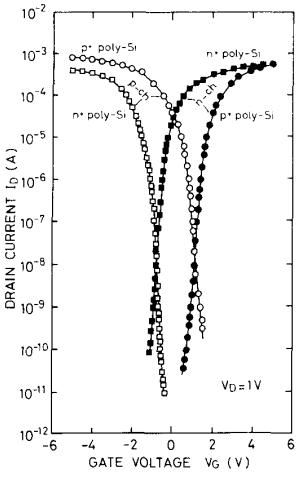


Fig. 11. Drain current versus gate voltage characteristics of the U-grooved MOS SIT.

poly-Si gate for the n-channel transistor and the n^+ poly-Si gate for the p-channel transistor. Due to the work function difference between p^+ poly-Si and n^+ poly-Si, a potential barrier of sufficient height to cut off the drain current is formed even if the gate bias is equal to zero. Although the enhancement mode can be realized by increasing the impurity concentration of the channel, drain current saturation occurs, reducing transconductance.

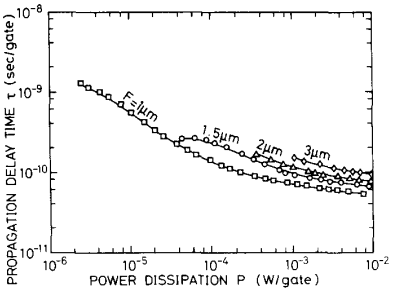


Fig. 12. Variation with design rules in p–τ curves of the U-grooved SIT CMOS: $W/F = 1$ where W is the channel width and F is the design rule.

All types of U-grooved MOS SIT have large transconductance. A maximum transconductance of 106 mS/mm in the n-channel transistor and 100 mS/mm in the p-channel transistor are obtained at a drain voltage of 1 V. This value is at least one order of magnitude greater than that of the 0.8 μm gate planar MOS SIT. Therefore, it appears that the U-grooved SIT CMOS has a potential comparable to Bi-CMOS technology [21].

In order to evaluate the switching characteristics, 31-stage ring oscillators have been fabricated. Fig. 12 shows the power dissipation versus propagation delay time (p–τ) curves at varying design rules while maintaining the ratio of the channel width W and the design rule F to be unity. As the design rule is miniaturized, the device operates with higher speed and lower power. At a design rule of 1 μm, a minimum dissipation energy of 3 fJ/gate is obtained for oscillation. Also, a minimum propagation delay time of 49 ps/gate, which is faster than that of the bulk FET CMOS [22], is obtained at a dissipation power of 7 mW/gate, which corresponds to a p–τ product of 350 fJ/gate.

In Fig. 13, the depletion/enhancement mode device and the enhancement mode device are compared on the p–τ curves. In the case of the former device, a propagation delay time of 180 ps/gate is obtained at a supply voltage of 1.5 V (36 μW), and 0.57 V operation is confirmed, too. Therefore, the former device is suitable for low-voltage high-speed operation. In the case of the latter device, a power dissipation of 9 μW is obtained at a supply voltage of 1.5 V (2.7 ns), showing its suitability for low-power operation.

In Fig. 14, the propagation delay time is plotted as a function of the reciprocal of transconductance $1/G_m$, where G_m is estimated from the I–V characteristics of ring oscillators. The propagation delay time decreases in proportion to the reduction of $1/G_m$. This result is similar to that of the circuit simulation as shown in Fig. 4. It is considered that the proportionality constant $1/G_m$ indicates the effective load capacitance per stage in the ring oscil-

Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on March 08,2010 at 00:46:18 EST from IEEE Xplore. Restrictions apply.

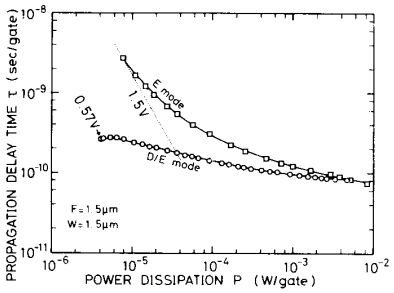


Fig. 13. Dependence of operation modes on p-τ curve of the U-grooved SIT CMOS.

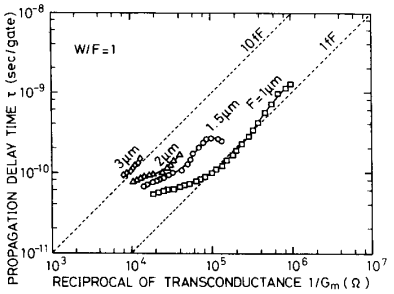


Fig. 14. Propagation delay time versus reciprocal of transconductance.

lator. This effective load capacitance can be reduced by miniaturization. The minimum propagation delay time is obtained at the point where G_m becomes largest. As the I-V characteristics tend to saturate as shown in Fig. 10(c) and (d), it is important to reduce the residual source series resistance for the improvement of G_m. Even if the transconductance becomes larger, however, the reduction of the propagation delay time tends to saturate. The reason for this may be attributed to the limited switching speed by the gate series resistance as shown by the data on circuit simulation in Fig. 5. The reduction of gate series resistance is another important problem for improvement of the propagation delay time.

IV. Conclusion

A circuit simulation by the discrete devices and elements which are in actual operation with large signals is a useful method to clarify what device parameters influence the propagation delay time of the SIT CMOS. According to the results of the circuit simulation, the propagation delay time is proportional to the load capacitance divided by the transconductance. Therefore, the devices must be designed to have a small input capacitance as well as a large transconductance.

To realize the MOS SIT with large transconductance and small input capacitance, the U-grooved structure is very appropriate. In this structure, parasitic capacitances are small, and the reproducibility of short-channel length is excellent because the channel is formed depthwise.

The U-grooved SIT CMOS is fabricated by PCl_3 anisotropic plasma etching. The damage and contamination during the plasma etching is sufficiently reduced to fabricate the MOS devices by the combinated use of $SiCl_4$ plasma etching, chemical oxidation with a HNO_3/HCl solution and light etching of the SiO_2.

The switching characteristic of the U-grooved SIT CMOS is measured by 31-stage ring oscillators. At the design rule of 1 μm, a minimum dissipation energy for oscillation of 3 fJ/gate is obtained. Also, a minimum propagation delay time of 49 ps/gate is obtained at a power dissipation of 7 mW/gate which corresponds to a p-τ product of 350 fJ/gate. As is the case with circuit simulations, the propagation delay time measured by the ring oscillator decreases in proportion to the reduction of $1/G_m$. In order to achieve further improvement in the propagation delay time, the reduction of the gate series resistance is another problem yet to be solved.

References

[1] Y. Watanabe and J. Nishizawa, Japanese Patent 205068, application date Dec. 20, 1950.
[2] J. Nishizawa, T. Terasaki, and J. Shibata, "Field effect transistor versus analog transistor (static induction transistor)," *IEEE Trans. Electron Devices*, vol. ED-22, no. 4, pp. 185-197, Aug. 1975.
[3] Y. Mochida, J. Nishizawa, T. Ohmi, and K. Gupta, "Characteristics of static induction transistors—Effect of series resistance," *IEEE Trans. Electron Devices*, vol. ED-25, no. 7, pp. 761-767, July 1978.
[4] W. Shockley, "Transistor electronics; Imperfections, unipolar and analog transistors," *Proc. IRE*, vol. 40, pp. 1280-1313, Nov. 1952.
[5] J. Nishizawa and K. Yamamoto, "High-frequency and high-power static induction transistor," *IEEE Trans. Electron Devices*, vol. ED-25, no. 3, pp. 314-322, Mar. 1978.
[6] Y. Kajiwara, M. Aiga, Y. Higaki, M. Kato, Y. Yukimoto and K. Shirahata, "A 100 W static induction transistor operating at 1 GHz," in *Proc. 1979 Int. Conf. on Solid State Devices* (Tokyo, Japan), *Jap. J. Appl. Phys.*, suppl., vol. 19-1, pp. 305-308, 1980.
[7] J. Nishizawa and K. Nakamura, "Characteristics of new thyristors," in *Proc. 1976 Int. Conf. on Solid State Devices* (Tokyo, Japan), *Jap. J. Appl. Phys.*, suppl., vol. 16-1, p. 541, 1977.
[8] Y. Kajiwara, Y. Watanabe, M. Bessho, Y. Yukimoto, and K. Shirahata, "High speed and high voltage static induction thyristor," in *IEDM Tech. Dig.*, pp. 38-41, Dec. 1977.
[9] Y. Terasawa, K. Miyata, S. Murakami, T. Nagano, and M. Okamura, "High power static induction thyristor," in *IEDM Tech. Dig.*, pp. 250-253, Dec. 1979.
[10] J. Nishizawa and B. M. Wilamowski, "Static induction logic—A simple structure with very low switching energy and very high packing density," in *Proc. 1976 Int. Conf. on Solid State Devices*, (Tokyo, Japan), *Jap. J. Appl. Phys.*, suppl., vol. 16-1, pp. 151-154, 1977.
[11] J. Nishizawa, "Problems of miniaturized devices," in *Handoutai Kenkyu (Semiconductor Electronics)*, no. 18, pp. 3-25, chap. 1. Kougyochosakai, Japan: 1981 (in Japanese).
[12] Y. Mochida and T. Nonaka, "Application of SIT for logic LSI," in *Semiconductor Technology*, J. Nishizawa, Ed. New York, NY: Ohm & North-Holland, 1982, ch. 18.
[13] J. Nishizawa, N Takeda, and T. Ohmi, "High speed current mode logic of static induction transistor," in *Proc. 1st Speciality Conf. on Giga Bit Logic for Microwave Systems* (Orlando, FL, May 1979), pp. 65-72.
[14] P. Richman, "Moduration of space-charge limited current flow in insulated-gate field effect tetrode," *IEEE Trans. Electron Devices*, vol. ED-16, pp. 759-766, 1969.
—, *MOS Field Effect Transistor and Integrated Circuits*. New York, NY: Wiley Interscience, 1973, ch. 4.
[15] T. Nakamura, M. Yamamoto, H. Ishida, and M. Shinoda, "Submicron channel MOS-FET's logic under punch-through," *IEEE J. Solid-State Circuits*, vol. SC-13, no. 5, pp. 572-576, Oct. 1978.
[16] S. Suzuki, "SIT integrated circuits," Res. Rep. of Nishizawa Perfect Crystal Project, ERATO, 1983 (in Japanese).
[17] J. Nishizawa, "MOS SIT—Its characteristics and theory," *Electron. Parts Mater.*, pp. 74-79, Aug. 1979 (in Japanese).

Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on March 08,2010 at 00:46:18 EST from IEEE Xplore. Restrictions apply.

[18] N. Takeda, "Si CMOS SIT integrated circuits," Res. Rep. of Nishizawa Perfect Crystal Project, ERATO, pp. 33-41, Dec. 1986 (in Japanese).
[19] K. Takahashi, S. Suzuki, and J. Nishizawa, "Anisotropic dry etching by using PCl_3," Tech. Rep. of Inst. Electron Communication Engrs., Japan, vol. 80, no. 23, SSD80-34, 1980 (in Japanese).
[20] K. Tsukamoto, T. Okamoto, M. Shimizu, T. Matsukawa, and H. Harada, "Self-aligned titanium silicidation by lamp annealing," in *Extended Abstracts of the 16th (1984 Int.) Conf. on Solid State Devices and Materials*, (Kobe, Japan, 1984), pp. 47-50.
[21] H. Higuchi, G. Kitsukawa, T. Ikeda, Y. Nishio, N. Sasaki, and K. Ogiue, "Performance and structure of scaled-down bipolar devices merged with CMOS FETS," in *IEDM Tech. Dig.*, pp. 694-697, 1984.
[22] H. Momose, H. Shibata, S. Saito, J. Miyamoto, K. Kanazaki, and S. Kohyama, "1.0 μm n-well CMOS/bipolar technology," *IEEE Trans. Solid-State Circuits*, vol. SC-20, no. 1, pp. 137-143, Feb. 1985.

*

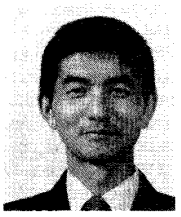
Jun-ichi Nishizawa (M'57-SM'62-F'69), was born in Sendai, Japan, on September 12, 1926. He received the B.S. degree in 1948 and the Doctor of Engineering degree in 1960 from Tohoku University, Sendai, Japan.

Following a year as a Research Assistant, he became an Associate Professor in 1954, a Professor in 1962, and Director in 1983 at the Research Institute of Electrical Communication, Tohoku University, where he served a term until 1985. In 1968, he was appointed Director of the Semiconductor Research Institute in Sendai and holds the post at present. His main work has involved the inventions of p-i-n diodes and p-n-i-p (n-p-i-n) transistors in cooperation with p-i-n photodiodes (1950), ion implantation (1950), avalanche photodiodes (1952), semiconductor injection lasers (1957), solid-state focusing optical fibers (1964), and transit time effect negative-resistance diodes (1954) including the avalanche injection and the tunnel injection (1958), hyperabrupt variable capacitance diodes (1959), semiconductor inductance (1957), static induction transistor (SIT) (1950, 1971), etc. At present, he is carrying out work specializing in development of static induction transistors to high frequencies and high-power devices, the high-speed thyristor, and the high-speed and low power dissipation integrated circuit, and growth method of III-V compound semiconductors: a temperature difference method under controlled vapor pressure (TDM-CVP) giving rise to high-efficiency LED and long-life laser diodes based on silicon perfect crystal technology by lattice constant compensation. He also originated electroepitaxy (1955) and photoepitaxy (1961). He discovered the avalanche effect in semiconductors and explained the backward character of the p-n junction by this effect (1953).

Nobuo Takeda was born in Shizuoka Prefecture, Japan, on November 14, 1956. He received the B.S., M.S., and Ph.D. degrees in electronics from Tohoku University, Sendai, Japan, in 1979, 1982, and 1985, respectively.

He joined the Fundamental Structure Research Laboratory, Prof. Nishizawa's Perfect Crystal Technology Research Project, Exploratory Research for Advanced Technology, Japan in 1985, where he has been engaged in research and development of SIT CMOS. In 1986, he was employed by the Semiconductor Research Institute, Sendai, Japan and has been working in research and development of SIT.

*



Sohbe Suzuki (S'72-S'78-M'78) received the B.S. degree in electronics in 1972 from Shizuoka University and the M.S. and Ph.D. degrees in electronics from Tohoku University in 1974 and 1978, respectively.

He joined the Semiconductor Research Institute in Sendai in 1978. Since 1979 he has been working on research and development of SIT. He is now a staff engineer of the laboratory.

*

Toshifumi Suzuki was born in Morioka, Japan, on August 28, 1962. He received the B.S. and M.S. degrees in electronics from Tohoku University, Sendai, Japan, in 1986, and 1988, respectively, where he studied CMOS SIT.

Since 1988, he has been engaged in research on ideal static induction transistor (ISIT) in Prof. Nishizawa's TeraHertz Project, Exploratory Research for Advanced Technology, Research Development Corporation of Japan.

*

Tetsu Tanaka was born in Sendai, Japan, on March 3, 1964. He received the B.S. degree in electrical engineering from Tohoku University in 1987. Now he is studying electrical engineering in M.C. of Tohoku University.

Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on March 08,2010 at 00:46:18 EST from IEEE Xplore. Restrictions apply.