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Three-Dimensional Integration Technology Based on Wafer Bonding With Vertical Buried Interconnections

Mitsumasa Koyanagi, *Fellow, IEEE*, Tomonori Nakamura, Yuusuke Yamada, Hirokazu Kikuchi, Takafumi Fukushima, Tetsu Tanaka, and Hiroyuki Kurino, *Member, IEEE*

***Abstract*—A three-dimensional (3-D) integration technology has been developed for the fabrication of a new 3-D shared-memory test chip. This 3-D technology is based on the wafer bonding and thinning method. Five key technologies for 3-D integration were developed, namely, the formation of vertical buried interconnections, metal microbump formations, stacked wafer thinning, wafer alignment, and wafer bonding. Deep trenches having a diameter of 2 μm and a depth of approximately 50 μm were formed in the silicon substrate using inductively coupled plasma etching to form vertical buried interconnections. These trenches were oxidized and filled with n+ polycrystalline silicon or tungsten. The 3-D devices and 3-D shared-memory test chips with three-stacked layers were fabricated by bonding the wafers with vertical buried interconnections after thinning. No characteristic degradation was observed in the fabricated 3-D devices. It was confirmed that fundamental memory operation and broadcast operation between the three memory layers could be successfully performed in the fabricated 3-D shared-memory test chip.**

***Index Terms*—Buried interconnection, microbump, three-dimensional (3-D) large-scale integration (LSI), wafer bonding, 3-D memory.**

I. Introduction

A SERIOUS problem for large-scale integration (LSI) is that the signal propagation delay and the power consumption by the interconnections increase significantly as the LSI capacity increases. In addition, I/O circuits in LSI tend to consume more power due to the need to rapidly drive the output pins and the external wiring with large capacitances and inductances in package and print circuit boards. As a result, it is difficult to achieve high performance and low power consumption in LSIs. To overcome these problems associated with the interconnections and the I/O circuits, the wiring length, the chip size, and the pin capacitance have to be reduced. Three-dimensional (3-D) LSI satisfies these requirements, and thus, it has been attracting considerable attention from many researchers in the LSI device and package technology areas [1]–[9]. We can easily reduce the wiring length, the chip size, and the pin capacitance by employing 3-D LSIs, and consequently, we can increase the signal processing speed and decrease the power consumption. Three-dimensional LSIs are also useful for increasing the wiring connectivity within a chip. It therefore becomes possible to produce new kinds of LSIs such as real-time image processing chips, neuromorphic chips, memory-merged processor chips, and intelligent memory chips by using 3-D LSIs [10]–[23]. Thus, 3-D LSIs have many attractive potential uses.

We have developed a 3-D integration technology based on wafer bonding and thinning to produce 3-D LSIs. In this paper, we describe our 3-D integration technology and demonstrate the fundamental characteristics of 3-D devices and 3-D shared-memory test chip fabricated using the 3-D integration technology.

II. Fabrication Process for 3-D LSI

The concept of 3-D LSI itself is not new. Several papers on 3-D devices or 3-D LSI test chips have been published [24]–[32]. A typical LSI using 3-D devices is dynamic random access memory (DRAM). The stacked-capacitor (STC) cell with a 3-D structure, which was proposed by M. Koyanagi, has been employed in DRAMs, having a memory capacity of exceeding 1 Mbits [24]–[26]. A storage capacitor is stacked on a switching transistor in an STC cell. Another example of 3-D devices is the stacked CMOS device proposed by J. F. Gibbons, in which a p-channel MOSFET (pMOSFET) is stacked on an n-channel MOSFET (nMOSFET) [27]. In this stacked CMOS device, the pMOSFET is fabricated from a polycrystalline silicon (poly-Si) film, the grain sizes of which are enlarged by laser annealing. The first genuine 3-D LSI test chip having three device layers was reported by Akasaka and Nishimura [28]. In this 3-D LSI test chip, MOSFETs are fabricated in poly-Si films formed on an LSI wafer. The poly-Si film is recrystallized by laser annealing prior to fabricating the MOSFETs to improve the electrical characteristics of the poly-Si film. Two poly-Si layers with MOSFETs are stacked on an LSI wafer in this 3-D LSI test chip. However, the 3-D LSI fabrication process using laser recrystallization has a critical flaw, in that, the fabrication process is sequential, and hence, it requires a very long fabrication time. Another problem is that the electrical characteristics of MOSFETs fabricated in recrystallized poly-Si films are inferior to those of devices fabricated in a single crystal silicon (single-Si) substrate. A more realistic 3-D LSI fabrication process using a thinned-wafer transfer method was proposed by Hayashi *et al.* [32]. In this 3-D LSI process, an LSI wafer in which devices are fabricated is glued to a supporting material and then thinned from the back surface by mechanical grinding and polishing to a thickness of approximately 0.5 μm. This thinned LSI wafer is bonded to another LSI wafer, and then, the supporting material

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The authors are with the Department of Bioengineering and Robotics, Tohoku University, Sendai 980-8579, Japan (e-mail: koyanagi@sd.mech.tohoku.ac.jp).

Color versions of Figs. 1–3 are available online at http://ieeexplore.ieee.org.

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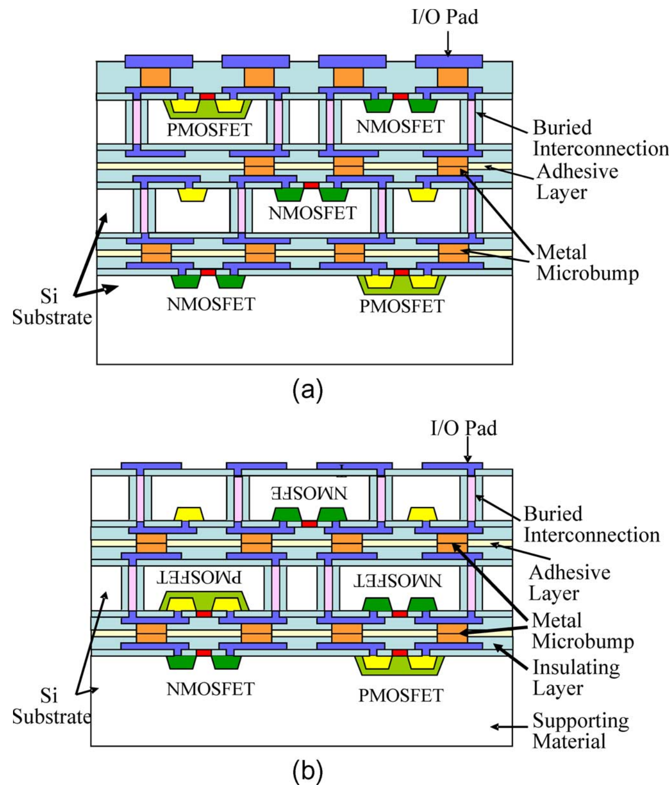

Fig. 1. Cross-sectional structure of 3-D LSI. (a) Faceup stacking. (b) Facedown stacking.

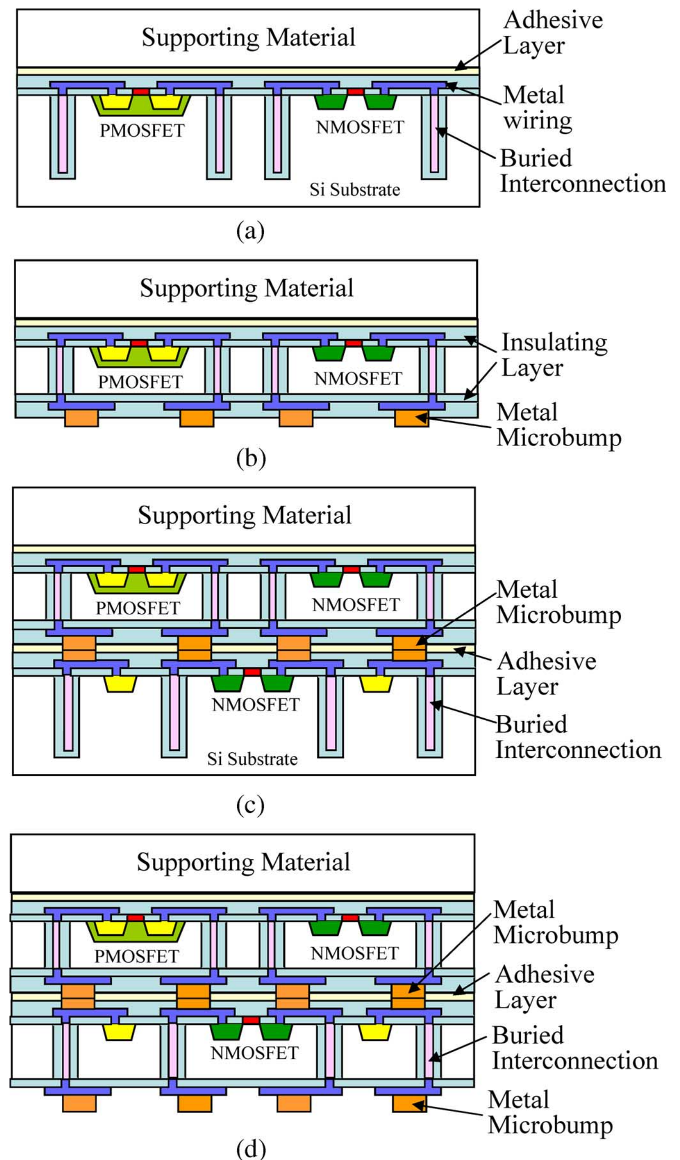

Fig. 2. Fabrication process flow for 3-D LSI in which the buried interconnections are formed before wafer bonding.

is removed from the thinned LSI wafer. In doing so, the thinned LSI wafer is transferred to the other LSI wafer. This fabrication method is very attractive because we can fabricate 3-D LSIs by bonding completed LSI wafers and significantly reduce the fabrication time. However, the main problem with this method is transferring the extremely thin LSI wafer having a thickness of less than 0.5 μm onto the other LSI wafer. This procedure is difficult because the thin LSI wafer is very fragile. In addition, the wafer thinning down to 0.5 μm and the wafer transfer processes may degrade the device characteristics. To solve these problems during the thinned wafer transfer process, the LSI wafer should not be thinned to a thickness less than several tens of micrometers. However, it is not possible to establish an electrical interconnection between the device layers if the relatively thick silicon layers having thicknesses of several tens of micrometers remain after wafer thinning. Therefore, vertical interconnections have to be formed in the silicon substrate when relatively thick wafers are employed in wafer bonding. We proposed forming vertical buried interconnections in the LSI wafer prior to thinning the wafer [33]–[35]. The buried interconnections are produced using a deep trench formed in the wafer. An insulating film such as silicon oxide film is formed on the trench surface before filling the trench with an electrically conducting material. The bases of the buried interconnections are exposed after thinning the wafer. Several silicon wafers having such buried interconnections are stacked in our 3-D integration technology.

The cross-sectional structures of the 3-D LSI fabricated by our 3-D integration technology are illustrated in Fig. 1. The thinned upper layers are stacked faceup onto the thick LSI wafer with its faceup as shown in Fig. 1(a), while Fig. 1(b) shows the arrangement when the thinned upper layers are stacked facedown onto the thick LSI wafer. In these 3-D LSIs, a relatively thick silicon substrate remains after completing the fabrication process shown in Fig. 1. This remaining silicon substrate is useful for reducing the damage caused to the devices during the 3-D fabrication process. The electrical interconnection in the vertical direction is created by the buried interconnections and the metal microbumps in both types of 3-D LSIs. The fabrication process flow for the 3-D LSI shown in Fig. 1 is illustrated in Fig. 2. In the depicted process flow, the vertical buried interconnections are formed in the silicon substrate first, but they can be formed either before or after the multilevel metallization process. When the buried interconnections are formed before the multilevel metallization process, the metal microbumps are formed on the top surface of the chip and connected with the buried interconnections by the multilevel metallization layers. For the case when the buried

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interconnections are formed after the multilevel metallization process, they have to be formed through the thick multilevel metallization layers into the silicon substrate. Thus, it may be difficult to employ this method for an LSI wafer having a multilevel metallization of more than five levels; for such a case, it is recommended to form the buried interconnections before the multilevel metallization process. After the formation of buried interconnections, the thick LSI wafer with the buried interconnections is glued to the supporting material as shown in Fig. 2(a). Various kinds of materials can be used as the supporting material, including quartz glass, a bare silicon wafer, and an LSI wafer. The LSI wafer glued to the supporting material is thinned from the back surface by the mechanical grinding and chemical mechanical polishing (CMP) to expose the base of the buried interconnections. This is followed by the formation of metal microbumps as shown in Fig. 2(b). The thinned LSI wafer with the supporting material is then bonded to another thick LSI wafer having buried interconnections as shown in Fig. 2(c). Then, the bottom thick LSI wafer is thinned from the back surface and metal microbumps are formed on the base of the buried interconnections as shown in Fig. 2(d). By repeating this sequence, a 3-D LSI can be easily fabricated. Finally, we can obtain a 3-D LSI having the structure shown in Fig. 1(a) by removing the supporting material. A 3-D LSI having the structure shown in Fig. 1(b) can be obtained by employing an LSI wafer as the supporting material. In this case, the first LSI wafer with the buried interconnections and the supporting LSI wafer are bonded face to face. In this 3-D integration technology, the thick LSI wafer which acts as the supporting material remains even after completing the 3-D fabrication process. Therefore, a very wide range of thicknesses from several tens of nanometers to several tens of micrometers can be used for the thinned wafers bonded to the thick LSI wafer.

A variation of this 3-D integration technology is shown in Fig. 3. In this 3-D integration technology, the buried interconnections are formed after thinning the LSI wafer. The thick LSI wafer without the buried interconnections is glued to a supporting material as shown in Fig. 3(a). A thick LSI wafer can be employed as a supporting material. The LSI wafer glued to the supporting material is thinned from the back surface by mechanical grinding and CMP as shown in Fig. 3(b). After that, deep trenches are formed in the thinned LSI wafer from the back surface as shown in Fig. 3(c). Then, an insulating film such as a silicon oxide film is formed on the trench surface, and the trenches are filled with an electrically conducting material after the insulating film at the base of the trench has been selectively removed by a reactive ion etching. After filling the trenches, metal microbumps are formed on the tops of the buried interconnections as shown in Fig. 3(d). By repeating this sequence, a 3-D LSI can be fabricated as shown in Fig. 3(e). This 3-D integration technology is useful for the case when there are no spaces to form the buried interconnections on the front surface, as is the case for logic LSIs having many metallization layers.

In this paper, we mainly describe the 3-D integration technology based on wafer bonding. However, our technology can be applied to a chip-to-chip bonding and to a chip-to-wafer

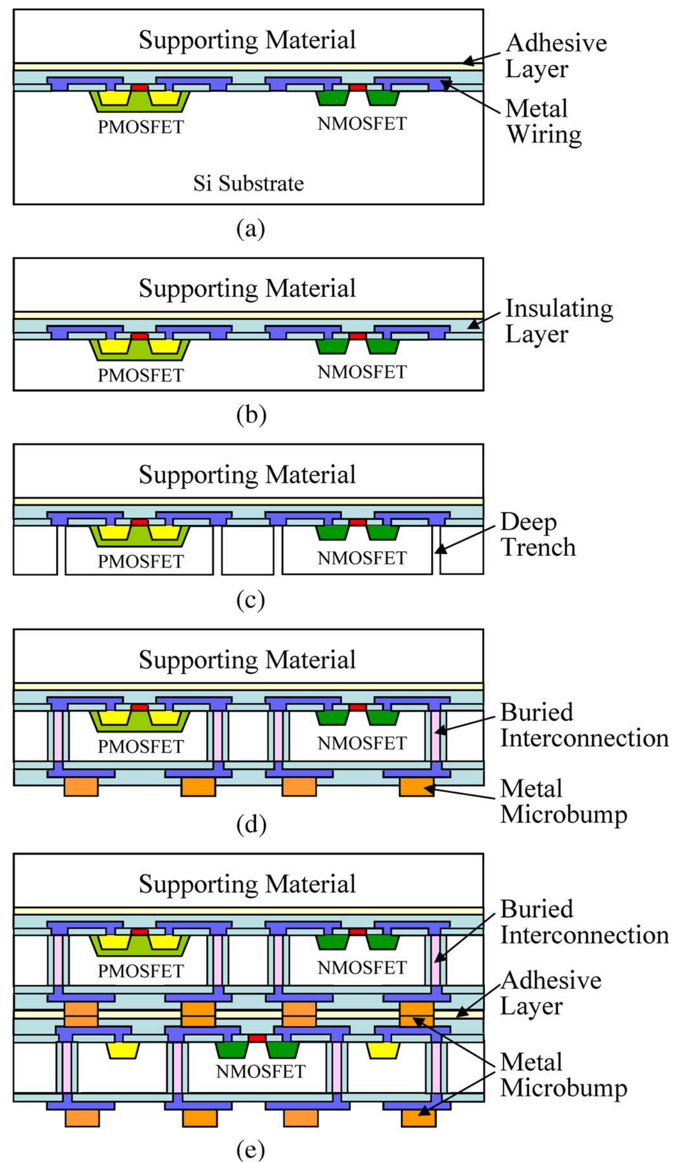

Fig. 3. Fabrication process flow for 3-D LSI in which the buried interconnections are formed after wafer bonding.

bonding as well. Three-dimensional integration technologies for chip-to-chip bonding and chip-to-wafer bonding involve dicing an LSI wafer with buried interconnections in the LSI chips after thinning from the back surface to expose the base of the buried interconnections and then bonding these LSI chips onto a thick LSI chip or a thick LSI wafer. We can fabricate 3-D LSIs using known good dies, and hence, we expect a higher production yield for these 3-D integration technologies. However, these technologies provide a lower production throughput. Therefore, the 3-D integration technology based on the wafer bonding is preferable when the wafer production yield is high since it provides a higher production throughput.

III. Fundamental Characteristics of 3-D Devices

We have fabricated a device test chip having a 3-D stacked structure (3-D device test chip) to evaluate the effect of the 3-D fabrication process on the device characteristics. To fabricate

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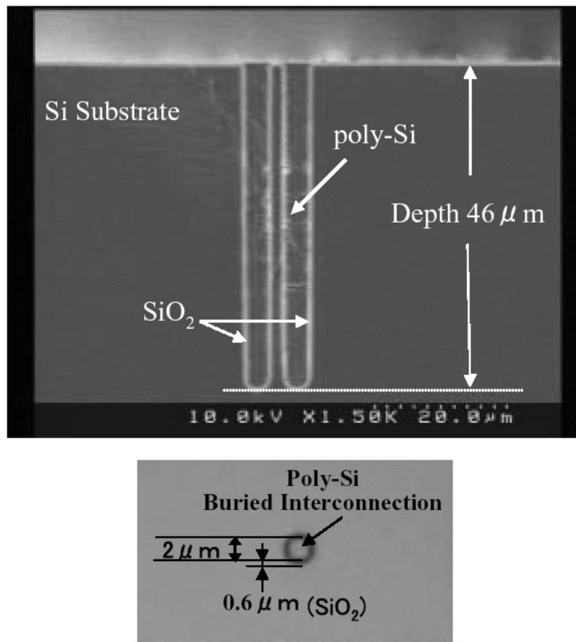

Fig. 4. Micrographs of a poly-Si buried interconnection. Upper figure: SEM cross-sectional view. Lower figure: Photomicrograph of the back surface with the base of the buried interconnection exposed.

the 3-D device test chip based on the fabrication process depicted in Fig. 2, we have developed five key technologies, namely, the formation of buried interconnections, microbumps, stacked wafer thinning, wafer alignment, and wafer bonding. At first, it is necessary to form deep trenches in the silicon substrate (Si trenches) in order to produce the buried interconnections, which act as vertical interconnections. Silicon trenches with a diameter of 2 μm and a depth of approximately 50 μm were formed using inductively coupled plasma etching. The Si trenches were then oxidized and filled with n+ poly-Si (0.4 m$\Omega \cdot$ cm) by low-pressure chemical-vapor deposition as shown in Fig. 4. For the case when the buried interconnections having a much lower resistance are required, the trenches are filled with tungsten. After filling the Si trenches with n+ poly-Si or tungsten, the wafer is bonded to the supporting material and then thinned to approximately 30 μm from the back surface using mechanical grinding and CMP techniques. A photomicrograph of the back surface after wafer thinning is shown in Fig. 4 where the base of the buried interconnection having a diameter of 2 μm is clearly visible. After thinning the wafer, In–Au microbumps were formed on the back surface using the liftoff technique. The thinned wafer was then aligned and temporarily bonded to the bottom device wafer. In–Au microbumps were also formed on the front surface of the bottom wafer before aligning the two wafers. We have developed a new wafer aligner having an alignment accuracy of ± 1 μm for 3-D integration technology [35]. This wafer aligner can also provide a uniform force and has a function to increase the temperature during temporary wafer bonding to guarantee firm contact between the upper and lower microbumps. The In–Au microbumps and an epoxy adhesive layer are used to bond two wafers. The liquid epoxy adhesive is injected into the gap of approximately 3 μm between the two wafers in a vacuum chamber after the temporary bonding of the microbumps [35]. Then, the bottom wafer was thinned again to approximately 30 μm from the back surface to expose the buried interconnections. By repeating this sequence three times, we fabricated a 3-D stacked device test chip having three layers.

We evaluated the electrical characteristics of the buried interconnections by measuring the voltage dependencies of their resistance, capacitance, and leakage current using daisy chains having 72 pairs or 144 pairs of poly-Si buried interconnections and In/Au microbumps which were allocated to the three layers of the 3-D device test chip. The cross-sectional area of the poly-Si buried interconnections is 2 by 12 μm. As a result, a resistance of approximately 10 Ω and capacitance of 0.217 pF at an applied voltage of 0 V were obtained for a single pair of poly-Si buried interconnection and In/Au microbump. The resistance decreased to 0.23 Ω when tungsten was used for the buried interconnection. We also evaluated the fundamental characteristics of MOSFETs, which were fabricated in the 3-D stacked device test chip and confirmed that there were no observable differences between the current–voltage characteristics before and after wafer bonding and thinning. The input and output characteristics of an inverter chain having a 3-D stacked structure (3-D inverter chain) are shown in Fig. 5. The second layer is deliberately not shown so that the buried interconnections can be seen in the chip photomicrograph of Fig. 5(a). It is obvious from Fig. 5(b) that a normal output waveform is obtained in the 3-D inverter chain fabricated using our 3-D integration technology.

IV. Scaling Capability of the Buried Interconnection

Fig. 6 shows the scaling capability of the buried interconnection. The diameter, length, and RC delay of a buried interconnection, the silicon oxide thickness underneath the buried interconnection and the microbump size (side length) are plotted as a function of the buried-interconnection pitch in Fig. 6(a). The maximum number of buried interconnections as a function of the ratio of the total area of the buried interconnections to the chip area is plotted in Fig. 6(b). In deriving the maximum number of buried interconnections, we assumed that the area of each layer in the 3-D LSI is 10 by 10 mm, and the allowable area for the buried interconnections was 1%, 5%, and 10% of each layer. We approximated the RC (resistance–capacitance) delay of the buried interconnections as $2\rho\varepsilon \times (l/r)^2/\ln(1 + d/r)$, where ρ, l, r, ε, and d denote the resistivity of the buried interconnection material, the length and the radius of buried interconnection, the dielectric constant, and the thickness of the insulator underneath the buried interconnection, respectively. In the figure, the buried interconnection material is tungsten and the insulator underneath the buried interconnection is silicon oxide. It is obvious from the figure that we can significantly increase the maximum number of buried interconnections without a serious area penalty by reducing the buried-interconnection size. For example, we can form tens of thousands of vertical buried interconnections in a chip with an area penalty of 1 mm^2, even for the case of a buried-interconnection pitch of 10 μm. Therefore, in the case of a 3-D memory LSI, we can achieve approximately ten times higher packing density by stacking 11 memory layers compared with a conventional two-dimensional

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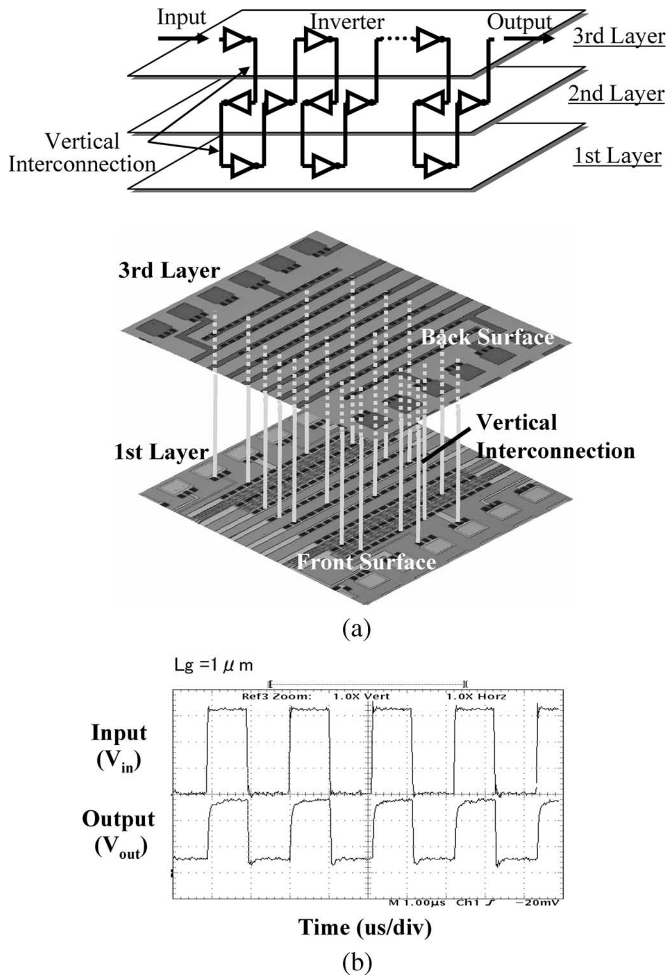

Fig. 5. Inverter chain with 3-D structure. (a) Photomicrograph of the fabricated inverter chain circuit having three stacked layers with the second layer omitted. (b) Measured waveforms of the inverter chain having three stacked layers.

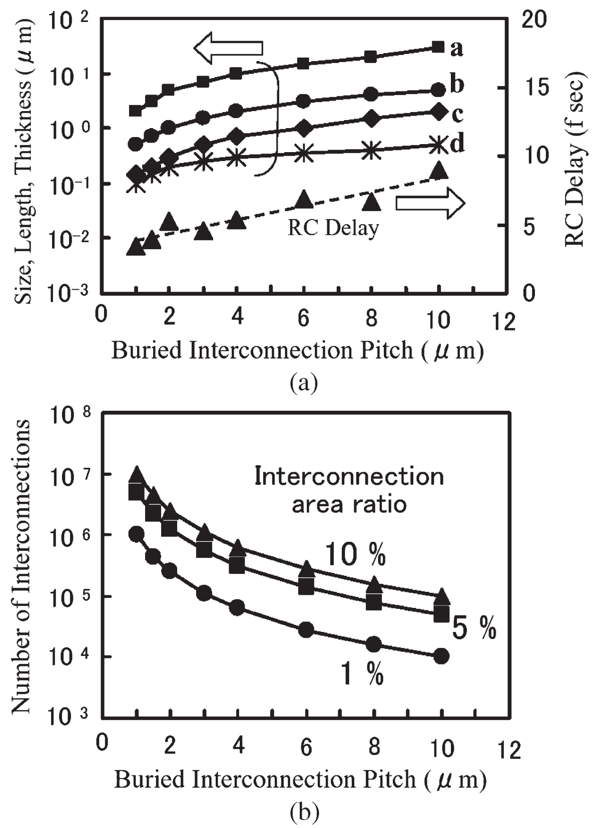

Fig. 6. Scaling capability of buried interconnection. (a) Diameter and length of buried interconnection, thickness of insulator underneath the buried interconnection, microbump size, and RC delay as a function of the buried-interconnection pitch. a—buried-interconnection length, b—microbump size, c—buried-interconnection diameter, and d—insulator thickness. (b) Number of buried interconnection as a function of buried-interconnection pitch.

memory chip having the same footprint. The total area penalty $(10\ \mathrm{mm}^2)$ for ten memory layers can be canceled out in the 11th layer. If the buried-interconnection pitch is reduced to 1 μm, we can form 10^6 buried interconnections in a chip with an area penalty of 1 mm^2. The RC delay of a buried interconnection decreases to less than 5 fs as the buried interconnection pitch is reduced to 1 μm.

It is very important to choose a suitable material for the buried interconnections in the 3-D integration technology based on wafer bonding with buried interconnections. Mostly, we have employed a low-resistive n+ poly-Si for the buried interconnections since poly-Si is a stable material and affects the device characteristics less than other materials. It is therefore suitable for the buried interconnection of a 3-D stacked DRAM. However, a tungsten or a copper is suitable for the buried-interconnection material in the case when buried interconnections having much lower resistances are required. Specifically, tungsten and copper are indispensable for scaling down the size of the buried interconnections. We have also developed a 3-D integration technology using tungsten buried interconnections. Fig. 7 shows SEM cross-sectional views of the tungsten buried interconnections having diameters of 1 and 0.6 μm. Ultrahigh-vacuum chemical vapor deposited was used for tungsten deposition. A thin poly-Si layer was formed to avoid peeling off the tungsten before tungsten deposition. It is obvious from the figure that the tungsten completely filled the deep Si trenches when the atomic-layer-deposition method was used. It is also obvious that the diameter of the buried interconnection and the distance between two adjacent buried interconnections (the buried-interconnection pitch) can be easily reduced to less than 1 and 2 μm, respectively. The resistivity of the buried interconnection can be reduced to approximately 2% of that of the low-resistive n+ poly-Si. We can further reduce the resistance of the buried interconnections by decreasing the buried-interconnections lengths and hence the silicon substrate thickness. We can easily decrease the silicon substrate thickness and hence the length of buried interconnection to less than 50 nm using our 3-D integration technology, since the thick supporting material can support such a thin silicon substrate. We have succeeded in bonding extremely thin LSI wafers with a silicon thickness of approximately 30 nm on the supporting material by employing silicon-on-insulator (SOI) LSI wafers and removing the thick silicon substrates of the SOI wafers after bonding.

V. Fabrication of 3-D Shared-Memory Test Chips

Three-dimensional LSIs are suitable for parallel processing and parallel data transferring due to the increased connectivity

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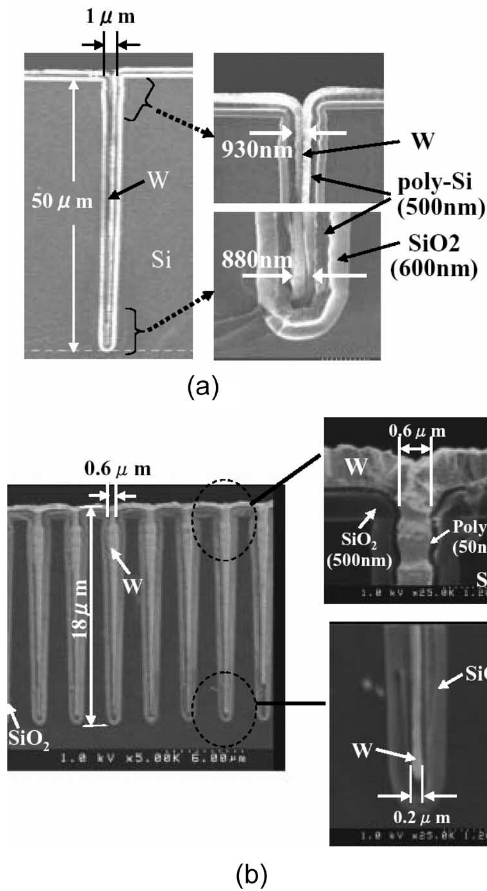

Fig. 7. SEM cross-sectional views of tungsten buried interconnections with diameters of (a) 1 μm and (b) 0.6 μm.

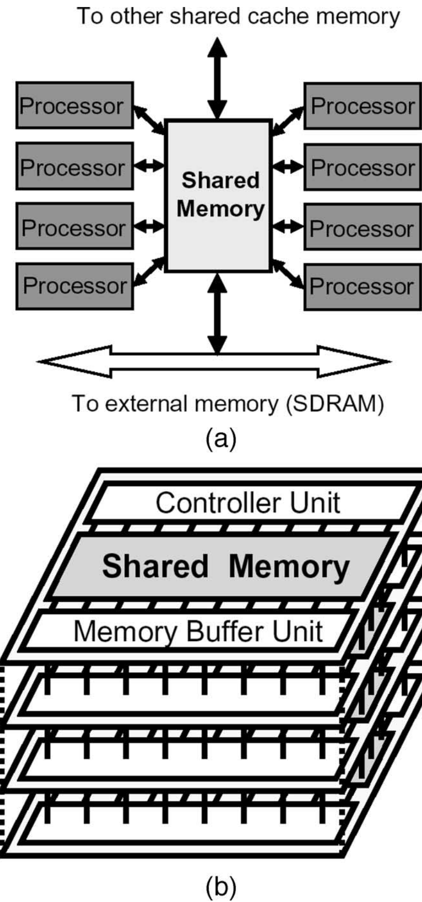

Fig. 8. Parallel processor system with a new shared memory. (a) System configuration. (b) Memory configuration of 3-D shared memory.

of their short vertical interconnections compared with conventional LSIs. We can create various kinds of new LSIs with parallel processing and parallel data transferring capabilities by employing 3-D stacked structures having many vertical interconnections. We propose a new shared memory having a 3-D stacked structure as an example of these new LSIs. A new shared memory with multiports is required in a high-performance parallel processor system. In a conventional parallel processor system having a shared memory, several processors are connected to a memory with large capacity through a common bus. The memory with large capacity acts as a shared memory in this system. A serious problem in this system is the memory access conflict caused by using a common bus. When the common bus is occupied by one processor, the other processors have to wait for memory access. Therefore, we cannot expect a dramatic increase in the performance of this system. However, we can solve this problem if we can create a new shared memory with multiports as shown in Fig. 8(a). We can realize a multiport memory by using a multiport static-random-access-memory (SRAM) cell. However, the number of memory ports is limited to three or four in such a multiport memory. To overcome this limitation, we propose a new shared memory with a 3-D stacked structure as shown in Fig. 8(b). Many memory layers are vertically stacked and connected by a large number of vertical interconnections, which act as broadcast buses. The processors are connected to their corresponding memory layers, and data written to a memory layer by its corresponding processor are simultaneously transferred to the other memory layers. As a result, memory cells having an identical address in each memory layers contain identical data which can be simultaneously read out by the respective processors without any access conflicts. Therefore, this 3-D memory can act as a shared memory with multiports. We can increase the number of memory ports by increasing the number of memory layers in this shared memory.

We fabricated a shared-memory test chip having a 3-D stacked structure by using our 3-D integration technology. We employed a conventional six-transistor SRAM memory cell in this 3-D shared-memory test chip, although a multiport SRAM memory cell or a DRAM memory cell could be employed instead. This 3-D shared-memory test chip consists of three memory layers and each memory layer has two memory mats to organize six ports as shown in Fig. 9. Each memory mat consists of a block of sense amplifiers and a 32-bit SRAM cell array. The three memory layers are connected by vertical buried interconnections, which act as vertical broadcast buses. The major sections of the memory circuits are shown in Fig. 10, where Fig. 10(a) depicts the memory cell circuit and Fig. 10(b) depicts the sense-amplifier circuit. The memory cell circuits are connected to the bit lines (BL, /BL) of the sense amplifier. The broadcast buses (BC and /BC) in Fig. 10(b) are composed of the vertical buried interconnections. The data transfer between the memory layers is performed through these broadcast buses,

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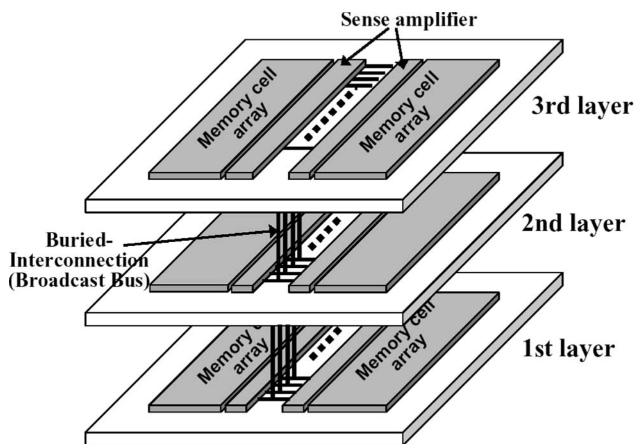
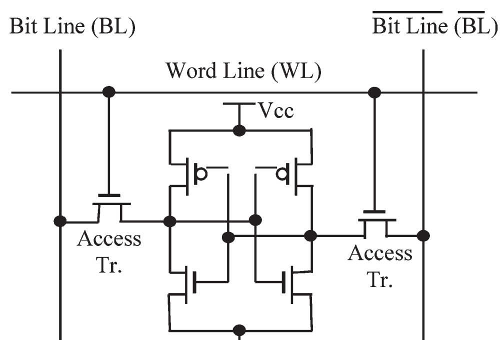


Fig. 9. Configuration of 3-D shared-memory test chip with three stacked layers.



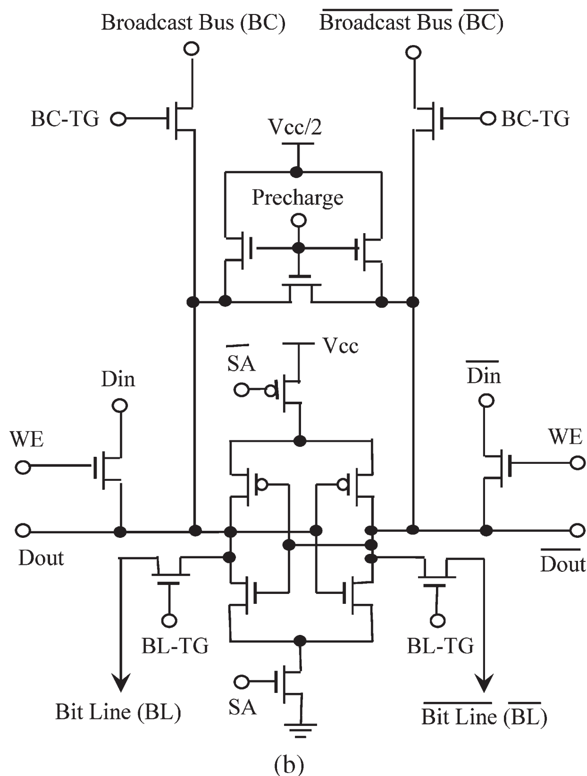
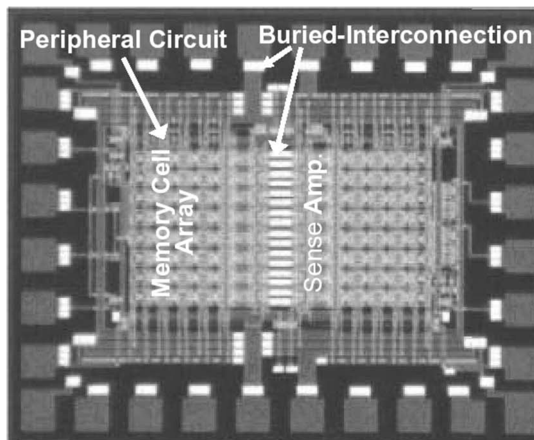


Fig. 10. Circuits for 3-D shared-memory test chip. (a) Memory cell. (b) Sense amplifier.



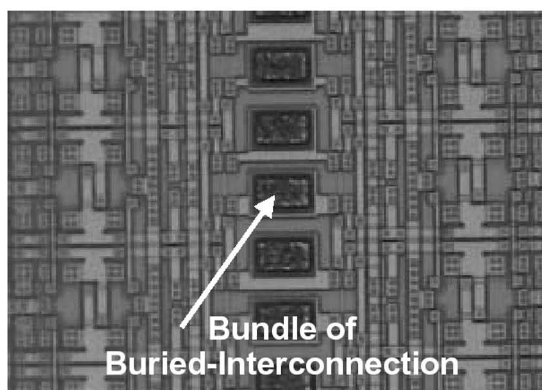


Fig. 11. Micrograph of the fabricated 3-D shared-memory test chip. (a) Photomicrograph for one memory layer of 3-D shared-memory test chip. Chip size is 2 × 1.6 mm. (b) Magnified photomicrograph of peripheral circuits such as sense amplifiers and bundles of buried interconnections.

which are driven by the sense amplifiers. The bit lines and the broadcast buses are precharged to half the supply voltage (1/2 Vcc) before data transfer. Assuming that the data are transferred from the first memory layer through the second memory layer to the third memory layer, then the sense amplifier in the first memory layer is activated by applying the clock signal to the SA and /SA terminals. The output signals of the sense amplifier in the first memory layer are then transferred to the broadcast buses by applying the clock signal to the BC–TG terminals. Next, the sense amplifiers in the second and third memory layers are activated to amplify the differential signal between the BC and /BC broadcast buses. In this way, the data of the sense amplifier in the first memory layer are transferred to the sense amplifiers in the second and third memory layers.

Fig. 11(a) shows a chip photomicrograph of one memory layer fabricated using 1-μm CMOS technology. The chip size is 2 by 1.6 mm. We used 1-μm CMOS technology to perform all the fabrication processes for 3-D shared-memory test chip by ourselves in a clean room, since the advanced CMOS technology with buried interconnections was not commercially available. However, the transistor size is not always important in our shared memory because it is not necessary that a memory cell in the upper memory layer be directly connected to a memory cell in the lower memory layer. The three memory layers are

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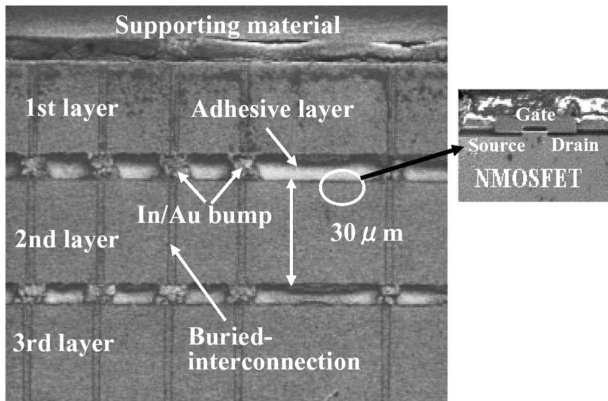
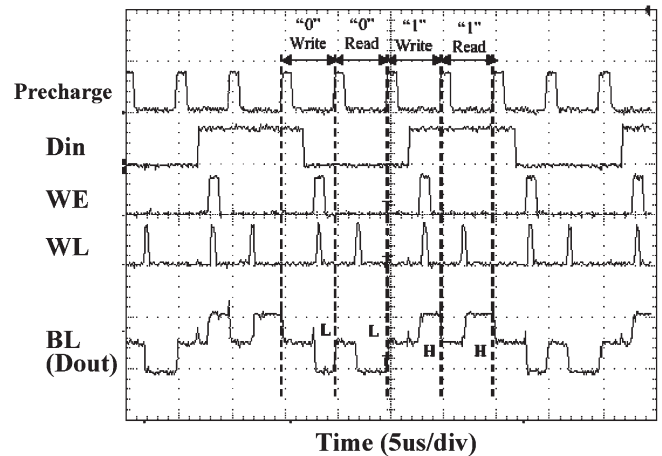


Fig. 12. SEM cross-sectional view of the 3-D shared-memory test chip with three stacked layers



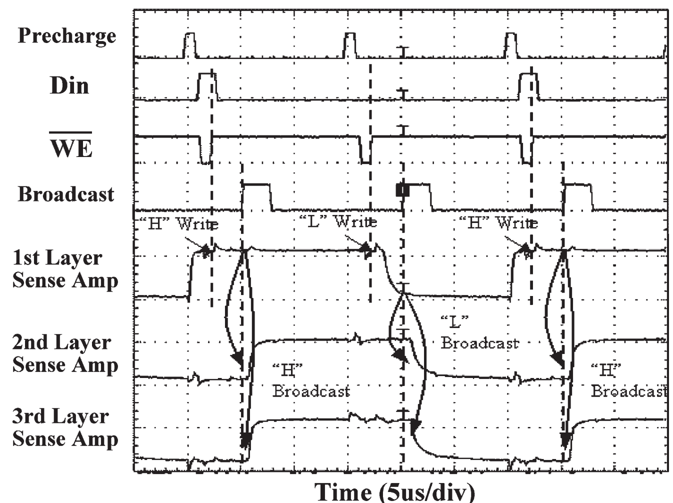


Fig. 13. Measured waveforms of the 3-D shared-memory test chip. (a) Waveforms for one memory layer. (b) Waveforms for the data transfer between three memory layers.

connected by the vertical buried interconnections through their respective sense amplifiers but not their respective memory cells. However, our 3-D integration technology is applicable to more advanced CMOS technology such as 90-nm technology node, since the 3-D integration does not compete with the scaling down of device size. We will be able to integrate 64 Mbit SRAM cells in each memory layer area of approximately 70 mm^2 in 3-D shared memory where approximately 6.0×10^4 buried interconnections with a 4-μm pitch are assigned to an area of 1 mm^2 if we employ the advanced CMOS technology with a 90-nm technology node. A magnified photomicrograph of the peripheral circuits including the sense amplifiers is shown in Fig. 11(b) where bundles of vertical buried interconnections with upper microbumps are clearly observable. Four buried interconnections are accommodated in one bundle. Fig. 12 shows the SEM cross section of a 3-D shared-memory test chip. It can be clearly observed in the figure that three memory layers are vertically stacked and connected by many vertical buried interconnections which act as broadcast buses. The silicon substrate thickness is approximately 30 μm, and the cross-sectional area of poly-Si buried interconnection is 2 by 12 μm. The size and thickness of the In/Au microbump is 5 by 5 μm and 2 μm, respectively. The cross-sectional view of the memory transistor is also visible in the magnified picture. The measured waveforms of the 3-D share memory test chip are shown in Fig. 13. Fig. 13(a) represents the waveforms measured in one memory layer. It is obvious from the figure that the read/write operations for both data "0" and "1" are successfully performed in the respective memory layers. Fig. 13(b) represents the measured waveforms for the broadcast data transfer between the three memory layers. In this experimental result, the data "1" and "0" are written into the memory cell and the sense amplifier in the first memory layer. Then, these data are transferred to the sense amplifiers and the memory cells in the second and third memory layers through the broadcast buses by applying the clock signal to the BC–TG terminals. It is clear from Fig. 13(b) that the broadcast operation is successfully performed between the three stacked memory layers through the buried interconnections, and consequently, the memory cells having an identical memory address in the three memory layers contain identical data. Thus, we were able to confirm the basic shared-memory operation in a 3-D shared-memory test chip fabricated using our 3-D integration technology based on the wafer bonding and thinning method.

VI. Conclusion

A 3-D integration technology based on the wafer bonding and thinning method has been described. Five key technologies for 3-D integration, namely, formation of buried interconnection, metal microbump formation, stacked wafer thinning, wafer alignment, and wafer bonding were developed. A new shared-memory test chip with three memory layers was fabricated using this 3-D integration technology. Fundamental memory operation and broadcast operation between the three memory layers were confirmed in this 3-D shared-memory test chip.

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Mitsumasa Koyanagi (M'86–SM'90–F'97) was born in Hokkaido, Japan, on February 4, 1947. He received the B.S. degree in electrical engineering from Muroran Institute of Technology, Japan, and the M.S. and Ph.D. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1969, 1971, and 1974, respectively.

In 1974, he joined the Central Research Laboratory, Hitachi, Ltd., where he worked on research and development of MOS memory device and process technology, and invented a stacked capacitor DRAM memory cell which has been widely used in the DRAM production. Stacked capacitor DRAM was the first commercialized 3-D LSI. He employed high-k materials in DRAM for the first time in 1978. In addition, he fabricated MOS transistors with shallow junction using laser-annealing technology for the first time in 1979. From 1980 to 1985, he worked with the Device Development Center, Hitachi, Ltd. In 1985, he joined the Xerox Palo Alto Research Center, California, where he worked on research and development of submicrometer CMOS devices, poly-silicon thin-film transistors, and the design of analog/digital LSIs. In 1988, he joined the Research Center for Integrated Systems, Hiroshima University, as a Professor, where he worked on scaled MOS devices, three-dimensional (3-D) integration technology, optical interconnection, and parallel computer system specific for scientific computation. In 1992, he fabricated the smallest MOS transistor with a gate length of 70 nm. He proposed 3-D integration technology based on wafer-to-wafer bonding for the first time in 1989. Since 1994, he has been a Professor with the Department of Machine Intelligence and Systems Engineering (currently the Department of Bioengineering and Robotics), Tohoku University, where his current research interests include nano-CMOS devices, memory devices, low-voltage and low-power integrated circuits, new intelligent memory for parallel processor systems, 3-D integration technology, optical interconnection, parallel computer system specific for scientific computation, real-time image processing systems and artificial retina chips, retinal prosthesis and brain implant devices, and brainlike computer systems. He has been researching 3-D integration technology and optical interconnection for more than 15 years.

Dr. Koyanagi was awarded the 2006 IEEE Jun-ichi Nishizawa Medal, the 1996 IEEE Cledo Brunetti Award, the 2001 Award of Ministry of Education, Culture, Sports, Science and Technology, the 1994 SSDM (Solid-State Devices and Materials) Award, the 2004 Optoelectronic Technology Achievement Award (Japan Society of Applied Physics), the 1990 Okouchi Prize, etc.

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Tomonori Nakamura was born in Shizuoka, Japan, on October 21, 1976. He received the B.S., M.S., and Ph.D. degrees in machine intelligence and systems engineering from Tohoku University, Sendai, Japan, in 1999, 2001, and 2004, respectively.

With Tohoku University, he was engaged in the research of three-dimensional integration technology.

Dr. Nakamura is a member of Japan Society of Applied Physics and Japan Society for Precision Engineering.

Yuusuke Yamada was born in Yamaguchi, Japan, on September 25, 1977. He received the B.S. and M.S. degrees in machine intelligence and systems engineering from Tohoku University, Sendai, Japan, in 2000, and 2002, respectively, where he is currently working toward the Ph.D. degree in machine intelligence and systems engineering.

Since 1999, he has been engaged in research of three-dimensional integration technology.

Mr. Yamada is a member of Japan Society of Applied Physics.

Hirokazu Kikuchi was born in Miyagi, Japan, on May 11, 1979. He received the B.S. degree in machine intelligence and systems engineering and the M.S. degree in bioengineering and robotics from Tohoku University, Sendai, Japan, in 2003 and 2005, respectively, where he is currently working toward the Ph.D. degree in bioengineering and robotics.

Since 2002, he has been engaged in research of three-dimensional integration technology.

Mr. Kikuchi is a member of Japan Society of Applied Physics.

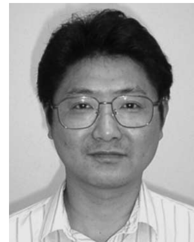
Takafumi Fukushima was born in Gunma, Japan, on February 6, 1976. He received the B.S., M.S., and Ph.D. degrees in synthetic chemistry from Yokohama National University, Yokohama, Japan, in 1998, 2000, and 2003, respectively.

From 2001 to 2003, he was a Technical Advisor with PI R&D Corporation in Yokohama, where he studied adhesives, interlayer dielectrics, electrodeposition, and photoresists based on soluble block-copolyimides. After that, he worked as a Postdoctoral Fellow with Venture Business Laboratory of Tohoku University, Sendai, Japan, where he is currently a Research Associate on many aspects of bioengineering and robotics including micro-TAS, optical interconnection, 3-D stacked LSI, and retinal prosthesis. His research interests include polymeric studies focusing on synthesis and characterization of high-performance heat-resistant polymers such as polyimides, BCB, and epoxy resins.

Tetsu Tanaka was born in Miyagi, Japan, on March 3, 1964. He received the B.S. and M.S. degrees in electronic engineering and the Ph.D. degree in machine intelligence and systems engineering from Tohoku University, Sendai, Japan, in 1987, 1990, and 2003, respectively.

In 1990, he joined Fujitsu Laboratories, Ltd., where he was engaged in the research and development of the scaled MOS devices including SOI devices. From 1994 to 1995, he was a Visiting Industrial Fellow with University of California, Berkeley. In 2005, he became an Associate Professor with Tohoku University. He is currently working on retinal prosthesis, brain implant devices, three-dimensional LSIs, nano-CMOS devices, nanodot memory, etc.

Dr. Tanaka is a member of the IEEE Electron Devices Society and the IEEE Solid-State Circuits Society.



Hiroyuki Kurino (M'99) was born in Gifu, Japan, on January 22, 1963. He received the B.S., M.S., and Ph.D. degrees in physics from Tohoku University, Sendai, Japan, in 1985, 1987, and 1990, respectively.

In 1990, he joined Texas Instruments Japan Ltd. From 1990 to 1993, he was a Visiting Researcher with the Research Center for Integrated Systems, Hiroshima University. In 1997, he was an Assistant Professor with Tohoku University. In 2000, he was a Visiting Assistant Professor with Johns Hopkins University. In 2001, he was an Associate Professor, and in 2005, he became a Professor with Tohoku University. His research interests include biologically inspired systems, three-dimensional LSIs, nanodevices, optical interconnection, etc.

Dr. Kurino is a member of Japan Society of Applied Physics and Japan Institute of Electronic Packaging. He was awarded the SSDM Young Researcher Award in 1992.

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