



Tunneling Through ultrathin GaAs n++-p++-n++ Barrier Grown by Molecular Layer Epitaxy

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Tunneling Through Ultrathin GaAs n⁺⁺-p⁺⁺-n⁺⁺ Barrier Grown by Molecular Layer Epitaxy

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Abstract—The I-V characteristics of ultrathin GaAs $n^{++}-p^{++}-n^{++}$ barrier structures with a 45 Å thick p^{++} layer grown by molecular layer epitaxy (MLE) have been measured at room temperature and 77 K. The tunneling probability for this structure has been calculated as a function of effective tunneling width. It was found that good agreement between experiment and calculation is obtained when the effective tunneling width is assumed to be 75 Å, which is much smaller than the depletion width about 190 Å measured by C-V method. This fact indicates that the depletion width approximation cannot be used to measure the exact tunneling width for ultrathin barrier devices.

Index Terms—Effective tunnelling width, molecular layer epitaxy, ultrathin barrier.

I. INTRODUCTION

Molecular layer epitaxy (MLE) [1] is a crystal growth method that is able to produce thin crystal films controlled with a single molecular layer precision. This method has been applied to preparation of ideal static induction transistor (ISIT) in which electrons transport in the crystal without collision [2]-[4]. The operation of the ISIT with tunneling has been reported [5]. The I-V characteristics of planar doped barrier (PDB) n⁺-i-p⁺-i-n⁺ structures with source-drain distances larger than 460 Å have been explained with thermionic emission theory at and above room temperature [6]-[8] and by tunneling theory at 77 K [9]. In the calculation of tunneling probability for PDB structures, the design source-drain distance was used as an effective tunneling width at zero bias because the depletion width measured by C-V method is almost equal to the design source-drain distance. However, discrepancies occur between the measured depletion width and the design source-drain distance with thinning of the sourcedrain distance. For example, the depletion width measured by C-Vmethod for a PDB structure with design source-drain distance 110 Å was about 320 Å [9].

In this work, we compare the measured and calculated I-V characteristics of the ultrathin $n^{++}-p^{++}-n^{++}$ structure with a 45 Å thick p^{++} layer grown by MLE. The tunneling probability and current for this structure are calculated by using triangular barrier model. The differences between the effective tunneling width and the depletion width measured by C-V method are simply discussed by considering the electron distribution tails from the n^{++} source and drain regions into the depleted channel region.

II. EXPERIMENTAL RESULTS AND DISCUSSION

The ultrathin GaAs $n^{++}-p^{++}-n^{++}$ barrier structure with a design metallurgical p^{++} layer thickness of 45 Å was grown by MLE,

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TABLE I Designed Layer Parameters in MLE

Source	n**	300Å	5×10 ¹⁹ cm ⁻³
Gate	p''	45Å	$9 \times 10^{19} \text{ cm}^{-3}$
Drain	n**	180Å	5×10 ¹⁹ cm ⁻³
Buffer	\mathbf{n}^{+}	425Å	5×10 ¹⁸ cm ⁻³
Substrate	\mathbf{n}^{+}	GaAs (100)	2×10 ¹⁸ cm ⁻³

using selenium and zinc as n^{++} and p^{++} dopants, respectively. After growth of the structure, the device mesa was etched with $H_2SO_4: H_2O_2: H_2O = 4:1:90$ solution. About 40 diodes with an area $S = 100 \times 100 \ \mu\text{m}^2$ were formed on a wafer. A lift-off Ti/Au metallization was used for nonalloyed contact to the top layer and Au/Ge was used for back contact. The design parameters in MLE are listed in Table I. The doping concentrations of both n^{++} layers are the same, $N_D = 5 \times 10^{19} \text{ cm}^{-3}$. The thickness $W_{p0} = 45$ Å and doping level $N_A = 9 \times 10^{19} \text{ cm}^{-3}$ of the p^{++} layer are designed so that the thin p^{++} layer is completely depleted. The doping levels of each layer have been determined by Hall effect with about 1500 Å thick layers and the thicknesses for each layer have been determined by the growth rate (Å/cycle) in the MLE [1]. The p^{++} and n^{++} doping profiles have been found to be nearly abrupt, by a dynamic SIMS instrument with depth resolution of 30 Å.

At thermal equilibrium, the relation of space charge neutrality $N_A \times W_{p0} = 2N_D \times W_{n0}$ should be valid, where W_{n0} is the depletion width on one side n^{++} region. The value of W_{n0} can be calculated to be 40.5 Å. Thus, the total depletion width is obtained as $W_0 = W_{p0} + 2W_{n0} = 126$ Å. The measured depletion width by C-V method is about 190 Å. The potential distribution at the thermal equilibrium can be calculated from Poisson equation, and the barrier height is obtained as $\Psi_{00} = 0.88$ V. This analysis is based on the depletion width approximation, which neglects the electron distribution tails from n^{++} regions into the depleted channel region.

The schematic diagram of the ultrathin $n^{++}-p^{++}-n^{++}$ barrier structure is presented in Fig. 1(a), where the black circles illustrate the electron distribution tails from both n^{++} regions into the depleted channel region. The potential distribution taking into account the electron distribution tails is calculated, and the zero bias barrier height is obtained as $\Phi_{00} = 0.91$ V. In this calculation, the electron distribution tails are expressed as $n(x) = N_D \exp[-q\Phi(x)/k_{\rm B}T]$, where $\Phi(x)$ is potential, q is elementary charge, $k_{\rm B}$ is Boltzmann constant, T is absolute temperature. Two dashed lines in Fig. 1(b) correspond to the calculated potential distributions at zero bias and $V_{DS} = 0.5$ V. It can be seen from these profiles that the position of potential maximum moves to the source direction with increasing bias (the substrate biased positively with respective to the top). Considering these factors, the triangular barrier model is adopted to simplify the calculation of tunneling probability for our structure. Two solid lines in Fig. 1(b) represent the triangular potential distribution at zero bias and $V_{DS} = 0.5$ V, where W_{gs} and W_{gd} are the effective source-gate and gate-drain distances, $W_{\rm eff 0}$ is the effective tunneling width at zero bias, a and b are the effective classical turning points, Φ_0 and Φ_1 are the effective barrier heights with respect to the source Fermi level E_{FS} at zero and V_{DS} biases, E_C is the energy at the bottom of conduction band, $V_{ns} = (E_{FS} - E_C)/q$ is degeneracy which is small [10], [11].

The tunneling current at zero absolute temperature is easily calculated by using this triangular potential barrier model, and can be expressed as [9]

$$I \approx S \cdot A' \cdot qV_{DS} \cdot (2qV_{ns} - qV_{DS})$$
$$\cdot \exp\left(-\alpha \cdot \sqrt{\Phi_1} \cdot W_{\text{eff}}\right) V_{DS} \leq V_{ns}$$
(1)

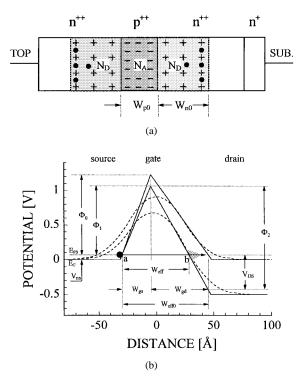


Fig. 1. (a) Schematic diagram of the ultrathin n⁺⁺-p⁺⁺-n⁺⁺ barrier structure. Black circles illustrate the electron distribution tails from both the n⁺⁺ regions into the depleted channel region. (b) Potential distributions from calculation (dashed lines) and triangular barrier model (solid lines) at zero bias and $V_{DS} = 0.5$ V. The parameters are assumed as $\Phi_0 = 1.15$ V, $W_{gs} = 25$ Å, $W_{gd} = 50$ Å, and $\mu_F^* = 3$.

$$I \approx S \cdot A' \cdot (qV_{ns})^2$$

$$\cdot \exp\left(-\alpha \cdot \sqrt{\Phi_1} \cdot W_{\text{eff}}\right) V_{DS} > V_{ns}$$
(2)

where S is device area, $A' \approx 2\pi m^* q/h^3 \approx 5.5 \times 10^8$ [A cm⁻² (eV)⁻²], $\alpha \approx 8\pi (2m^*q)^{0.5}/3h \approx 0.178$ [Å⁻¹ V^{-0.5}], m^* is effective mass of an electron, h is Planck constant. Φ_1 can be expressed as $\Phi_1 \approx \Phi_0 - V_{DS}/\mu_F^*$, where $\mu_F^* (\approx 1 + W_{gd}/W_{gs})$ is the intrinsic voltage amplification factor [2], [8]. $W_{\rm eff}$ can be expressed as $W_{\rm eff} \approx W_{gs} + W_{gd}/(1 + V_{DS}/\Phi_1)$ [9].

Fig. 2 shows the calculated tunneling current from (1) and (2) with the effective tunneling width $W_{\text{eff}\ 0}$ at zero bias as a single parameter. The other parameters qV_{ns} , μ_F^* and Φ_0 are fixed to 75 meV, 3 and 1.15 V, respectively. As mentioned before, the design metallurgical thickness of p⁺⁺ layer is 45 Å, the depletion width from the space charge neutrality is 126 Å, and is about 190 Å by C-V measurement. It is clear from Fig. 2 that the tunneling current magnitude and shape is very different as $W_{\text{eff}\ 0}$ changes from 45 to 195 Å.

Fig. 3 shows the calculated tunneling current from (1) and (2) with the zero bias barrier height Φ_0 as a parameter. The other parameters qV_{ns} , μ_F^* and $W_{\text{eff }0}$ are fixed to 75 meV, 3 and 75 Å, respectively. $\Phi_0 = 0.9$ V corresponds to the calculated barrier height at thermal equilibrium. The tunneling current does not strongly depend on the Φ_0 , as compared with $W_{\text{eff }0}$.

We have also calculated the tunneling current with μ_F^* ranging from 2–4, and qV_{ns} , Φ_0 , and $W_{\text{eff }0}$ are fixed to 75 meV, 1.15 V, and 75 Å, respectively. There are no pronounced changes in the calculated I-V characteristics.

Fig. 4 compares the calculated tunneling current from (1) and (2) and the experimental data at room temperature and 77 K. It is found that the best fit between the experimental data and calculated one is obtained when the parameters are assumed as $W_{\rm eff 0} = 75$ Å,

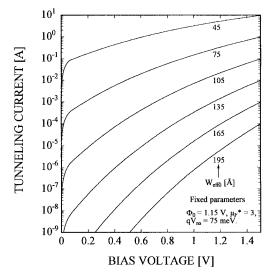


Fig. 2. Calculated tunneling current with the effective tunneling width at zero bias as a single parameter.

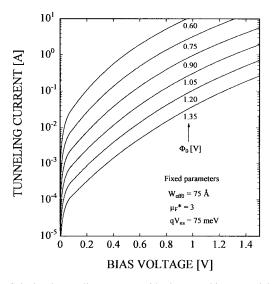


Fig. 3. Calculated tunneling current with the zero bias potential barrier height as a single parameter.

 $\Phi_0 = 1.15$ V, $qV_{ns} = 75$ meV, and $\mu_F^* = 3$. Although there are some differences in the potential distributions between the triangular barrier model and the calculated one, as solid lines and dashed lines in Fig. 1(b), the triangular barrier model explains our experimental data. The insert in Fig. 4 shows a logarithmic plot of the experimental and calculated I-V characteristics. The current in the vicinity of zero bias is approximately ohmic. This result is reasonable because the product of the $\Phi_1^{0.5} \times W_{\rm eff} \approx \Phi_0^{0.5} \times W_{\rm eff 0}$ is almost a constant for small bias ($V_{DS} < V_{ns}$), and the current should be determined by (1) with a nearly linear dependence on the bias voltage V_{DS} .

The parallel capacitance C_p and resistance R_p of our sample were measured at different frequencies using **hp**-impedance/gain-phase analyzer, and obtained as $C_p \approx 60$ pF and $R_p \approx 140 \Omega$. These values are independent of frequency up to 10 MHz. The estimated series resistance is about 1 Ω . The depletion width from the capacitance, 190 Å, is much larger than the effective tunneling width, 75 Å. Because of the electron distribution tails shown as black circles in Fig. 1(a), the classical abrupt space-charge edge approximation is not adequate

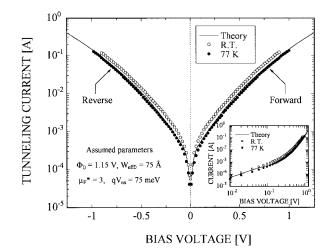


Fig. 4. Comparison between experiment and calculation at forward and reverse biases. The insert is a logarithmic I-V characteristics.

[12], [13], and the depletion width from the C-V data can not be referred to the blocking distance of electrons. Moreover, because the main contribution to the tunneling current is due to electrons with the energy near E_{FS} , the effective tunneling width should be smaller than the depletion width. However, for the PDB structures with a few hundred Angstrom long channels, this effect is not important and the design source-drain distance can be used as a tunneling barrier width [9]. The more precise expression of tunneling current with exact potential distribution requires further study.

III. CONCLUSION

The I-V characteristics for ultrathin GaAs $n^{++}-p^{++}-n^{++}$ barrier structures with a 45 Å thick p^{++} layer grown by molecular layer epitaxy (MLE) have been measured at room temperature and 77 K. The tunneling current for this structure has been calculated as a function of effective tunneling width. Good agreement between the experimental and calculated I-V characteristics is obtained when the effective tunneling width is assumed 75 Å, much smaller than the depletion width of about 190 Å measured by C-V method. The depletion width for ultrathin barrier devices. When the metallurgical source-drain distance is about 45 Å, the diode current is tunneling current even at room temperature.

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