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Local Electronic Function Shift in LSI Chips Stacked Three-Dimensionally by Area-Arrayed Bump Structures Caused by Local Deformation of the Laminated Chips

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Abstract

The clear periodic thermal deformation and thus, the periodic thermal residual stress distribution appears in each chip in three-dimensionally stacked chip structures due to the periodic alignment of metallic small bumps when the thickness of a chip is decreased to less than 200 μm. The estimated local deformation was validated by using a scanning blue laser microscope. It reached about 180 nm when the thickness of the stacked chip was 100 μm. The local distribution of the residual thermal stress was also measured by using stress-sensing test chips which consisted of about 1400 2-μm-long strain gauges. It was found that the residual stress varied from -200 MPa to +100 MPa depending on the position of the chip in the stacked structure and the layout of the small bumps. Finally electronic function shift of transistors formed near the strain gauges were measured between two bumps. For example, the amplitude of a periodic distribution of the function change of 90-nm-gate NMOS transistors between two bumps reached about 8%. Therefore, it is very important to minimize the local thermal deformation and residual stress of three-dimensionally stacked chips to assure the reliable electronic performance of products.

Introduction

So far, electronic products such as mobile phones and PCs have been miniaturized continuously and their functions have been improved drastically. Three dimensionally stacked structures such as multi-chip modules and multi-chip packages are indispensable for these products in order to increase the assembly density [1]. System in package (SiP) and chip on chip (CoC) of the multi chip structures have been already used in actual products. For example, the multi chip structure called MCL (Multi chip LSI) that was composed of the combination of a logic LSI chip and a memory chip has been employed in some products. In addition, the methods of the interconnection between an LSI chip and a substrate or another chip has been changed from a wire-bonding structure (WB) to a flip-chip structure (FC) for maximizing the interconnection density. The flip-chip technology using an area-arrayed solder bumps has been already employed in the MCL mentioned above. Since the total thickness of the stacked structure is strictly limited for mobile application, in particular, each chip has been thinned to less than 50 μm to minimize the total thickness of the modules or packages.

These flip-chip structures using area-arrayed tiny metallic bumps such as copper or solder are surrounded by insulating material (underfill) such as epoxy or plastic for assuring the reliability of the connection between an LSI chip and a substrate or another chip. The authors have already found that the distribution of the residual stress on a transistor formation surface of a chip was changed significantly by changing the interconnection structure of packages or modules from a wire-bonding structure to an area-arrayed flip-chip bonding structure. [2] In addition, a periodic stress with amplitude of more than 100 MPa appeared due to the periodic alignment of metallic bumps because of the mismatch in the material properties such as the coefficient of elasticity and the thermal expansion coefficient between metallic bumps and underfill material. [3] The periodic stress distribution was validated by the measurement using stress sensing chips with poly-crystalline-silicon-film gauges of 10 μm in length. In addition, the important structural factors that determine the distribution of the residual stress were found to be the thickness of a chip, the height and the width of a bump, the period of the bumps, and the thermal expansion coefficient of underfill material [4]. This high residual stress may give rise to disconnection of interconnections, chip-breaking and degradation of electronic performance of transistors. [5]-[7] For example, when a compressive stress is applied to a PMOS transistor perpendicularly to its channel, the transconductance (Gm) decreases by about 18% per 100 MPa. Therefore, it is very important to measure the local distribution of the residual stress or strain in three dimensionally stacked structures assembled by flip-chip technology for optimizing the structures and materials of packages and modules.

In this paper, therefore, the local distribution of the residual thermal stress was analyzed by using a finite element method to make clear the important structural factors that determine the local residual stress of the stacked chips. The estimated results of the local thermal deformation and the residual thermal stress were validated by using a laser microscope and small piezoresistive stress sensors. [8]-[12] We have successfully developed a piezoresistive stress sensor chip with 2-μm long gauges that consisted of single-crystalline silicon. The local distribution of the residual thermal stress on the active layers of each chip in two chip-stacked structures assembled by flip-chip technology was measured by using this sensor chip. Such local distribution of the residual stress caused the electronic function shift of transistors and capacitors. The maximum change rate of the variation of the transconductance of NMOS transistors between two bumps reached about 8%.

Analysis of the residual stress in chips stacked by area-arrayed bump structures by using a finite element method

Figure 1 shows an example of a finite element model for the stress analysis of two chip-stacked structures. The width of the substrate was assumed to be 6 mm. The thickness of the substrate was 1 mm. The thickness of each stacked chip was 100 μm. The width and the height of Cu bumps were fixed at

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100 μm, respectively and the pitch of the bump is assumed to be 200 μm. Two relative positions of bumps in the upper connection layer and the bottom connection layer were assumed. One is the same bump alignment model (Fig. (a)); the bumps in the upper layer exist at the same positions where the bumps in the bottom layer exit. The other model is called the alternative bump alignment model (Fig. (b)). In this model, the bumps in the upper layer are located at the same position where the underfill exists in the bottom layer. Assuming the symmetry of the total structure, the half of the total structure was modeled for the stress analysis. The total number of the nodes of the three dimensional model and elements were 27025 and 26640, respectively. The three-dimensional generalization plane strain model was used in this analysis. The materials constant used in this analysis is summarized in Table 1. Most materials were assumed to be elastic materials. Only Cu was modeled as elastic-plastic material. The yield stress of the Cu was assumed to be 300 MPa. The chip was mounted on an organic printed circuit board at 150°C. The maximum value and the maximum amplitude of the normal stress along x-(horizontal) direction near the interface between the Si chip and the bump layer are used for evaluation parameters of the shift of electronic functions of semiconductor devices.

The distribution of the normal stress along x-direction on a transistor formation surface of each chip of the two-chip-stacked model is shown in Figs. 2 and 3. Figure 2 is the estimated residual stress distribution in each chip analyzed using the same bump alignment model shown in Fig. 1(a). Figure 3 is the estimated result analyzed using the alternative bump alignment model shown in Fig. 1(b). In these analyses, both the width of each chip and the width and the height of Cu bumps were fixed at 100 μm, respectively and the pitch of the bump was assumed to be 200 μm. The clear periodic stress distribution appears in each chip due to the periodic alignment of metallic bumps. However, the maximum values of the residual stress in the two chips are quite different with each other when the stacked structure was analyzed by using the same-bump alignment model. The stress in the upper chip is about -150 MPa, and the residual stress in the bottom chip is about -170 MPa. Furthermore, the amplitude of the residual stress in the upper chip is about 100 MPa, while the amplitude of the residual stress in the bottom chip is about 40 MPa. The average residual stress in the stacked two chips differs with each other because of the difference of the distance from the bending neutral axis of the stacked structure. In addition, the amplitude of the residual stress of the bottom chip located in between the upper chip and the substrate is decreased drastically because the local deformation of the bottom chip is restricted strictly by bumps in the upper layer and the bottom layer.

On the other hand, it was found that the distribution of the residual stress in the bottom chip changes drastically depending on the relationship of the alignment of bumps between the upper layer and the bottom layer. Figure 3 summarizes the distribution of the residual stress in the two chips stacked using the alternative bump alignment structure.

Fig. 1 Finite element model for analysis of residual stress in Si chips mounted on a substrate by flip chip technology

Table 1 Materials constant for a finite element analysis

Material	Young's modulus (GPa)	Poisson's ratio	Thermal expansion coefficient (ppm/K)	Yield stress (MPa)
Si chip	130	0.28	2.3	-
Cu bump	130	0.34	16	300
Underfill	5	0.3	70	-

Fig. 2 Distribution of the normal stress along x-direction in each Si chip in the same bump alignment model

Fig. 3 Distribution of the normal stress along x-direction in each Si chip in the alternative bump alignment model

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The stress distribution of the upper chip does not change so much. However, the amplitude of the periodic stress of the bottom chip increases drastically and the value is almost the same as that of the upper chip. The reason for the difference of the average residual stress between the stacked two chips is the difference of the distance from the bending neutral axis of the stacked structure as was explained before. The maximum value of the residual stress in the bottom chip is about -210 MPa, and the amplitude of the residual stress in the bottom chip is about 120 MPa. The both values increase significantly comparing with the analytical result obtained from the same bump alignment model. Therefore, it is concluded that the residual stress in the upper chip does not depend on the structure of the bump alignment. However, the residual stress in the bottom chip changes drastically depending on the difference of the bump alignment position between the upper and bottom interconnection layers. The main reason for this bump alignment dependence of the residual stress is the constraint of the local deformation of the bottom chip. Though the local deformation of the chip stacked using the same bump alignment structure is strictly limited by the bumps in the upper and the bottom layers, the local deformation of the chip stacked in the alternative bump alignment structure is not restricted by bumps. According to these analysis results, it is concluded that it is very important to optimize the position (layout) of bumps to optimize the residual stress distribution in the stacked plural chips.

Detection of the estimated local deformation of the chips stacked by area-arrayed bump structures

The estimated local deformation of a Si chip in a flip chip bonding structures was validated using a scanning blue laser microscope and a white right interference microscope. The area-arrayed bump structures were made on a substrate that was made of a thermally oxidized single-crystalline Si wafer as shown in Fig. 4. The thickness of the wafer was 280 μm. The 200-μm square bumps were area-arrayed on the substrate by changing the intervals. The 75-μm thick and 10-mm square chips were mounted on the various substrates with different alignment of bumps at room temperature using conducting paste. The mounted system was heated at 150°C for curing the underfill. The residual surface deformation of the thinned chip was measured using both a scanning blue laser microscope and a white light interference microscope. The short coherence length of white light enables us to measure the surface displacement of the mounted chip with high resolution and wide range. It is possible to measure the deformation with vertical resolution of 0.1 nm and a maximum range of the vertical displacement of 100 μm. The horizontal resolution is 1.4 μm when using a 10x objective lens. Thus, this white light interference microscope can be applicable to measuring the displacement of a smooth surface. Fig. 5 shows the measured two-dimensional distribution of the local surface deformation of a Si chip mounted on the substrate shown in Fig. 4. In this sample, the regular pitch of the 200-μm wide Cu bumps was 400 μm. The amplitude of the measured surface deformation is indicated by color contours. Concentric local surface deformation of the Si chip clearly appears on the Cu bumps existing under the chip. The pitch of these concentric deformation patterns is same as the pitch of periodically aligned Cu bumps. Thus, this result clearly indicates that the local thermal deformation of a silicon chip appears between two bumps in the three-dimensionally stacked chip structure.

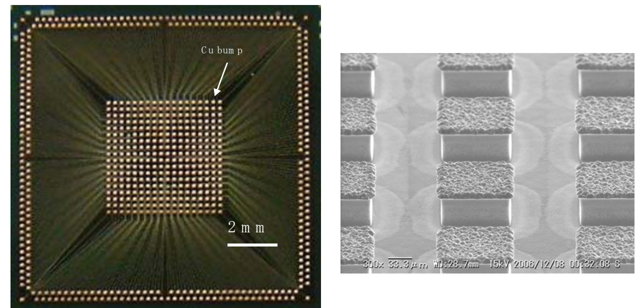

Fig. 4 Substrate for stacking test chips by using area-arrayed copper bump structures

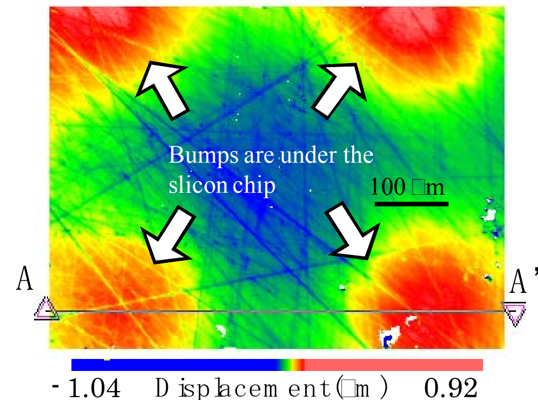

Fig. 5 Example of the local surface deformation of a silicon chip mounted by area-arrayed bump structure

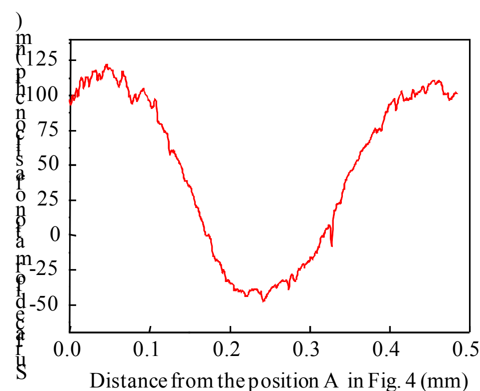

Fig. 6 Local surface deformation of a silicon chip along the line A-A' in Fig. 5

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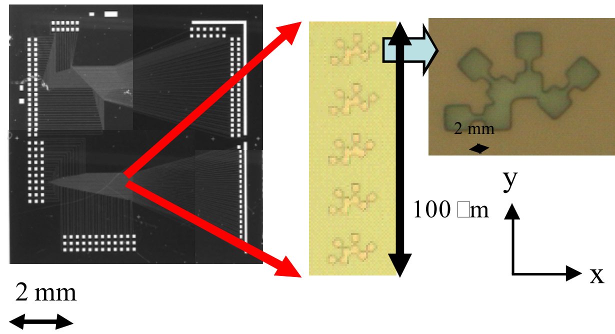

Fig. 7 Outlook of a sensor chip for measuring strain distribution in stacked chips

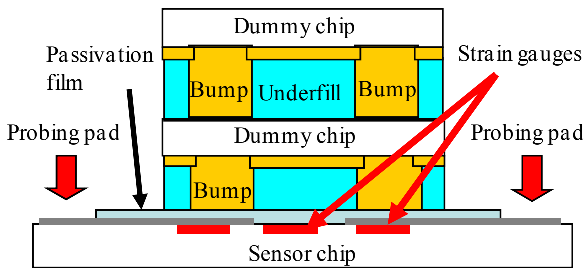

Fig. 8 Cross-section of test chip-stacked structure

The local residual deformation of the silicon chip along the A-A' line shown in Fig. 5 is summarized in Fig. 6. An symmetrical local deformation clearly appears on the surface of the silicon chip, and the amplitude of the local deformation is about 170 nm. Such local deformation should cause the local stress distribution in the silicon chip.

Local Residual Stress Measurement Using Stress-Sensing Test Chips

A Stress sensing chip was developed using single-crystalline silicon by applying the piezoresistive effect of silicon in order to validate the estimated stress distribution in the stacked two chips. Outlook of the stress sensing chip is shown in Fig. 7. A basic structure of the strain gauges is also shown in the figure. The length of each gauge is 2 μm. The width of the gauge is 0.5 μm. The sheet resistance of the diffused layer used for the strain gauges was controlled by ion implantation of phosphorus, and it was about 900 Ω/square. The average resistance of each gauge was about 4 kΩ. About 1420 gauges were formed on a 8 mm x 8 mm Si chip as shown in the figure. 20 gauges were formed between two bumps or under the bump. The sensitivity of the strain gauges was calibrated by applying four-point bending test of the test chip. This stress sensing chip was mounted by a flip-chip technology in the two chip stacked structure as shown in Fig. 8, and the local residual stress distribution of the stacked chip was measured by changing the relative positions of bumps in the upper and the lower interconnection layers. The estimated change of the stress distribution in the bottom chip was validated by this measurement.

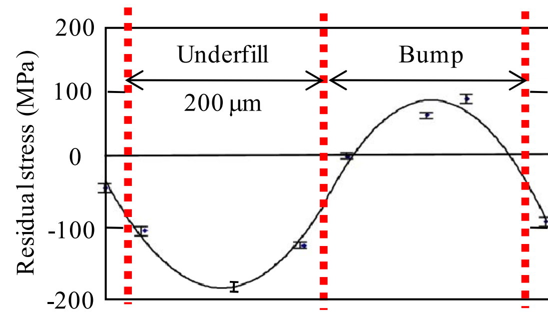

Fig. 9 Local distribution of the residual thermal stress on a surface of the sensor chip

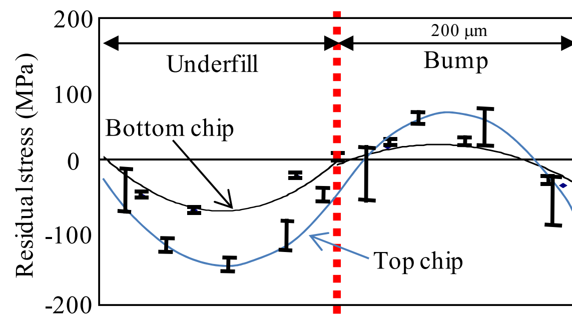

Fig. 10 Local distribution of residual thermal stress in two-chip-stacked structures

At first, the residual stress near an interface between the chip and the bump layer in one chip flip-chip structures was measured using this sensor chip. The sensor chip was bonded to the dummy chip at 200ºC for 30 minutes. During the bonding, compressive load of 20 N was applied. Figure 9 shows an example of the measured stress distribution between two bumps in the one chip-stacked structure. The periodic distribution of the residual thermal stress appeared clearly between two bumps. Compressive stress occurred in the area of the test chip on underfill, while tensile stress appeared where the chip was attached to bumps. This distribution was caused by the local deformation of the sensor chip as shown in Figs. 5 and 6, and this local deformation was caused by the difference in the thermal shrinkage between the underfill and the copper bumps. The estimated amplitude of the residual stress was about 300 MPa. This result clearly indicated that the periodic stress appeared in a silicon chip assembled by area-arrayed bump structure. This local stress distribution is caused by the difference of material properties such as the coefficient of elasticity and the thermal expansion coefficient among metallic bumps, underfill and silicon.

Next, the residual thermal stress was measured in two chip-stacked structures. Figure 10 shows an example of the local distribution of the residual thermal stress in chips between two bumps in the stacked structure. The periodic stress distribution also appeared in both chips this two-chip stacked structure. The average residual stress in the top chip was about -50 MPa, while it was about -10 MPa in the bottom chip. The amplitude of the residual stress in the top chip was about 230 MPa and it was about 3 times higher than that in the bottom chip. This difference was due to the structure of

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the bump alignment as was shown in Fig. 2. However, the shape of the distribution is not symmetrical. The main reason for the asymmetry was random plastic deformation of copper bumps during mounting process. Therefore, this result clearly validated that the periodic stress distribution appears in the three-dimensional chip stacking structures due to the mismatch of the mechanical properties between underfill material and bump material. Such local distribution of the residual stress in the stacked chips causes the local distribution of the change of the electronic performance of devices because the residual stress changes the electronic band structure of not only semiconductor materials but also dielectric materials.

Change of the Electronic Characteristics of Transistors and Capacitors due to the Local Residual Stress in the Stacked Chips

Since the electronic band structure of semiconductor and dielectric materials changes seriously due to the deformation of crystallographic structures of the materials, electronic performance of devices varies depending on the residual stress in a silicon chip. The piezoresistance effect is one of the simple examples of the strain-dependent change of the electronic characteristics of devices. However, the quantitative prediction of the change in actual products is very hard because of the fluctuation and variation of material properties and structures of packaging materials, and manufacturing conditions. Therefore, it is very important to evaluate the stress dependence of the electronic characteristics of important devices.

In this study, the stress dependence of two key components, 90-nm node NMOS transistors and MOS capacitors using high-k material, were measured by applying four-point bending test as shown in Fig. 11. Uniform uni-axial strain was applied to thin strips cut from a silicon wafer on which the transistors and capacitors were fabricated. An example change of the I-V characteristics of an NMOS transistor is shown in Fig. 12. In this experiment, the source-drain voltage was fixed at 0.5 V and the applied uni-axial tensile stress was varied from 0 MPa to 150 MPa. The drain current increased monotonically with the increase of the tensile strain. The increase rate of the transconductance of this transistor was about 10%/100-MPa. The threshold voltage did not change substantially during this experiment. Considering the experimental result of Fig. 9, for example, the local distribution of the transconductance of an NMOS transistor should appear between two bumps in the chip mounted on a substrate by area-arrayed small bumps. The estimated amplitude of the variation reaches about 30%. Such variation may deteriorate the reliability of products seriously. This stress sensitivity, however, is a strong function of the structure of each transistor, such as the thickness of the chip, the width of a gate, materials of the gate, and the concentration of dopant in the source and drain of the transistor. It is very important, therefore, to minimize the amplitude of the distribution of the change of the residual stress in LSI chips.

A similar phenomenon was observed when uni-axial stress was applied to MOS capacitors. The dielectric constant of the oxide film k is a function of band gap of the oxide, and it is expressed as follows.

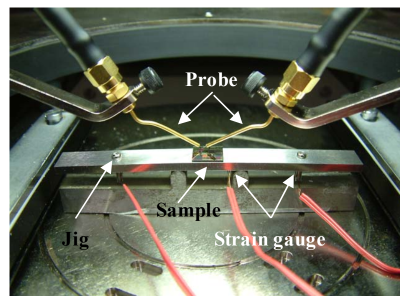

Fig. 11 Application of uni-axial strain to a test chip by four-point bending method

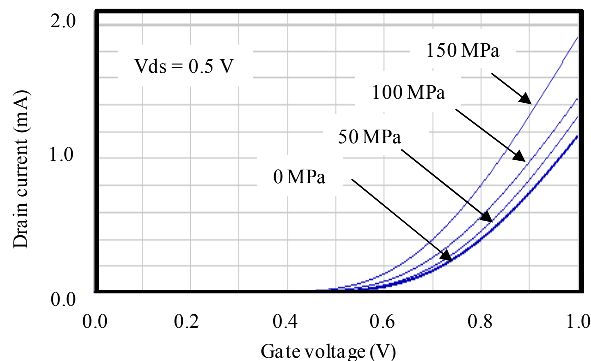

Fig. 12 Change of I-V characteristic of an NMOS transistor under uni-axial tensile stress applied parallel to its channel

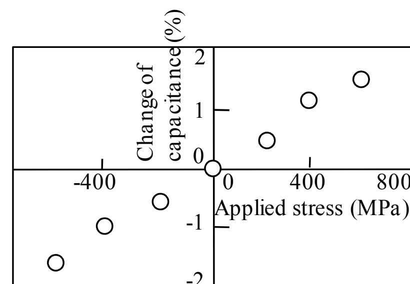

Fig. 13 Change of capacitance of a MOS capacitor under uni-axial tensile stress applied parallel to its channel

$$k = k_0\{1 + 4\pi ne/m^*Eg^2\} \quad (1)$$

Here, k_0 is constant, n is the density of molecules, e is the element charge of an electron, m* is the effective mass of an electron, and Eg is the band gap of the material. Since both the effective mass of electron and the band gap of the material are a function of stress, the capacitance of the thin-film capacitor changes depending on the amplitude of the applied stress. The stress dependence of MOS capacitors is shown in Fig. 13. The capacitance of the capacitors increased monotonically with the increase of the applied tensile stress. The increase rate was about 0.3%/100-MPa. The change rate is rather small comparing with the rate of the transconductance of the NMOS transistor.

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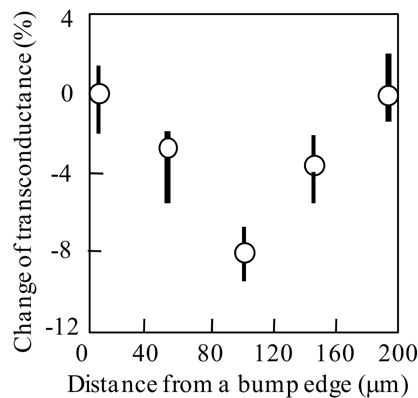

Fig. 14 Change rate of transconductance of NMOS transistors after mounting a test chip on a substrate by area-arrayed copper bumps

Finally, the change of the transconductance of the NMOS transistors was validated using the assembly structure of silicon chips using area-arrayed small bumps shown in Figs. 4 and 8. An example of the measured distribution of the change between two bumps is shown in Fig. 14. Since a silicon chip between the bumps deformed concavely due to thermal shrinkage of underfill, compressive stress occurs in this area. Thus, the transconductance of the NMOS transistors decreased due to the assembly. The maximum change rate was about 8%. Such a change may deteriorate the electronic performance of products. Therefore, such a local distribution of the residual stress should be minimized by optimizing the structure of the stacked structure.

Conclusions

A finite element analysis was performed to make clear the local distribution of the residual stress in stacked chips mounted by flip chip technology using area-arrayed metallic bumps quantitatively. The average residual stress in the stacked two chips changes depending on the distance from the bending neutral axis of the stacked structure. The local residual stress also varies depending on the relative position of bumps between the upper interconnection layer and the bottom interconnection layer. The estimated local deformation of silicon chips and the residual stress distribution in the stacked two chips were validated in detail by the experiment using a laser microscope and the stress-sensing chips with 2-μm long strain gauges consisted of single-crystalline Si. The amplitude of the local deformation reached about 180 nm and such local deformation caused the variation of the residual stress of about 300 MPa. Since the electronic performance of transistors and capacitors varies depending on the mechanical stress, such local distribution of the residual stress causes the distribution of the performance seriously.

It is concluded, therefore, that it is very important to optimize not only the thickness of a chip and the period of bumps, but also the relative position (layout) of bumps between the upper and the lower interconnection layers in order to optimize the residual stress distribution in the stacked plural chips.

Acknowledgments

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