A Matched Expansion MEMS Probe Card with Low CTE LTCC Substrate

doi: 10.1109/TEST.2007.4437618

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Abstract

This paper describes the fabrication technology of a new MEMS-based probe card. The probe card is designed to satisfy requirements from advanced wafer-level burn-in LSI tests. The problem of thermal expansion mismatch between the probe card and LSI wafers is solved by using a LTCC (low temperature cofired ceramics) substrate with a coefficient of thermal expansion of 3.4 ppm/°C. The probes are first formed on a silicon wafer, and then transferred to the LTCC substrate using Au/Sn solder bumps. The prototyped probe card was preliminarily evaluated in contact resistance. The measured contact resistance was 0.14 Ω during 2500 touchdowns.

1. Introduction

A probe card is an array of probes, which mechanically and electrically contact the bond pads of LSI under test to select known good dyes (KGD). A new probe card has been developed for high temperature wafer-level burn-in test by matching thermal expansion between the probe card and the wafer under test.

For wafer-level burn-in test, several features are required to the probe card. First, electrical contacts must be established simultaneously between several thousands of pads on DUT (device under the test) and the probe pins. Silicon wafers to be tested have warp due to residual stress generated during the fabrication process. Therefore, the probe pins must absorb a height difference of each pad on the wafer, which is usually several tens micrometers.

Second, the probe pins must achieve low contact resistance below 0.5 Ω. To establish low electrical resistance contacts to the pads on DUT, the probe pin must scrub the surface of the pads and break thin oxide layers. For this scrubbing action, the shape of the probe pins looks like a slantwise curve, which creates horizontal overdrive displacement when a vertical overdrive was applied. Furthermore, each probe pin should provide a sufficient contact force over 1 gf.

Third, the probe card must have a similar CTE (coefficient of thermal expansion) to silicon. During a burn-in test, a silicon wafer is heated up to 150 °C, and thermal expansion mismatch between a probe card and a silicon wafer results in unacceptable dimension error of the probe pins from the pads on DUT. This deviation becomes over 70 μm for 300 mm wafers, if the CTE of probe card is 7.1 ppm/°C, which is a typical value for a HTCC (high temperature cofired ceramic) substrate. This is larger than the minimum pitch of the bond pads of DRAM [1]. This thermal expansion mismatch problem makes conventional probe cards with a HTCC substrate inapplicable to wafer-level burn-in tests. Thus, we developed a new probe card on a special LTCC (low temperature cofired ceramic) substrate with a CTE of 3.4 ppm/°C, which is close to that of silicon. Thus, misregistration between the probe pins and the bond pads on DUT due to thermal expansion does not occur even in wafer-level burn-in tests.

Figure 1 illustrates the structure of the probe card developed in this study. The probe has a metal pyramidal contactor, whose sharp tip scratches oxide films on aluminum bond pads and lowers contact force to bond pads. The contactor is supported by a slantwise cantilever to absorb the height deviation of the bond pads up to 100 μm, which is caused by wafer bending in fabrication and high temperature testing.

The probes are attached on the LTCC substrate with a CTE of 3.4 ppm/°C using Au_{80}/Sn_{20} eutectic solder. The LTCC substrate must be thick enough to withstand the total contact forces, which are 10–100 kgf when 10000 probe pins are on the substrate.

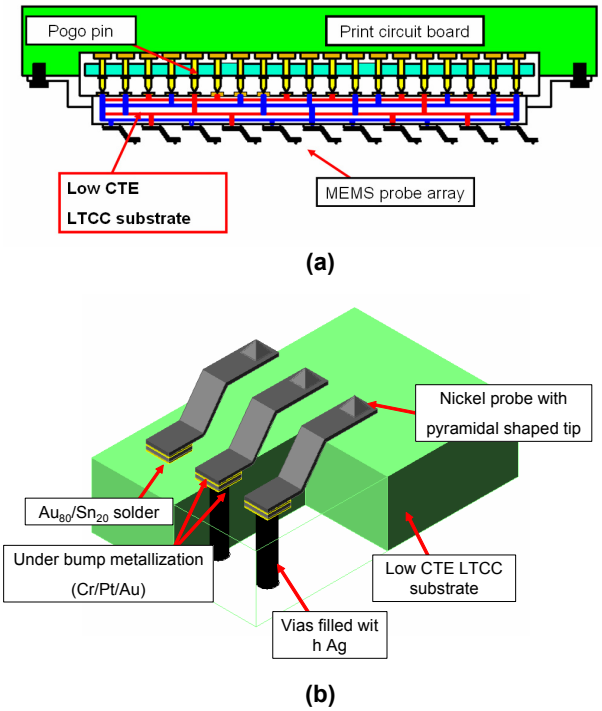

Figure 1. (a) Schematic structure of a MEMS-based probe card with a low CTE LTCC substrate. (b) Structure of probes transferred onto a LTCC substrate by Au/Sn eutectic bonding.

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The Au/Sn solder is selected, because the probe card operates in harsh environments with periodic thermal and mechanical stresses. The LTCC substrate is also called as a space transformer, because it has multilayer electrical lines, which expand probe pitches of 50–500 µm to more than 1 mm for the connection to a printed circuit board (PCB) through pogo pins. The pogo pins enable stable electrical connections by absorbing the thermal and mechanical deformation of the LTCC substrate and the PCB.

2. Design

2.1 Low CTE LTCC Substrate

Thermal expansion is a significant problem for wafer-level burn-in tests, as shown in Fig. 2. An alumina-based multilayer ceramic substrate used for conventional probe cards has a CTE of 7.1 ppm/°C. For example, the periphery of a 300 mm silicon wafer expands by 57 µm from the center when the temperature changes from 25 °C to 150 °C, while the thermal expansion of the alumina substrate reaches 130 µm under the same condition. Therefore, the dimension error becomes 130 – 57 = 73 µm, which is larger than the minimum pitch of the bond pads of DRAM.

Figure 3 shows the HTCC and low CTE LTCC substrate for probe card. The HTCC substrate was fabricated by NTK Technical Ceramics, and is being provided to Formfactor, Inc., which is the top share holder in probe card market. The low CTE LTCC substrate was specially prepared for this work by Nikko Company, Electro-Ceramic Division.

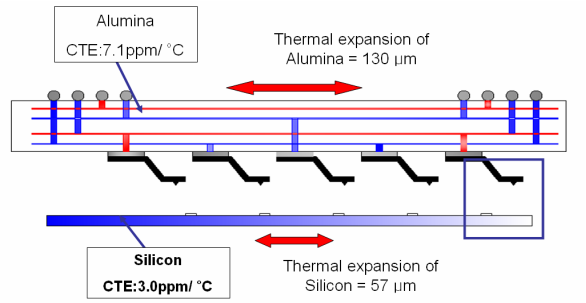
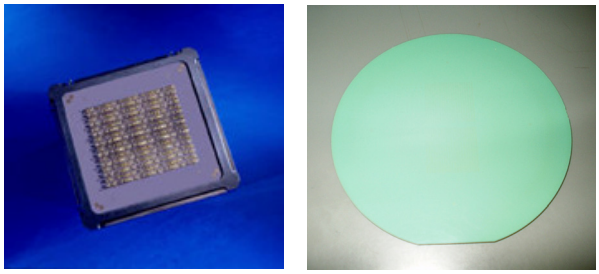


Figure 2. Thermal expansion mismatch between the probe card with a HTCC substrate and silicon wafer



(a) (b)

Figure 3. (a) HTCC and (b) low CTE LTCC substrate for probe cards ((a) Courtesy of NTK Technical Ceramics)

Table 1 compares three kinds of ceramic substrate [2]. The LTCC substrate can use Cu or Ag as a conductor material, which is not possible to be used in the HTCC substrate, because a cofiring temperature of HTCC is higher than the melting point of Cu or Ag. Therefore, the HTCC substrate must alternatively use W or Mo as a conductor material, which has a larger resistivity than Cu and Ag. The CTE of LTCC is smaller than that of HTCC, however, it is still much higher than that of silicon. Our low CTE LTCC substrate is based on cordierite and glass with an optimized mixture ratio for the required CTE of 3.4 ppm//°C, and uses Ag as a conductor material.

Table 1. Comparison of ceramic properties [2]

	HTCC (Alumina)	LTCC	Low CTE LTCC
CTE [ppm/°C]	7.1	5.0	3.4
Conductor	W/Mo	Cu	Cu/Ag
CTE match with DUT	Bad	Fair	Good

2.2 Predictive Contact Resistance of Probe Pin

One of the most important requirements of a probe card is its low contact resistance. Holm's theory on contact resistance between two metals could predict the contact resistance [3]. The contact resistance between the bond pad and the probe tip is comprised of a constriction resistance and an interfacial thin film resistance, as shown in Fig. 4.

During wafer test, a current flow between the probe tip and the bond pad is constricted to the narrow inter-metallic contacts. Distortion in the current flow causes increase in the constriction resistance. The contribution of the thin film resistance depends on the thickness of the oxide films on bond pads.

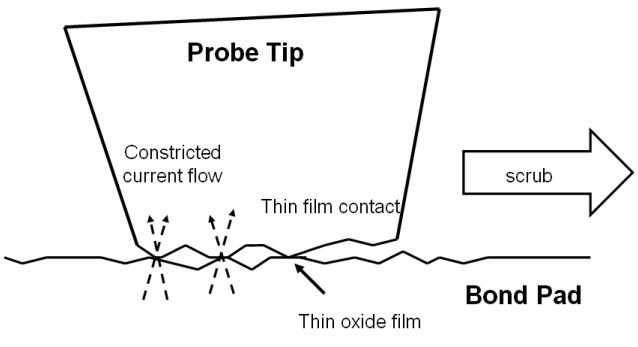


Figure 4. Contact resistance between a probe tip and a wafer [3]

The total contact resistance R_c can be expressed with hardness and some electrical properties of contact materials, as

$$R_C = \frac{\rho_1 + \rho_2}{4}\sqrt{\frac{\pi H}{F}} + \frac{\sigma_f H}{F} \quad (1)$$

ρ : electrical conductivity
H : hardness
σ_f : tunnel resistvity of thin film
F : contact force

In Eq. (1), the first term represents constriction resistance and the second term represents thin film resistance. With known material properties, the contact resistance can be predicted with a function of contact force. Figure 5 shows the predicted contact resistance between a Ni probe tip and bond pads made or Au or Ni.

As found in Fig. 5, contact force over 1 gf is required to make low contact resistance below 0.5 Ω. This information is important for designing a MEMS-based probe card, which generally has low rigidity. If the rigidity of the probe is not enough to produce 1 gf contact force, the contact resistance will be much higher than expected. Table 3 summarizes the detailed design specifications of the probe card.

Table 2. Schematics of material properties [3]

Material	H	ρ	σ_f
	10^8 N/m^2	10^{-8} Ωm	10^{-12} Ωm^2
Al (Pad)	2.4	2.8	25
Au (Pad)	3	2.2	1
Ni (Probe)	14	9	2 ~ 8

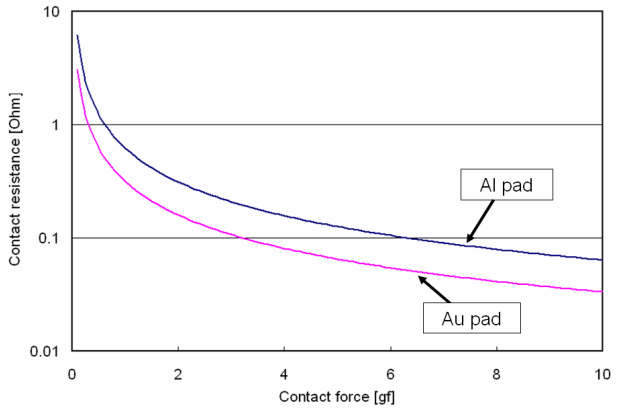


Figure 5. Predicted contact resistance between a probe tip and pads: To make low contact resistance (< 0.5 Ω), the probe must provide contact force larger than 1 gf.

Table 3. Design specifications of the probe card

Item	Parameter	Specification
Probe pin	Material	Nickel
	Overdrive	10~100 μm
	Stiffness	Each probe pin should generate contact force of 1 gf ~10 gf when 100 μm overdrive is applied.
	Spring constant	> 1000 N/m
	Pitch	100 μm
	Number of probes	1000 ~ 10000
	Contact resistance	< 0.5 Ω
	Tip shape	Pyramid shaped sharp tip
	Life time	> 10^6 touchdowns
Substrate	Material	Low CTE LTCC
	Load capacity	10 ~ 100 kgf
	CTE	3.4 ppm/°C
	Size	Φ 100 mm

3. Fabrication

Figure 6 shows the fabrication process. Nickel probes are first fabricated on a silicon wafer, and then transferred to the LTCC substrate. This transfer technology is one of key fabrication technologies for the probe card. Au/Sn eutectic solder paste is patterned on the LTCC substrate by screen printing, and then reflowed. This is used to bond the probes on a silicon wafer to the LTCC substrate, and then the silicon wafer is lost away. The detail is described below.

Another key fabrication technology is photolithography on an etched substrate. To form the slantwise cantilevers shown in Fig. 1(b), a silicon wafer is first wet-etched by KOH, and the probe structures are fabricated in these etched trenches by photoresist spray coating or ultra-thick photoresist casting in conjunction with projection exposure.

The process starts with a 4 inch (100) silicon wafer (Fig. 6 (a)). First, thermal oxidation is performed, and then TMAH wet etching follows to make trenches with a depth of 100 μm (b). After that, a thermal oxide layer is grown again (c). To make the molds of the pyramidal contactors on the bottom of the etched trenches, KOH etching is performed again (d). The spray coating of photoresist is used to make the mask pattern on the bottom of the etched trenches.

After removing the thermal oxide by buffered HF (e), 100-

nm-thick Ti is sputter-deposited on the silicon substrate (f). This Ti layer is used as a seed layer for the following Ni electroplating. After that, ultra-thick photoresist (THB-

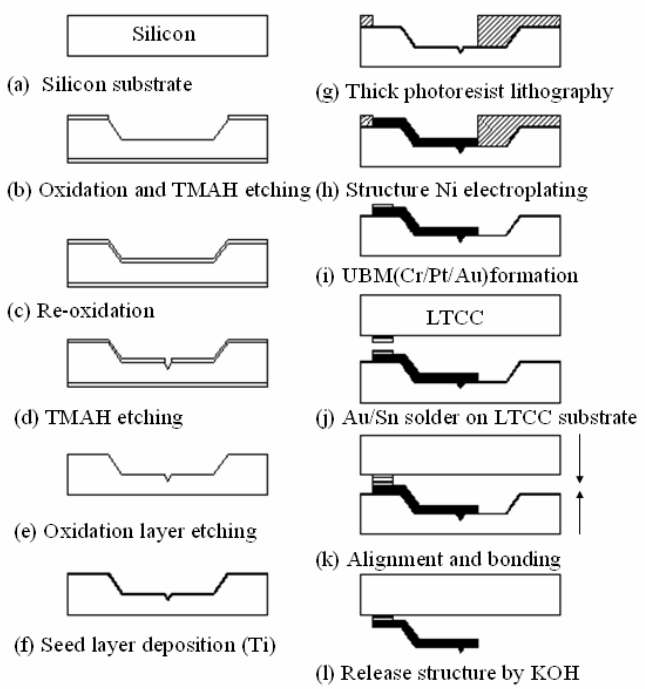


Figure 6. Fabrication process of the probe card

151N, JSR Corp.) is spin-deposited on the silicon substrate (g). The photoresist fills the etched trenches of 100 μm depth. In this process, special care to avoid any bubbles in the photoresist must be taken. In the previous study, we used XP KMPR-1050 (Kayaku MicroChem Corp.), which is a new type of SU-8, for this process, but stripping the photoresist was difficult [4]. THB-151N is easy to be stripped using the stripper, but inferior in resolution to XP KMPR-1050. By using the thick photoresist layer as a mold, Ni is electroplated with a thickness of 10 μm (i).

After stripping the photoresist, an UBM (under bump metallization) layer is formed on the Ni structures. The UBM layer is Cr (100 nm)/Pt (100 nm)/Au (100 nm) triple layer (j), in which Cr is an adhesion layer, Pt is a diffusion barrier, and Au is an anti-oxidation layer. The UBM layer is patterned by lift-off technique. Spray coating of photoresist on (111) surface is again used in this step. On the UBM layer on the LTCC substrate, Au/Sn solder bumps with a height of 20 μm are formed by screen-printing and reflowing (k).

The completed silicon substrate and the LTCC substrate are aligned and bonded together (l). The bonding process is accomplished in vacuum, applying 800 N forces on the substrates at 400 °C for 1 hour. After the bonding, the silicon substrate is etched away by 40 wt% KOH solution (m). KOH is selected for this process, because it attacks only Si and Ti but not Ni and Au/Sn alloy.

Bonding process was the critical to successful fabrication of a probe card. Note that there is a very steep liquidus lines on both sides of the eutectic melting point, as shown in Fig. 7. This indicates that enriching the composition by one percent of gold leads to an approximate 30 °C increase in the melting temperature. Thus, it is very important to control the weight percent ratio of Au/Sn precisely[6].

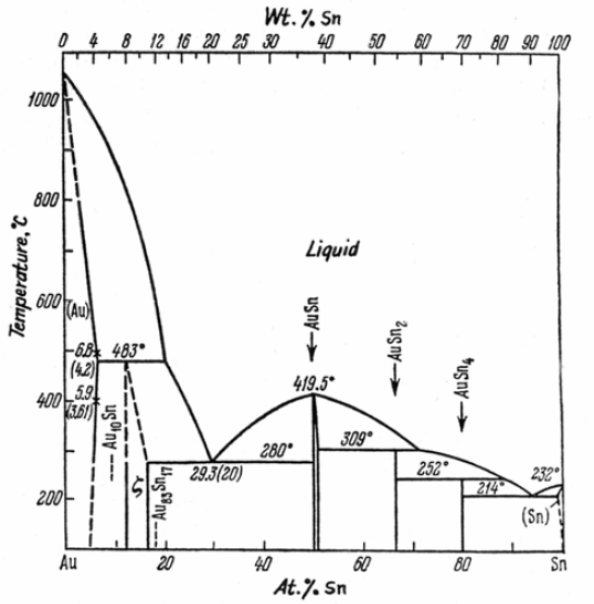


Figure 7. Phase diagram of Au/Sn alloy (Source [5])

Figure 8 is the photographs of the fabricated probe card. 1600 probes are arrayed in an area of 43 mm × 20 mm on the LTCC substrate. The width and length of each probe is 90 μm and 267 μm, respectively, and the pitch is 500 μm, which is much larger than requirements from current LSI testing, e.g. 80 μm for DRAM. The way to reduce the pitch is discussed in Section 5.

As shown in Fig. 8, the probes and the bond pads are misaligned. The misalignment error is 40 μm in row and 130 μm in column. The misalignment occurred in the bonding process (Fig. 6 (k)), in which bonding pressure was applied through the Au/Sn solder bumps in melting. This problem will be solved by self-alignment using the surface tension force of the melted solder or controlled collapse of the solder bumps.

Another problem found in the fabrication is low yield of the probes, which was only 20 % in the first prototype. 80% of the probes were broken in the last process, where silicon was etched by KOH to release the probes. A lot of bubbles were formed during the etching process, and these bubbles intended to lift up the silicon substrate from the LTCC substrate. The probes could be broken by this force before silicon was totally etched. To solve this problem, silicon dry etching was used instead of wet etching in the second prototype. Reactive ion etching (RIE) using SF_6 removed the silicon substrate with sufficient selectivity to other materials. As a result, the yield was improved to nearly 100 %.

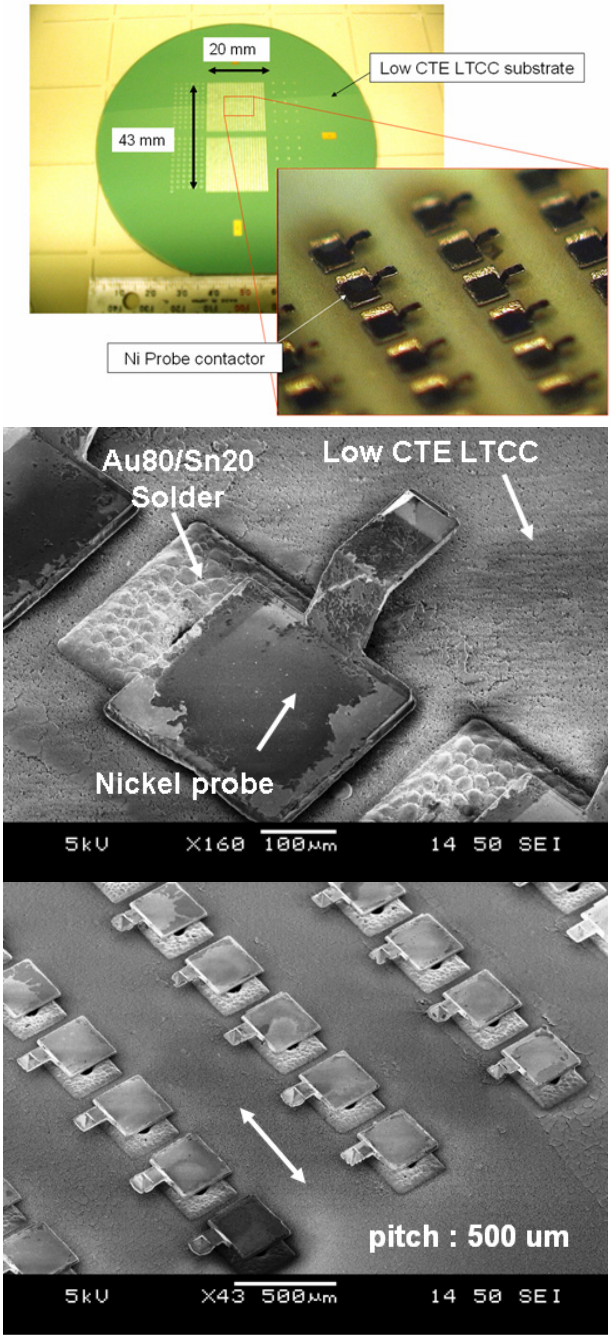


Figure 8. Fabricated probe card with a Low CTE LTCC substrate

4. Measurement

To measure the contact resistance of the probes, a probe card test systems shown in Fig. 9 was developed. The contact resistance was measured by recording voltage between two adjoining probes contacting a Au/Cr layer on a glass wafer at a constant current of 200 mA, as shown in Fig. 9 (b) [7]. The overdrive distance, that is, the vertical deformation of the probes was 50 μm, from which the contact force is calculated to be 1.5 gf. The wafer was kept at room temperature.

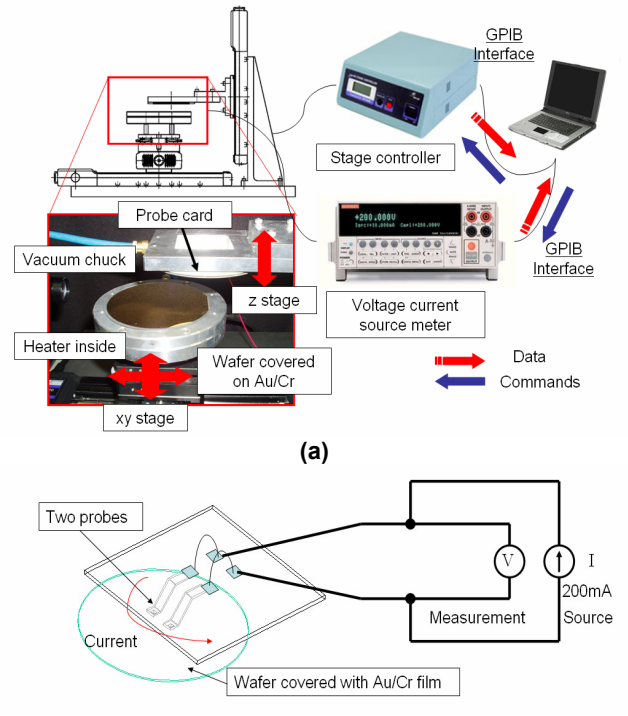


Figure 9. Contact resistance measurement setup

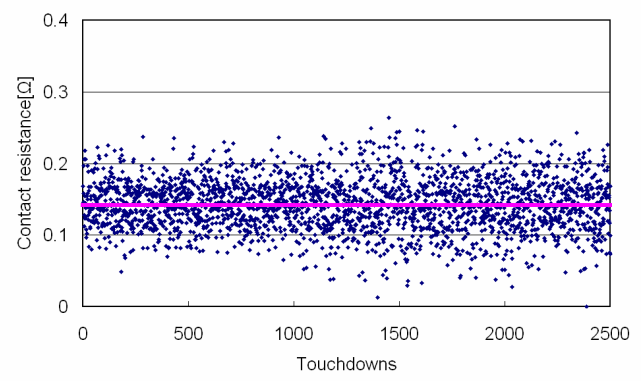


Figure 10. Measured contact resistance of the probe during 2500 touchdowns

The change of the contact resistance of one probe during 2500 touchdowns is shown in Fig. 10. The average contact resistance is a half of the resistance between two probes after subtracting parasitic resistances (0.04 Ω) from the measured values. The contact resistance was 0.14 Ω throughout the measurement. This value satisfies the industrial standard of probe cards, which is lower than 0.5 Ω. The life time of the probe card, which is expected to be more than 10^6 touchdowns, will be measured using the identical setup.

5. Discussion

The pitch of the fabricated probe card was 500 μm. However, this pitch is much larger than that of the pads on state-of-the-art memory devices. ITRS 2006 (International Technology Roadmap for Semiconductors) expects that

the bond pad pitch of memory devices will shrink to 40 μm in 2010.

The bottleneck process which decides the probe pitch is ultra thick photoresist patterning process (Fig. 6 (g)). In this process, we used THB-151N ultra-thick photoresist. However, the maximum resolution of photoresist is only 50 μm when the thickness is 100 μm. Therefore, the available minimum pitch is only 100 μm with the photoresist. This is far from the target in ITSRS roadmap. To realize finer pitch patterns, we can adopt an alternative process.

Instead of using the ultra-thick photoresist, we can use spray-coated photoresist as a mold pattern. The required thickness of mold is over 20 μm, because the thickness of probe pin required for sufficient contact force over 1 gf is 15 μm. In this method, we can use a variety of photoresists, which have better resolution than THB-151N.

In the exposure of the spray-coated photoresist in deeply-etched trenches, polarized illumination is effective to improve the resolution [4]. Figure 11 shows scanning electron micrographs (SEM) of photoresist patterns on (111) Si surfaces in etched trenches. We demonstrated that TM-polarized illumination can produce line-and-space patterns with a width of 20/20 μm on the (111) surface. This suggests that that probes with a pitch of 40 μm can be fabricated using this method.

6. Conclusions

A MEMS-based probe card formed on a LTCC substrate with a CTE of 3.4 ppm/°C, which is close to that of silicon was developed for wafer-level burn-in LSI tests. The metal probes were first fabricated on a wet-etched silicon substrate by photoresist spray coating and ultra-thick photoresist casting in conjunction with projection exposure. The probes were then transferred to the LTCC substrate using Au/Sn solder bumps, and finally the silicon substrate was etched away by KOH or SF_6 dry etching.

The fabricated probe card was preliminary evaluated in contact resistance. The measured contact resistance is 0.14 Ω in average, satisfying the industrial requirement. However, the pitch of the probes in this prototype is 500 μm, which is much larger than the industrial requirement. A method to reduce the pitch to 40 μm, which meets ITRS roadmap, was proposed with the experimental results of fine patterning in deeply-etched trenches.

Acknowledgement

This work was supported by a Grant-in-Aid for Scientific Research from Sendai-City Intelligent Cooperative Link of Unique Science and Technology for Economy Revitalization.

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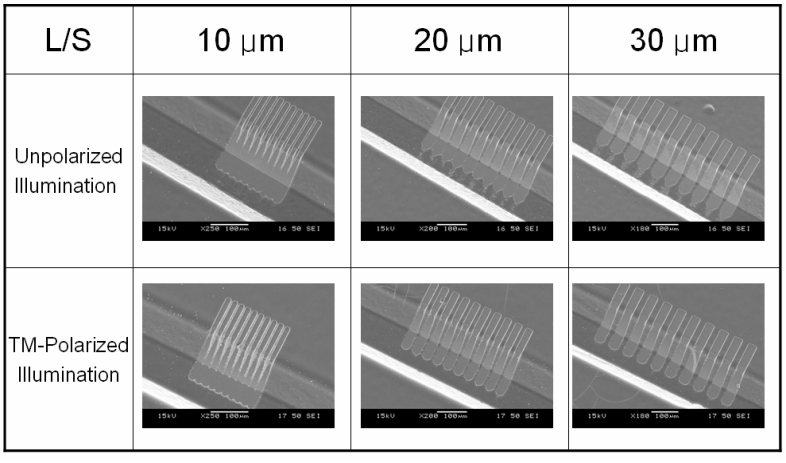

Figure 11. Resolution enhancement of patterns on spray-coated photoresist by polarized Illumination