東北大学機関リポジトリ
TOUR
Tohoku University Repository

# New Three-Dimensional Integration Technology Using Self-Assembly Technique



| | |
|---|---|
| 著者 | 福島 誉史 |
| journal or publication title | IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest |
| volume | 2005 |
| page range | 348-351 |
| year | 2005 |
| URL | http://hdl.handle.net/10097/46417 |



doi: 10.1109/IEDM.2005.1609347

# New Three-Dimensional Integration Technology Using Self-Assembly Technique

Takafumi Fukushima, Yusuke Yamada, Hirokazu Kikuchi, and Mitsumasa Koyanagi

Department of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University
6-6-01 Aza Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan.
Phone: +81-22-795-6906; Fax: +81-22-795-6907; E-mail: sdlab@sd.mech.tohoku.ac.jp

**Abstract**

To achieve ultimate super chip integration, we have developed a new three-dimensional integration technology called Super-Smart-Stack technology using a novel self-assembly technique. The chip alignment accuracy of within 1μm is obtained by the self-assembly technique. We demonstrated for the first time that 3D SRAM test chip with ten memory layers was successfully fabricated using the Super-Smart-Stack (SSS) technology.

## Introduction

Three-dimensional (3D) integration is the most promising technology to achieve a future advanced LSI since not only the packing density can be increased by vertically stacking several chips but also the performance can be improved and the power consumption can be reduced by decreasing the number of long interconnections. The long interconnections cause the serious degradation of LSI performance and the significant increase of power consumption whereas a number of short vertical interconnections make it easy to perform the parallel processing. So far we have developed 3D integration technology based on wafer-to-wafer bonding method and fabricated several 3D LSI prototype chips such as 3D image sensor chip, 3D shared memory, 3D artificial retina chip and 3D microprocessor chip[1-12]. However, such a wafer level 3D integration technology is applicable only for stacking of LSI wafers with high production yield since the overall yield for 3D chips is given by multiplying the respective wafer yield by the number of times corresponding to the number of stacked layers. Therefore, in order to dramatically improve the overall yield for 3D LSI, it is preferable to stack the known good dies (KGDs). 3D integration technology based on chip-to-chip bonding method makes it possible to stack KGDs. However, chip-to-chip bonding method is not always useful because the fabrication throughput is very low. Then, in this work, we propose a new 3D integration technology to vertically stack a number of KGDs in batch where many KGDs are temporarily glued to a wafer using the self-assembly technique and this wafer is stacked on another wafer with many KGDs. This new 3D integration technology using the self-assembly technique enables us to stack various kinds of chips with different chip size and chip thickness which are fabricated using different process technologies. Therefore, this technology is the ultimate integration technology.

## Concept of Super-Smart-Stack Technology

We call this ultimate 3D integration technology a Super-Smart-Stack (SSS) technology. Figure 1 describes the concept of Super-Smart-Stack technology. After wafer probing and dicing, known good dies (KGDs) for the first layer of 3D LSIs are aligned and bonded to the chips on LSI wafer using a self-assembly technique. In this case, LSI wafer acts as a thick supporting wafer as well. KGDs for the second layer are aligned and temporarily glued to a thick handling wafer again using a self-assembly technique. After that, these KGDs temporarily glued to the handling wafer are bonded to KGDs on the supporting LSI wafer and then the handling wafer is removed. By repeating this sequence, we can obtain a new 3D LSI called a super chip as shown in Fig.2. The most striking feature of this super chip is that various kinds of thin chips with different sizes such as MEMS chip, sensor chip, CMOS RF-IC, MMIC, power IC, control IC, analog LSI, and logic LSI are vertically stacked. Thus, Super-Smart-Stack technology can provide new advanced LSIs with small form factor, high packing density, high performance, low power consumption, and new functionality.

## Fabrication and Evaluation of Multiple Stacked 3D LSI

Figure 3 shows a cross-sectional view of 3D LSI fabricated by Super-Smart-Stack technology. The fabrication process sequence for Super-Smart-Stack technology is schematically shown in Fig.4. First, the deep trenches for buried interconnections are formed through the thick interlayer dielectrics into Si substrate by using RIE (Reactive Ion Etching) and filled with conductive materials such as polycrystalline Si (poly-Si), W or Cu after the formation of dielectric layer onto the trench surface (Fig.4(b)). These KGDs with buried interconnections for the first chip layer are bonded onto the supporting LSI wafer after alignment using a self-assembly technique and the adhesive is injected underneath the KGDs (Figs.4(c) and (d)). Then, KGDs are thinned from the backside by the mechanical grinding and chemical mechanical polishing (CMP) to expose the bottom of buried interconnections after coating a high-viscosity resin with low coefficient of thermal expansion (CTE) and the metal microbumps are formed onto the bottom of buried interconnections (Figs.4(e)-(g)). Next, the KGDs with buried interconnections for the second chip layer are flip-chip-bonded onto the KGDs for the first chip layer again using a self-assembly technique (Fig.4(h)). By repeating

0-7803-9269-8/05/$20.00 (c) 2005 IEEE
Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on February 28,2010 at 21:56:44 EST from IEEE Xplore. Restrictions apply.

these sequences, we can obtain 3D LSI chips with several chip layers (Fig.4(i)). We have developed several key technologies of buried interconnection formation, chip alignment and bonding by self-assembly technique, adhesive injection, chip thinning and planarization for Super-Smart-Stack technology. Figure 5 shows SEM cross-sectional view of deep trench for buried interconnection which is formed using ICP (Inductive Coupling Plasma) etching with $SF_6/C_4F_8$ source gases. It is clear in the figure that the deep trenches with small taper are formed without any undercut underneath the thick oxide. These trenches were filled with low resistive $n^+$ poly-Si (0.4 mΩ-cm) or W in this work. Figure 6 shows that test chips with In-Au microbumps and $n^+$ poly-Si buried interconnections are flip-chip-bonded onto a supporting Si wafer with the chip spacing of 180μm after aligning. The size and thickness of test chips are 7mm x 7mm and 280μm. The depth and diameter of deep trench for buried interconnection are 60μm and 3μm (top) and 2μm (bottom), respectively. The self-assembly technique was used for chip alignment and bonding. Figure 7 demonstrates the experimental results for the self-assembly technique in which the plateaus with rectangular shape and hydrophilic surface are formed on a supporting wafer surface and the test chips with hydrophilic surface are aligned and eventually bonded onto the plateaus on the supporting wafer (Fig.7(a)). In this experiment, a liquid was dropped onto the plateau on the supporting wafer and the test chip was placed with face-down on this plateau and precisely aligned by using surface tension of liquid and bonded after 0.06sec. (Fig.7(b)). The alignment tolerance is plotted versus the liquid concentration and the liquid volume in Fig.8. A very high alignment accuracy of within ±1μm is obtained in the condition of 0.2μL in liquid volume and 1% in liquid concentration (Fig.7(c)). The experimental results of adhesive injection are shown in Fig.9 where a quartz glass chip is used instead of Si chip to observe the adhesive injected underneath the chip. A very narrow gap of 3 to 5 μm between the quartz glass chip and the supporting wafer was completely filled with the low-viscosity epoxy adhesive at 1.55 min. after the injection started as clearly shown in Fig.9(c). The test chips with the buried interconnections bonded onto the supporting wafer were thinned from the backside by the mechanical grinding and CMP. Before these thinning processes, a high-viscosity resin was coated on the test chips to prevent the generation of their edge-chipping. However, the resin coating causes a serious wafer warpage. Then, we carefully examined the materials and the composition of heat-curable and UV-curable resins. As shown in Fig.10, a small wafer warpage was consequently achieved by using the heat-curable resin with fillers that gives rise to a low CTE. Photomicrographs of test chips before and after thinning are shown in Fig.11(a). The test chips are precisely aligned onto the supporting wafer using the self-assembly technique. After thinning the test chips down to 30μm, the bottom of buried interconnections with rectangular cross-section are clearly observed in the magnified SEM micrograph in Fig.11(a). Figure 11(b) shows the photomicrograph of test chip array after forming In-Au microbumps on the bottom of the buried interconnections using a lift-off technique. After the formation of In-Au microbumps, the second layer of test chips with different sizes (5mm x 5mm, 6mm x 6mm) were bonded onto the first layer of test chips with size of 7mm x 7mm as shown in Figs.12(a) and (b). Figure 12(c) shows the photomicrograph of the second layer chip array after coating with low-CTE resin. By repeating this sequence, three-layer stacked test chips with three kinds of chip sizes were successfully fabricated as shown in Fig.13. Figure 14 shows an SEM cross-sectional view of three-layer stacked structure with different chip thickness of 35μm, 7μm and 31μm. We have also succeeded in fabricating 3D memory test chip with ten layers using our Super-Smart-Stack technology based on self-assembly technique as shown in Fig.15. We confirmed the basic operation of this 3D memory test chip as shown in Fig.16 where the simultaneous data transfer among three memory layers through the buried interconnections is demonstrated.

## Conclusions

We have developed a new three-dimensional (3D) integration technology called Super-Smart-Stack technology using a novel self-assembly technique that allows us to stack various kinds of KGDs with different chip size and chip thickness which are fabricated using different technologies. We demonstrated that the chip alignment accuracy of within ±1μm is obtained by the self-assembly technique. Furthermore, 3D SRAM test chip with ten memory layers was successfully fabricated using the Super-Smart-Stack technology.

## References


(1) H. Takata, M. Koyanagi, International Semiconductor Device Research Symposium, 327-330 (1991).
(2) T. Matsumoto, M. Koyanagi *et al.,* SSDM (International Conf. on Solid State Devices and Materials), 1073-1074 (1995).
(3) T. Matsumoto, M. Koyanagi *et al.,* SSDM (International Conf. on Solid State Devices and Materials), 460-461 (1997).
(4) M. Koyanagi *et al.,* IEEE MICRO, 18 (4), 17-22 (1998).
(5) H. Kurino, M. Koyanagi *et al.,* IEDM, 879-882 (1999).
(6) K. W. Lee, M. Koyanagi *et al.,* IEDM, 165-168 (2000).
(7) M. Koyanagi *et al.,* ISSCC, 270-271 (2001).
(8) H. Kurino, M. Koyanagi *et al.*, IEICE Trans. on Electronics, E84-C (12), 1717-1722 (2001).
(9) T. Ono, M. Koyanagi *et al.,* IEEE COOL Chips, 186-193 (2002).
(10) T. Sugimura, M. Koyanagi *et al.*, IEEE International Conf. on Field- Programmable Technology (ICFPT), 372-374 (2003).
(11) J. Deguchi, M. Koyanagi *et al.,* Jpn. J.A.P., 1685-1689 (2004).
(12) T. Fukushima, M. Koyanagi *et al*., SSDM (International Conf. on Solid State Devices and Materials) 64-65 (2005).


Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on February 28,2010 at 21:56:44 EST from IEEE Xplore. Restrictions apply.

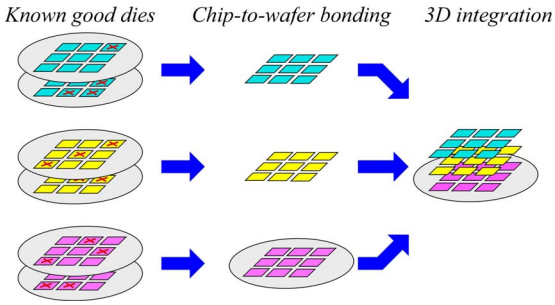


Fig.1 3D LSI fabrication by Super-Smart-Stack technology.

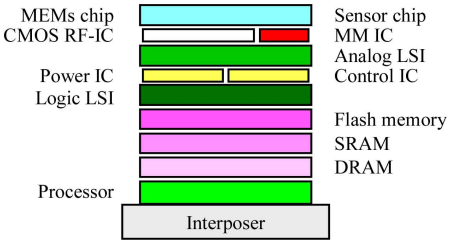


Fig.2 Conceptual structure of 3D super chip.

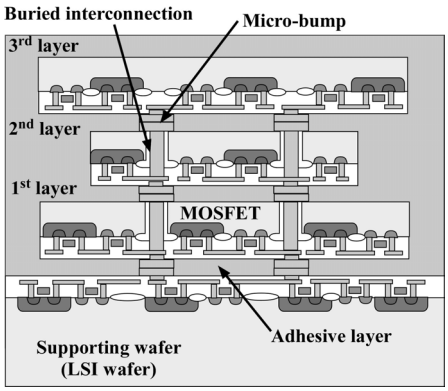


Fig.3 Cross-sectional structure of 3D LSI.

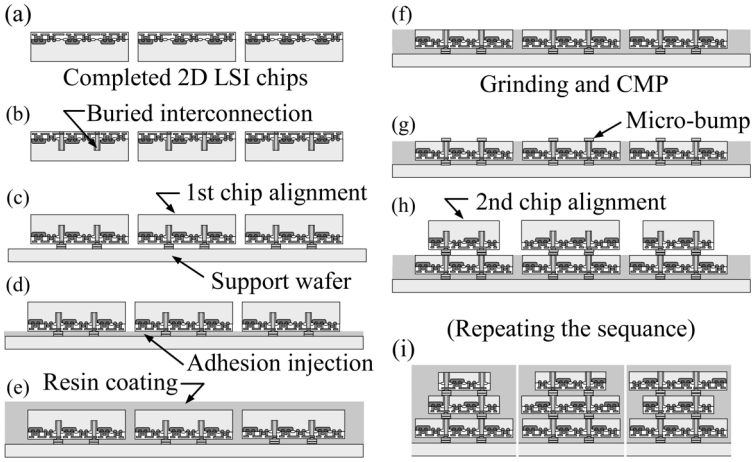


Fig.4 Fabrication process sequence for Super-Smart-Stack technology.

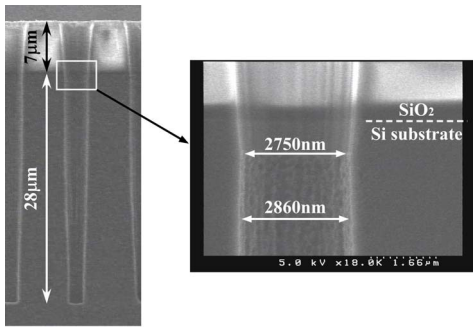


Fig.5 SEM cross-sectional view of trench formed through thick $SiO_2$ layer into Si substrate in a Si chip.

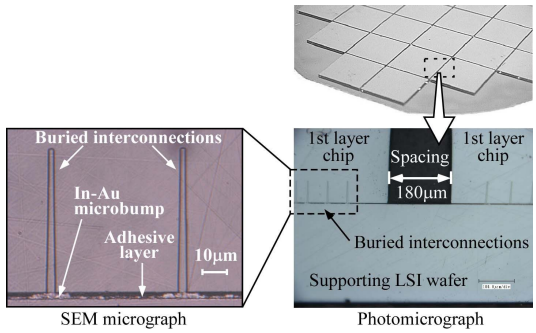


Fig.6 Cross-sectional view of test chips for the first layer bonded onto supporting wafer using self-assembly technique.

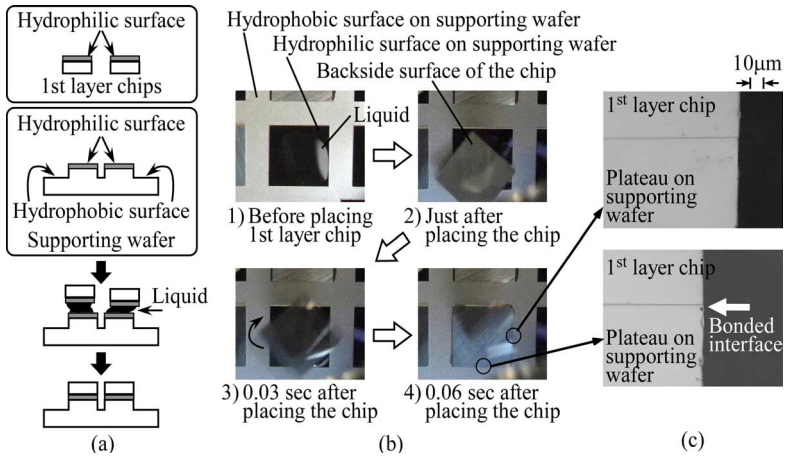


Fig.7 Self-assembly technique using surface tension of liquid (a), photographs for self-assembly events from a video (b), and SEM cross-sectional view of 1st layer chip bonded onto the plateau on supporting wafer (c).

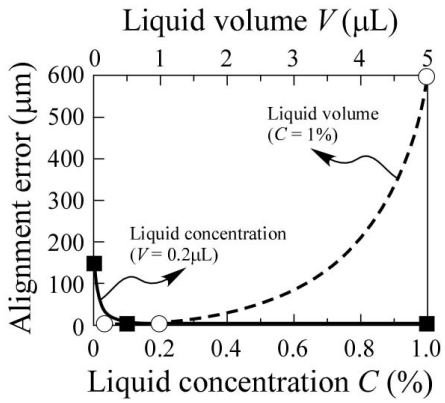


Fig.8 Dependence of alignment tolerance on liquid concentration and volume.

Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on February 28,2010 at 21:56:44 EST from IEEE Xplore. Restrictions apply.

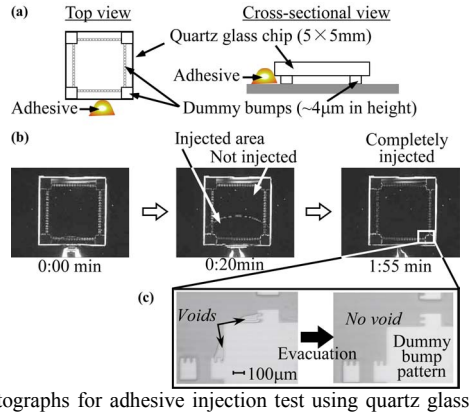


Fig.9 Photographs for adhesive injection test using quartz glass chip with injection time and magnified photomicrographs before and after evacuation in the adhesive injection process.

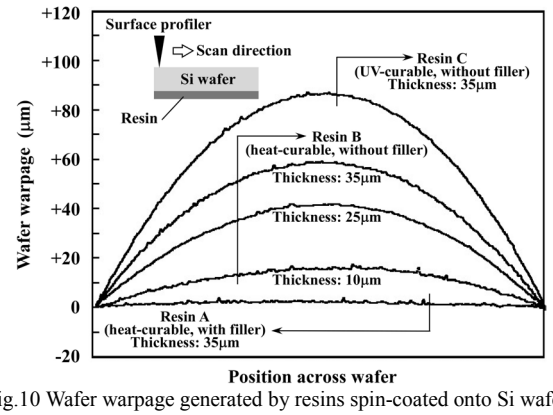


Fig.10 Wafer warpage generated by resins spin-coated onto Si wafer.

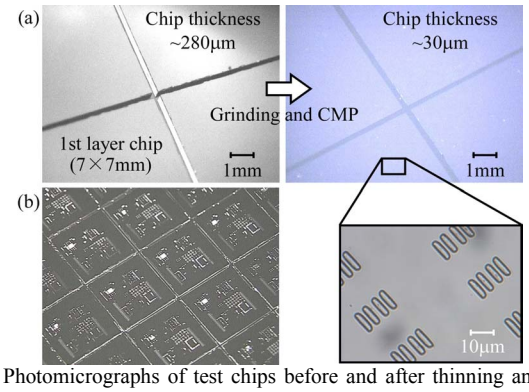


Fig11 Photomicrographs of test chips before and after thinning and SEM micrograph of the backside surface of the first layer chip after thinning (a) and SEM micrograph of test chip array after forming In-Au microbumps (b).

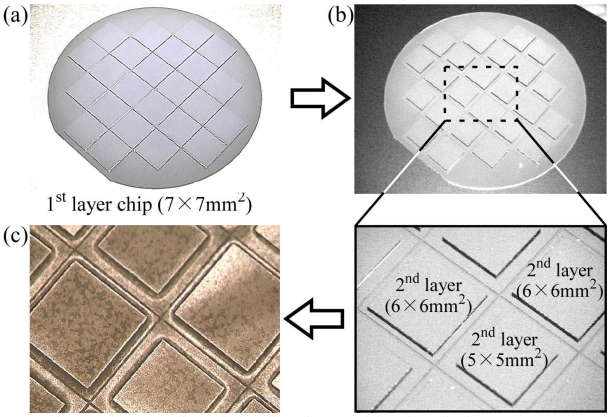


Fig.12 Photomicrographs of the first layer chips bonded onto a supporting wafer (a), the second layer chips with different size bonded onto the first layer chips (b), and the second layer chips coated with low-CTE resin (c).

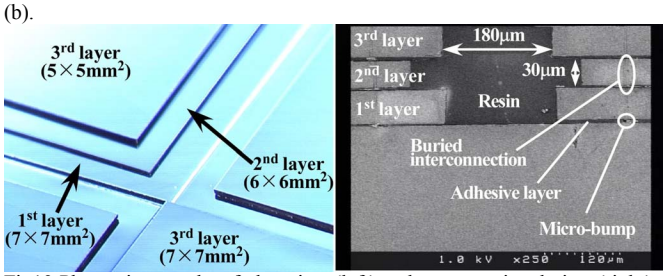


Fig13 Photomicrographs of plan view (left) and cross-sectional view (right) of three-layer stacked test chips with different chip sizes.

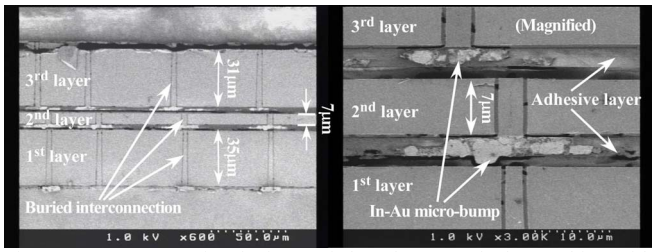


Fig14 SEM cross-sectional views of three-layer stacked test chips with different chip thickness.

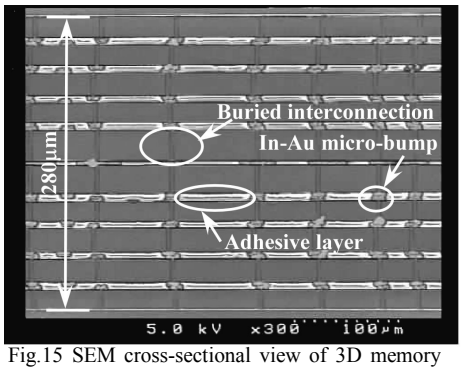


Fig.15 SEM cross-sectional view of 3D memory test chip with ten memory layers using Super-Smart-Stack technology.

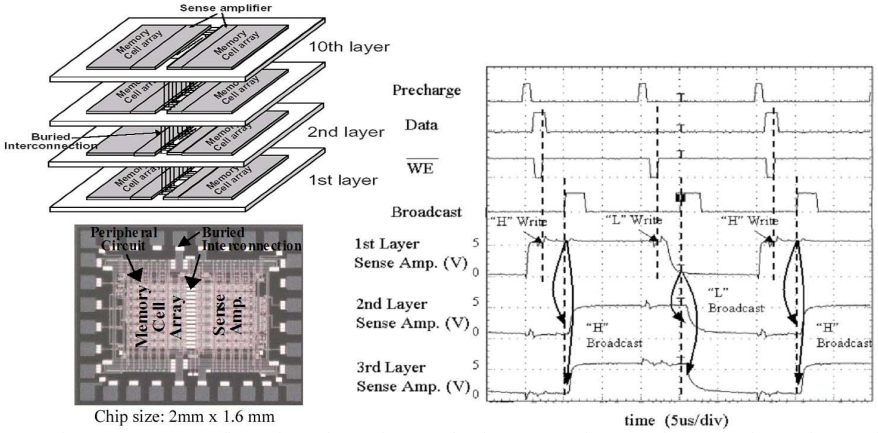


Fig.16 Memory configuration, photomicrograph of a memory layer, and measured waveforms of 3D SRAM fabricated using Super-Smart-Stack technology.

Authorized licensed use limited to: TOHOKU UNIVERSITY. Downloaded on February 28,2010 at 21:56:44 EST from IEEE Xplore. Restrictions apply.