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A Study of Nondestructive Inspection Method of Bump Connection in Three Dimensionally Stacked Chip Structures

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Abstract

The three dimensionally stacked chip structures of electronic packages and modules have started to be used to maximize assembly density and to minimize signal delay. Since the thickness of the stacked silicon chips has been thinned to less than 100 μm, the local thermal deformation of chips has increased drastically because of the decrease of bending elasticity of the chips. In such a stacked structure, it is hard to inspect the adhesion condition of metallic bumps that connect a bottom chip with an upper chip. We have, therefore, proposed a new nondestructive evaluation method for detecting delamination between a chip and metallic bumps by applying a measurement of local surface deformation of the chip. The magnitude of the local deformation was calculated using a three-dimensional finite element analysis. The local deformation of a silicon chip between the nearest two bumps is a strong function of the thickness of the chip, the pitch of the bumps, and the magnitude of the mismatch of the thermal expansion coefficient between the bump and underfill material. The amplitude of the local deformation exceeds 200 nm easily, and it sometimes reaches 600 nm when the underfill material used for assembly was assumed to be epoxy resin. To confirm that such an estimated local deformation of an LSI chip thinner than 100 μm appears in actual stacked structures, we applied a scanning blue laser microscope to measure the local deformation. The measured local deformation was about 200 nm when the thickness of a chip was 100 μm, as was predicted by a finite element analysis. In addition, the surface deformation of the upper chip changed drastically depending on the layout of the metallic bumps between the upper and the lower chip. The predicted local displacement at the sample surface was also validated by using a white light interference microscope.

Introduction

In electronic devices used in mobile phones or PCs, the improvement of electronic performances, miniaturizations, and low cost processing have been strongly required. Therefore, an area-arrayed flip chip bonding structure and a multi chip packaging structure such as SiP (System in a Package) and MCM (Multi Chip Module) have been developed for practical use. Moreover, a three dimensionally stacked structure with area-arrayed metallic bumps is introduced to maximize assembly density and to minimize signal delay [1]. The thickness of chips in these packaging structures is thinned to less than 100 μm and a number of stacked layers will reach 10 layers within a few years. In addition, a wiring method has been changed from wire bonding to flip chip bonding with an area-arrayed-bump structure for maximizing the number of I/O pins.

The degradation of the reliability of such miniaturized and highly densified packaging structures is worried about because of the increase of the number of interconnections, difficulty of the production process of the stacked structure [2]-[6]. In addition, non-destructive inspection for bump interconnections of an area-arrayed stacked structure is indispensable. However, conventional visual inspection or optical inspection method can not be applied because invisible areas exist in this packaging structure. Therefore, some non-destructive inspection methods have been proposed [7]-[12]. But there is no inspection method that can detect thin delamination by high horizontal resolution. Thus, we have proposed a new non-destructive inspection method for detecting open failure in flip chip structures [13]. The local thermal deformation is caused by mismatch in the coefficient of thermal expansion among packaging materials. This local deformation is increased by thinning of Si chips. For instance, when the thickness of a Si chip is less than 100 μm, the local deformation becomes more than several hundreds nm at a Si chip surface. When a delamination or a lack of bump occurs at the interface between metallic bumps and a Si chip, the local deformation at the surface of the Si chip is significantly increases because of the change of the local stiffness of the bump interconnection layer. If this local deformation can be measured, it is possible to detect open failures caused by delamination or a lack of a bump. We have previously estimated the amplitude of this local deformation and validated the existence of this local deformation using a scanning blue laser microscope. In this paper, we discuss the effect of an open failure in multi layer bump interconnections on the surface deformation of the top chip using finite element analysis to apply this inspection method to the detection of the open failures in three-dimensional stacked structures. The local surface deformation of the top chip varies drastically depending on the layout of the metallic bumps in the lower interconnection layers. Thus, it is important to calibrate the surface deformation without any open failures before the inspection. The difference between the measured surface deformations with the calibrated one tells us the abnormal signal, i.e. occurrence of open failures. The estimated predicted local displacement at the surface of the top chip is validated by using a white light interference microscope.

Finite element analysis of local thermal deformation

The effect of the structure of the lower interconnection layer (bump alignment) on the surface deformation of a upper chip was analyzed using a finite element method. The change

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of the structure includes not only the relative position between the bumps in the upper layer and those in the lower layer but also the delamination and a lack of bumps. The finite element model is show in Figure 1. The size of a chip was fixed at 10 mm square, and the thickness of the chip was varied from 200 μm to 20 μm. The chip was mounted on a substrate by area-arrayed bumps with and without underfill. The diameter and the height of a bump were varied from 200 μm to 50 μm, and the interval of the aligned bump was varied from 400 μm to 100 μm. The total number of the nodes and elements of the three dimensional model were about 20000, respectively. The Si chip was connected with the substrate at room temperature. Then, the underfill was assumed to be filled around the bumps and cured at 150°C. The materials constants used for the analysis are summarized in Table 1. The yield stress of 300 MPa was assumed only for Cu bumps. Other materials were assumed to be elastic material. The elastic-plastic analysis was performed and the local residual deformation was discussed at room temperature. In addition, the effects of a lack of bump and delamination between a bump and a Si chip on the local deformation at a surface of a Si chip were also analyzed. The difference in the local deformation between the regular (normal) structure and the structure with defects (abnormal structure) was analyzed.

Figure 2 indicates the definition of the relative displacement, in other words, the difference of the local deformation at a surface of a Si chip between the normal structure and the abnormal structure. First, the local deformation at the surface of a Si chip in the normal (no defect) structure was calculated. In this figure, three bumps A, B, C are aligned at a constant interval. Then the center bump B is eliminated to model a missing bump. Then, the local deformation of this structure is analyzed. The relative displacement is defined as the difference of the magnitude of the surface deformation of the Si chip at the center position of a bump B as shown in the figure.

To define the relationship between the upper and the lower layer of bump alignment, we used "ratio of the overlapping area of bumps in the upper layer and the lower layer" as shown in Figure 3. When the ratio is 100%, an in-plain position of upper bumps is completely same as the position of the lower bumps. When the ratio is 0%, there is no overlapping area, in other words, the position of the bumps in the upper layer is the position of underfill in the lower layer.

In actual structures, open failures may occur at plural bumps at the same time. Thus, it is important to define the failure mode separately. Figure 4 shows the calculated surface deformation of a Si chip under which one bump and two bumps are assumed to be delaminated. When one bump was delaminated (the delamination point is x=0.2), the abnormal local deformation of about 450 nm appeared at the surface of the chip on the delaminated bump. Similarly, when the isolated two bumps were delaminated (the delamination points are x=0.2, 0.8), the change of surface displacement at each position is exactly the same as that calculated assuming one-bump delamination. However, when the adjacent two bumps were delaminated (the delamination points are x=0.2, 0.4), the change of the shape of the surface deformation was seemed

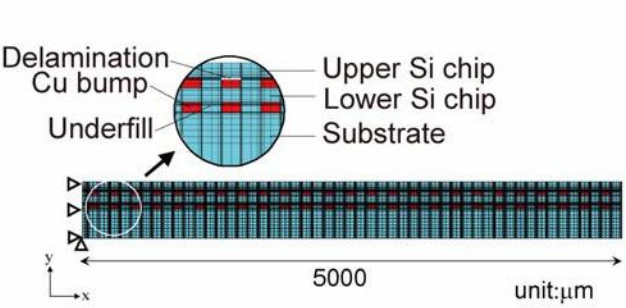


Figure 1. A Finite element model of two-layer flip chip structure.

Table 1. Materials constants for deformation analysis.

Material	Young's modulus (GPa)	Poisson's ratio	Thermal expansion coefficient (ppm/K)	Yield stress (MPa)
Si chip	130	0.28	2.3	-
Cu bump	130	0.34	16	300
Underfill	5	0.3	70	-

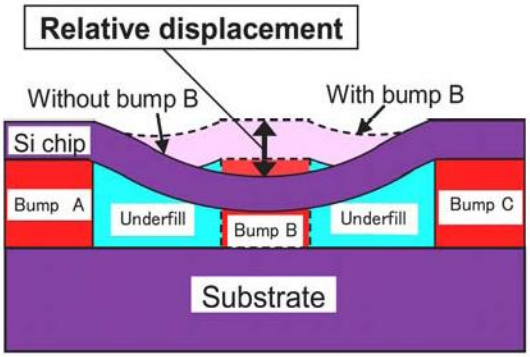


Figure 2. Definition of relative displacement.

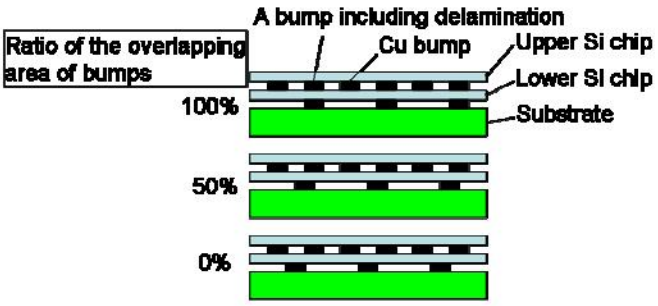


Figure 3. Definition of ratio of the overlapping area of bumps between the upper interconnection layer and the lower interconnection layer.

to be different. But it was confirmed that the calculated change was the summation of the local change of the one delaminated bump. Therefore, it is confirmed that even when there are plural defects under one chip, each delamination or lack of bump can be detected separately by measuring the surface deformation of a Si chip precisely.

Figure 5 shows the effect of filling of underfill around a delaminated or lacked bump on the change of the local surface deformation of a Si. The gap between the Si chip and the delaminated bump was assumed to be 1 μm. The calculated result of the normal position at distance of 0.4 or 0.6 mm (without delamination of a bump), the change of the local deformation on the delaminated bump at distance of 0.2 mm reaches about 200 nm. The difference is enhanced to about 400 nm when underfill is filled around the delaminated bump. However, once the delaminated gap is filled by underfill, the change of the local deformation decreases remarkably to about 30 nm. When the delamination occurs after the underfill filling, large change of the local deformation of a Si chip appears and it is easy to detect the change. However, in case the delamination occurs before the underfill filing and the delaminated gap is filled by the underfill, it is hard to detect the change. Therefore, two step inspection before and after the filling of underfill is indispensable for the reliable detection of the delamination.

Next, the effect of the bump structure in the lower interconnection layer on the surface deformation of the upper chip was analyzed. Figure 6 shows the effect of the dominant structural factors of the bump in the lower layer on the relative displacement at the upper chip surface on a delaminated bump after filling of underfill. The pitch between the bumps is fixed at 200 μm in both upper and lower layers. The ratio of the overlapping area between the upper and the lower bumps was fixed at 100%. The dominant structure factors that affect the surface deformation of a thinned chip are found to be the height of bumps, the diameter of bumps, and the thickness of bumps by previous analysis in a 1-layered flip chip model [4]. However, no significant change occurred even when those parameters were varied by about twice. No change was also observed in the structures before the underfill filling. Similarly, there was no change even when the ratio of the overlapping area of bumps was varied from 100% to 0%.

However, when the pitch of bumps in the lower interconnection layer was broadened compared with that of the upper layer, the change of the surface deformation of the upper chip becomes very sensitive to the bump structure in the lower interconnection layer. Figure 7 indicates the effect of the ratio of overlapping area of bumps on the relative displacement at the surface of the upper chip. The pitch of the upper and the lower bumps are assumed to be 200 and 400 μm, respectively. The 1-μm gap delamination of a bump was assumed and underfill was filled around the bump. The relative displacement varies drastically with changing the ratio of overlapping area of bumps. The relative displacement at the ratio of bumps 100% is about three times higher than that of 0%. To make clear the reason for this change of local deformation, the actual displacement at the surface of the upper chip is shown in Figure 8. In this figure, the delaminated

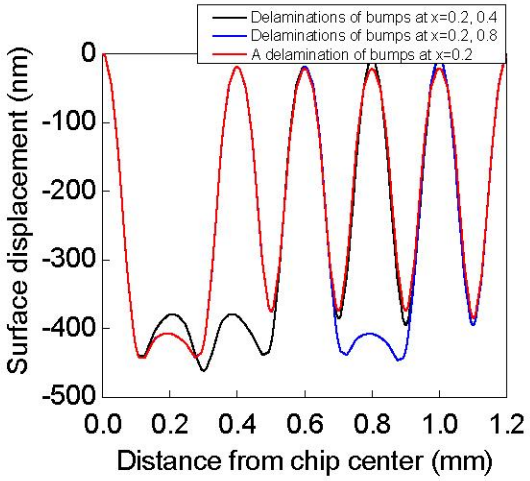


Figure 4. The change of the local surface displacement of a Si chip under which one or two bumps are delaminated.

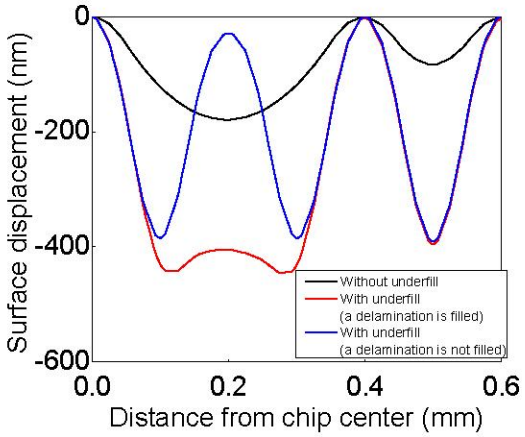


Figure 5. Effect of filling of underfill around a delaminated bump on the change of surface displacement of a Si chip.

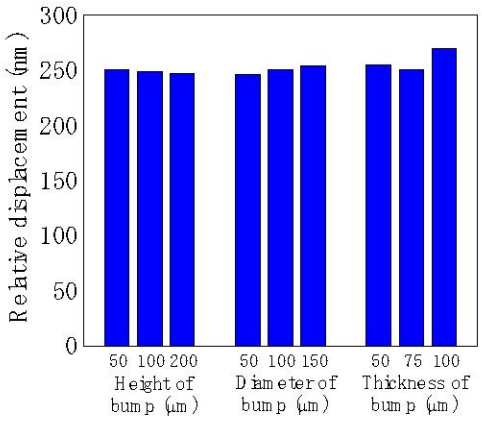


Figure 6. Effect of dominant structural factors on the relative displacement at the surface of a upper layer chip.

bump exists at 0.3 mm. The local deformation around this area is clearly different from other normal area. Even in the normal area (at distance from 0.6 mm to 1.2 mm), the local deformation varies depending on the ratio of overlapping area of bumps. However, it was found that these surface deformation curves consist of two periodic curves. One of the periods is 200 μm, and another one is 400 μm. These periods agree with the pitches of the upper bumps and the lower bumps respectively. The surface deformation of the upper chip is determined by the combination of the deformation caused by the bump alignment in the bottom interconnection layer and that in the under interconnection layer.

The reason for the change of the local deformation around the delaminated bump is the variation of the constraint of the deformation caused by rigid bumps. When the pitch of the bump is large, a Si chip can deform easily between the adjacent bumps because the elastic constant of underfill is much smaller than that of the bump material. Thus, when the pitch of the adjacent bumps in the lower interconnection layer is larger than that in the upper layer, the surface deformation of a silicon chip stacked between the two layers increases comparing with a chip stacked between the same alignment layers. Thus, the surface deformation of the upper chip on the delaminated bump shown in Fig. 7 varies depending on the ratio of overlapping area of bumps.

These deformation curves can be estimated quantitatively by a finite element analysis or measured directly by laser system. Thus, an inspection algorithm can be established by obtaining the normal deformation curve at a surface of an upper chip considering the effect of the interconnection structure in the lower layer. Therefore, it is possible to find open failures in LSI chips stacked by an area-arrayed bump structure by detecting the change of surface deformation of the upper chip.

Measurement of surface displacement by a white light interference microscope

The estimated local deformation of a Si chip in a flip chip bonding structures was validated using a white right interference microscope. The area-arrayed bump structures were made on a substrate that was made of a thermally oxidized single-crystalline Si wafer as shown in Figure 9. The thickness of the wafer was 280 μm. The 100-μm square bumps were area-arrayed on the substrate by changing the intervals as shown in the figure. Some intentional lacks of bump were also introduced on the substrate to measure the effect of the lack of a bump on the local deformation of the mounted thin Si chip.

The 75-μm thick and 10-mm square chips were mounted on the various substrates with different alignment of bumps at room temperature using conducting paste. The mounted system was heated at 150°C for curing the conductive paste. The residual surface deformation of the thinned chip was measured using a white light interference microscope. The short coherence length of white light enables us to measure the surface displacement of the mounted chip with high resolution and wide range. It is possible to measure the deformation by vertical resolution of 0.1 nm and a maximum range of the

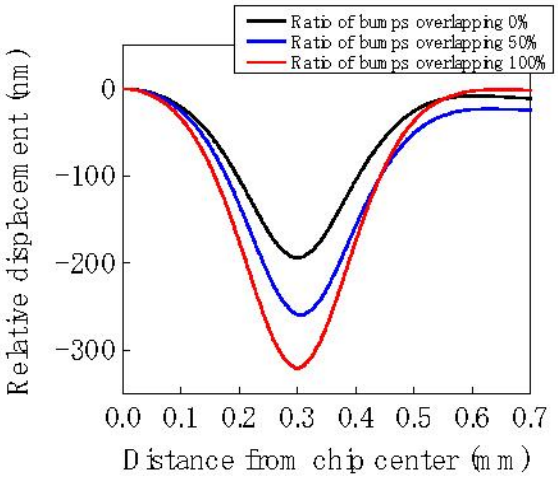


Figure 7. Effect of the ratio of overlapping area of bumps on relative displacement at a upper layer chip.

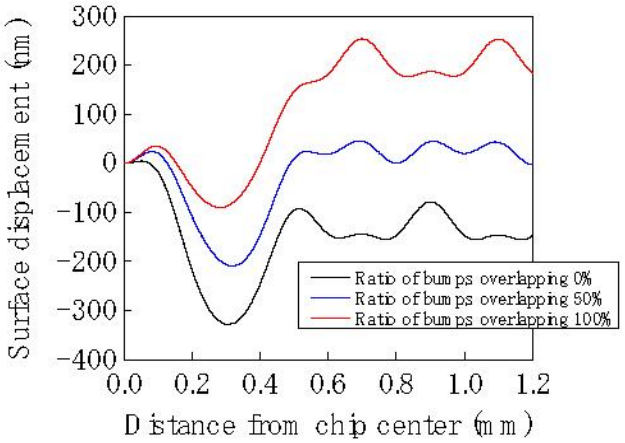
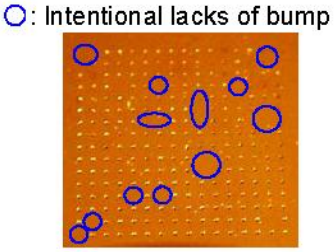


Figure 8. Effect of the ratio of bumps overlapping on surface displacement at a upper layer chip. This model is filled by underfill.



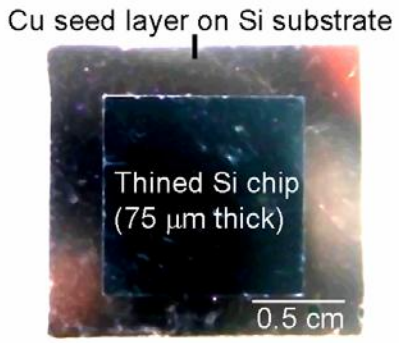


Figure 9. Outlook of a test flip sample

vertical displacement is 100 μm. The horizontal resolution is 1.4 μm when using a x10 objective lens. Thus, this white light interference microscope can be applicable to measuring the displacement of a smooth surface.

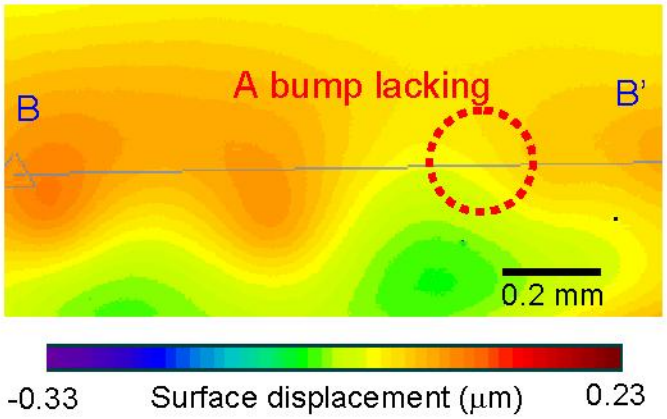
Figure 10(a) shows the measured two-dimensional distribution of the local surface deformation of a Si chip mounted without underfill. In this sample, the regular pitch of the 100-μm wide Cu bumps was 400 μm. And one Cu bump was eliminated intentionally for modeling the lack of a bump. The amplitude of the measured surface deformation is indicated by color contours. Concentric local surface deformation of the Si chip clearly appears on the Cu bumps existing under the chip. The pitch of these concentric deformation patterns is same as the pitch of periodically aligned Cu bumps.

However, the local concentric deformation pattern doesn't appear at the position of the missing bump. The local deformation around this area clearly differs from other areas where bumps are aligned normally under the chip. Figure 10(b) summarizes the surface displacement of the chip along the A-A' line shown in Fig. 10(a). The periodic surface deformation clearly appears where the bumps are aligned normally under the chip. The amplitude of this surface displacement is about 30 nm. However, the surface displacement changes from 30 nm to -30 nm at distance of about 0.8 mm where a bump is eliminated intentionally under the chip. The relative displacement, that is the difference of the surface displacement between a point of normal bump interconnection and a point of abnormal one, is thus, about 60 nm. This relative displacement can be detected easily by applying a laser measurement system. In addition, the pitch of the peak position of the periodic deformation changes from 400 (normal area) to 800 μm (abnormal area). This change of the pitch of the peak position of the deformation is also caused by the lacking of a bump.

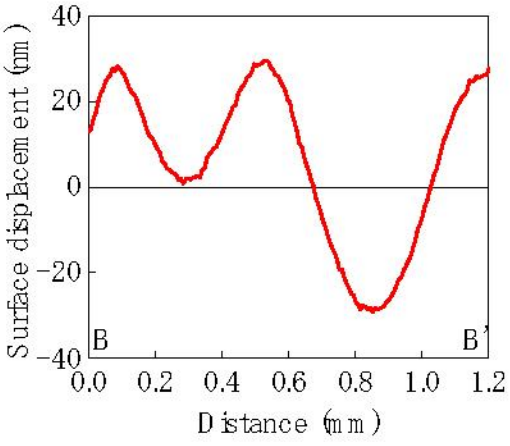
Therefore, it is concluded that defects in the bump interconnection can be detected accurately by measuring the changes of both the local surface displacement and the pitch of the peak position of the periodic deformation.

Conclusions

To develop a nondestructive inspection method for detecting defects (open failures) of bump interconnection in three-dimensionally stacked chip structures, we have analyzed the effect of the interconnection layer structure on the local surface deformation of a stacked thin Si chip. The local surface deformation caused by delamination of a bump varies from about 100 nm to 400 nm depending on the structure of the bump alignment in each interconnection layer. The two step inspection method of detecting the local surface displacement of a silicon chip before and after filling underfill is effective for highly reliable inspection of open failures. When the pitch of the bump alignment in the lower interconnection layer is larger than that in the upper layer, it is necessary to calibrate the deformation caused by lower layer structure because the final surface deformation of a chip is determined by not only the bump structure under the chip but also the bump structure in the lower layer. The estimated change of the local surface deformation caused by the delamination of a bump was validated by measurement using a white light interference microscope. Both the amplitude of



(a) The distribution of surface displacement



(b) The cross-sectional displacement

Figure 10 Measured displacement at a surface of a Si chip unfilled by underfill material with lacks of bump. The pitch of Cu bumps is 400 μm.

the local deformation of the chip on the delaminated bump and the pith of the peak position of the periodic deformation were observed clearly. The measured change of the local deformation was about 60 nm, and the change of the pitch was about 400 μm. Therefore, it is possible to inspect open failures of a silicon chip mounted by area-arrayed small bumps nondestructively and quantitatively by detecting the change of the local surface deformation of the chip.

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