FABRICATION OF MICROPROBES ON A ULTRATHICK GLASS SUBSTRATE WITH NARROW-PITCH ELECTRICAL FEEDTHROUGHS FOR NEXT-GENERATION LSI BURN-IN TESTS

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ABSTRACT

This paper describes microprobes fabricated on a thick glass substrate with narrow-pitch electrical feedthroughs for the application to the next-generation LSI burn-in test. The feedthrough glass substrate was sliced off from the block of stacked Pyrex glass substrates with thin metal lines. The pitch of the feedthroughs in one direction is defined by photolithography, and thus can be made sufficiently small. The probes were made of heavily-boron-diffused silicon, and fixed on the feedthrough glass substrate by anodic bonding. The feedthrough glass substrate was evaluated in terms of the resistance of the feedthroughs. The probes were evaluated in terms of mechanical robustness against overdrive.

1. INTRODUCTION

A probe card is an array of probes, which mechanically and electrically contact the bond pads of LSI under test to select known good dyes [1]. With the evolution of LSI, LSI probing technology must be advanced together, because the pitch of the bond pads decreases, and simultaneously the number of the bond pads per chip and the size of LSI wafers increase year by year. In the future, the pitch of the probes will decrease to 50 µm, and the number of the probes on a probe card will increase to 10000 or more. Thus, the probes must be arrayed at narrow pitches on a rigid substrate with high-density electrical feedthroughs.

The rigidity of the substrate is important, because a contact force of 1–10 gf is applied to each probe and the total contact force reaches 10–100 kg. The electrical connection from each probe to the printed circuit board (PCB) of the probe card must be established through high-density electrical feedthroughs. In addition, a LSI burn-in test, in which a LSI wafer is heated up to 150 °C, requires the matching of thermal expansion between the probe card and the LSI wafer.

Conventionally, the probe card uses an alumina-based ceramic substrate referred as high temperature co-fired ceramic (HTCC) substrate. The HTCC substrate has a sufficient rigidity and can include multi-layered conductive tungsten or molybdenum lines inside, but its coefficient of thermal expansion (CTE) is approximately 7 ppm/K, which is much larger than that of silicon. A low temperature co-fired ceramic (LTCC) substrate with more conductive cupper, silver or gold lines is also available, but its CTE is also higher than that of silicon (e.g. 5 ppm/K). Furthermore, the minimum pitch of feedthroughs (vias) in the HTCC and LTCC substrates is 200–300 µm, which does not meet the requirement of the probe pitch for advanced LSI tests.

In this paper, we propose a solution to satisfy the above requirements for the next-generation LSI burn-in tests, and present the fabrication and evaluation of microprobes on a novel feedthrough glass substrate.

2. CONCEPT

The concept which we propose is illustrated in Fig. 1. MEMS-based probes are formed on a stacked-type feedthrough glass substrate [2], which is connected to a special low CTE LTCC substrate using AuSn eutectic solder [3]. The LTCC substrate is electrically connected to the PCB using compliant pogo pins, which absorb thermal expansion mismatch between the LTCC substrate and the PCB. In this study, the probes are made of heavily-boron-diffused p^{++} silicon, and have a structure shown in Fig. 2. This concept can be also applied to other types of microprobes.

The stacked-type feedthrough glass substrate includes thin film metal feedthroughs with sufficiently narrow pitches defined by photolithography in one direction. The thickness of the feedthrough glass substrate can be freely determined from submillimeters to millimeters or more without the penalty of the feedthrough pitch. The material of the feedthruough glass substrate is Pyrex glass, which has no CTE mismatch problem with silicon. In addition, anodic bonding can be used for connection between the feedthruough glass substrate and the silicon probes.

The low CTE LTCC substrate has a CTE of 3.4 ppm/K, which is close to that of silicon. It contains codierite and 50–70

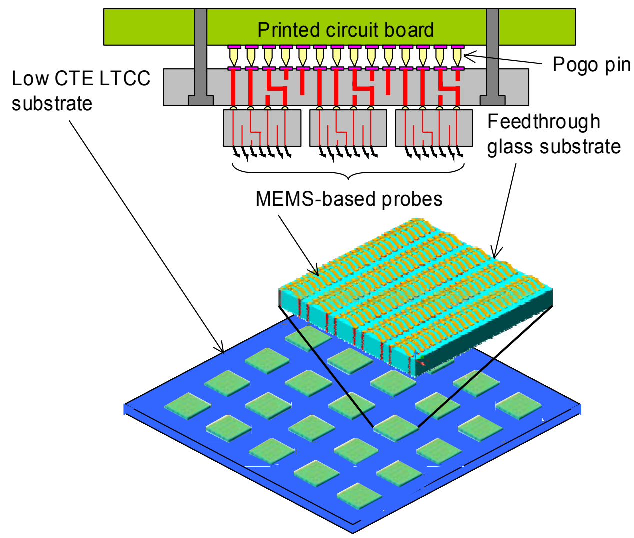

Figure 2: Schematic of a LSI burn-in test probe card using a feedthrough glass substrate and a low CTE LTCC substrate.

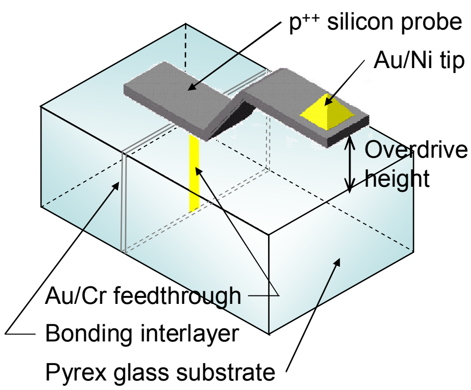

Figure 2: Structure of the probe on the feedthrough glass substrate.

wt % of glass. By using Pyrex glass, the LTCC substrate applicable to anodic bonding can be produced. The LTCC substrate is made by stacking and sintering green sheets with vias filled with metal paste. Therefore, the thickness can be freely determined by the number of the stacked green sheets, and inner electrical lines and vias can be variously designed.

3. FABRICATION PROCESS

Fabrication process of feedthrough glass substrate

Figure 3 shows the fabrication process of the stacked-type feedthrough glass substrate. On Pyrex glass substrates with a thickness of 1 mm, thin film metal lines are formed by the lift-off process of gold (150 nm)/platinum (50 nm)/chromium (50nm). The glass wafers with the thin film metal lines are stacked and bonded with each other using phenyl methyl siloxane-based adhesive (i seal, S.F.C). This adhesive is highly-viscous liquid like water glass at 120–130 °C, and is solidified by heating at 150 °C (30 min), 220 °C (30 min) and finally 300 °C (10–30 min). The solidified adhesive keeps practical bonding strength up to 380 °C, and can be used for vacuum sealing. The stacked glass wafer block is then sliced using a wire saw as the slicing surfaces cross the stacking interfaces vertically.

Figure 4 shows the fabricated feedthrough glass substrate with a thickness of 3 mm. The aspect ratio of the feedthroughs, i.e. the feedthrough width divided by the substrate thickness, is much higher than that for conventional feedthrough glass substrates [4–6]. Furthermore, the feedthroughs which have narrow pitches on one side can appear with larger pitches on the other side by photolithographic patterning. This feature is useful for the electrical connection of the probe array with narrow pitches to the LTCC substrate with wider pitches.

Fabrication process of probes

The fabrication process of the probes is shown in Fig. 5. A (100) silicon substrate is etched using tetramethyl ammoniumhydroxide (TMAH) to make trenches with a depth of 100 μm, which defines the overdrive height of the probes. The silicon wafer is thermally oxidized, and then

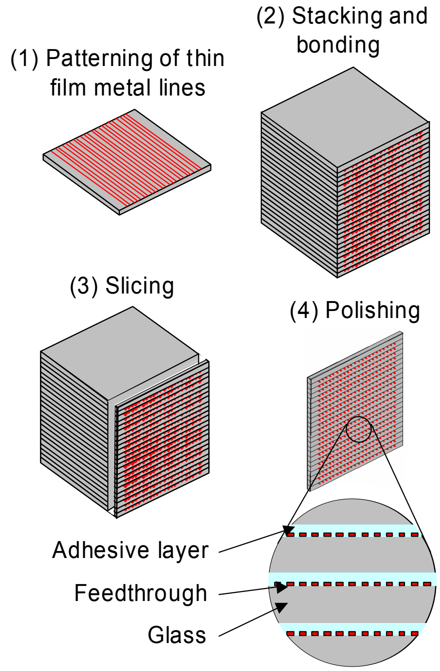

Figure 3: Fabrication process of the stacked-type feedthrough glass substrate.

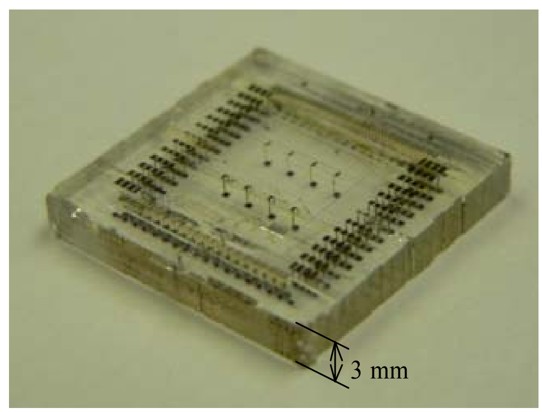

Figure 4: Stacked-type glass substrate with narrow-pitch feedthroughs.

probe shapes are defined by patterning photoresist sprayed in the wet-etched trenches. From the oxide mask windows, boron is heavily diffused into silicon for p^{++} etch stop. Probe tips are made by electroplating gold and nickel into wet-etched pits, which are composed of (111) silicon planes. This molding method using the wet-etched silicon pits allows us to make sharp tips. The silicon wafer is bonded to the feedthrough glass substrate by anodic bonding technique, and then silicon is etched away using ethylenediamine, pyrocatechol and water (EDP) to release the p^{++} silicon probes on the feedthrough glass substrate.

Figure 6 shows prototyped probes and a probe card. The probe is a 80-μm-wide slantwise cantilever, which realizes scratch motion on aluminum bond pads to remove the surface oxide for low contact resistance. Also, it has an overdrive height of 100 μm to absorb the unevenness of a LSI wafer under test. The feedthrough glass substrate with the probes is set on the low CTE LTCC substrate and the PCB. In this style, the probe card is used for LSI tests, but the electrical connections were not established between the feedthrough glass substrate and the LTCC substrate in this study.

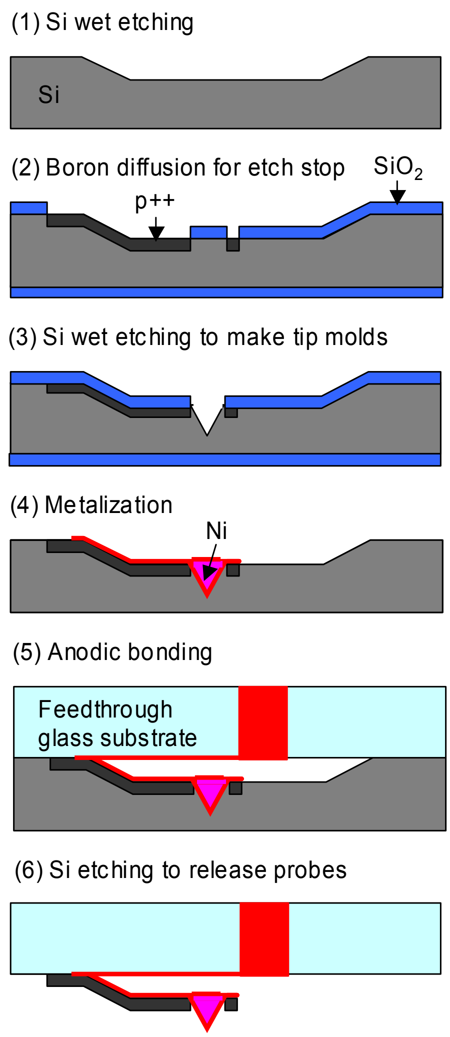

Figure 5: Fabrication process of the probes on the feedthrough glass substrate.

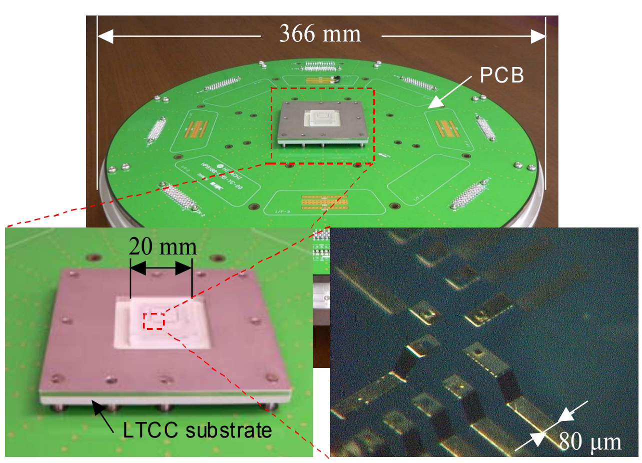

Figure 6: Prototyped probes and probe card with the low CTE LTCC substrate and the PCB.

4. EVALUATION

Resistance of feedthroughs

Before the measurement of the electrical resistance of the feedthroughs, the feedthrough glass substrate was once subjected to high voltage across the thickness (1 kV) and high temperature (400 °C). This simulates the condition of anodic bonding. After that, the surfaces were cleaned by ion milling and light acid etching. Gold (100 nm)/titanium (50 nm) pads were formed on one side, and the other side was covered with gold (100 nm)/titanium (50 nm) in whole. The measurement was performed using a tungsten cantilever probe, as shown in Fig. 7.

The resistance of the feedthrough itself was obtained by subtracting the parasitic resistances of the metal films, the tungsten cantilever probe, their contact and wires. Figure 8 summarizes the measured resistances of the feedthroughs. The resistances can be divided into two groups: low resistance group (< 75 Ω) and high resistance group (> 375 Ω). The feedthroughs in the high resistance group could have a problem in contact between the feedthroughs and the metal pads, or could be damaged in the fabrication or evaluation. Therefore, we think that the resistances in the low resistance group are valid, and averaged them. The average resistance of the feedthroughs is 16.4 Ω, and the minimum one is 9.7 Ω. The resistance calculated based on the dimensions of the feedthrough and the resistivities of bulk metals is 4.4 Ω, which is roughly four times as low as the measured average resistance.

Mechanical and electrical properties of probes

To evaluate the mechanical robustness against overdrive, the probes on the feedthrough glass substrate were mechanically pushed using the tungsten cantilever probe, as shown in Fig. 9, until the probes were broken. For some probes,

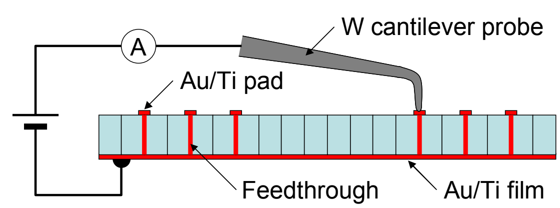

Figure 7: Measurement method of the resistance of the feedthroughs.

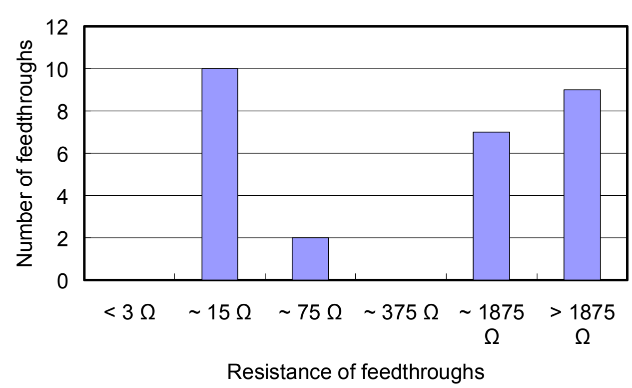

Figure 8: Distribution of the measured resistances of the feedthroughs.

the electrical resistance from the probe tip to the metal pad on the feedthrough glass substrate was measured using the tungsten cantilever probe. Figure 10 shows the allowable overdrives, i.e. the vertical deformations at which the probes were broken. The deformation of the tungsten cantilever probe was negligible, and the measurement included an uncertainty of 5 µm due to difficulty in finding the start point of the contact.

The initial height of the probes from the feedthrough glass substrate is 100 µm, but the allowable overdrive in average is only 36 µm. Because the probe card must follow the unevenness of a LSI wafer under test, the allowable overdrive with a safety margin should be larger than 100 µm. In this experiment, most of the probes were broken at the corner indicated by a cross in Fig. 9. The measured resistance from the probe tip to the metal pad ranged 2.7 kΩ to 4.5 kΩ, which is unacceptably high. This could be because the probe tips and following metal lines were eroded in the fabrication, or the contact between the probes and the feedthrough glass substrate, which was established by anodic bonding, was imperfect.

5. CONCLUSION

For the next-generation LSI burn-in test, microprobes were fabricated on a thick glass substrate with narrow-pitch electrical feedthroughs. The feedthrough glass substrate was sliced off from the block of stacked Pyrex glass substrates with thin metal lines. The pitch of the feedthroughs in the direction of the stacking interfaces is defined by photolithography, and thus can be made

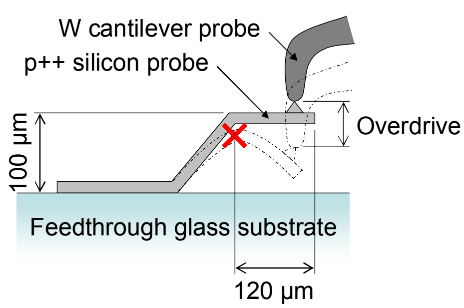

Figure 9: Measurement method of the mechanical and electrical properties of the probes.

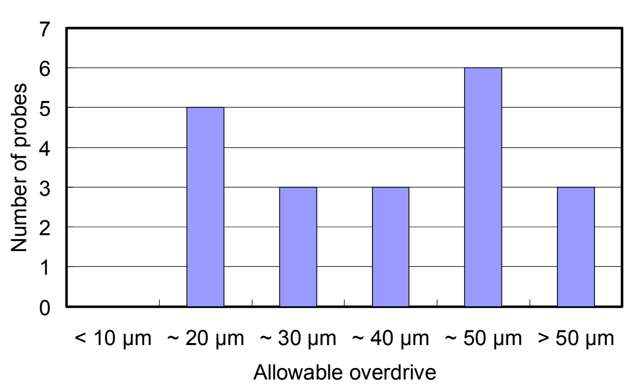

Figure 10: Distribution of the allowable overdrives, at which the probes were broken.

sufficiently small. The feedthrough glass substrate is 3 mm thick, and works as a rigid interposer with a coefficient of thermal expansion identical to that of silicon. The probes were made of heavily-boron-diffused silicon, and fixed on the feedthrough glass substrate by anodic bonding.

The feedthrough glass substrate was evaluated in terms of the resistance of the feedthroughs. The measured resistances can be divided into two groups: low resistance group (< 75 Ω) and high resistance group (> 375 Ω). The average of the low resistance group was 16.4 Ω, which is roughly four times as large as the calculated value. The probes were evaluated in terms of mechanical robustness against overdrive. The allowable overdrive, at which the probe was broken, was 36 µm in average.

The current results of the evaluation are unsatisfactory, but can be improved by the improvement of the fabrication and design. We believe that the developed technology is useful not only the prove card for the next-generation LSI burn-in test but also a variety of arrayed MEMS.

ACKNOWLEDGEMENTS

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REFERENCES

[1] W. R. Mann, F. L. Taber, P. W. Seitzer, J. J. Broz, "The Leading Edge of Production Wafer Probe Test Technology", *Proc. IEEE International Test Conference*, Charlotte, NC, USA, October 26–28, 2004, pp. 1168–1193.

[2] S. Tanaka, S. Fujimoto, O. Ito, S.-H. Choe, M. Esashi, "Laterally stacked glass substrates with high density electrical feedthroughs", *J. Micromech. Microeng.*, 17, 2007, pp. 597–602.

[3] S.-H. Choe, S. Tanaka, M. Esashi, "A Matched Expansion MEMS Probe Card with Low CTE LTCC Substrate", *Proc. IEEE International Test Conference*, Santa Clara, CA, USA, October 23–25, 2007, Paper 20.2.

[4] X. Li, T. Abe, Y. Liu, M. Esashi, "Fabrication of High-Density Electrical Feed-Throughs by Deep-Reactive-Ion Etching of Pyrex Glass", *J. Microelectromech. Syst.*, 11, 2002, pp. 625–630.

[5] Y.-K. Park, H.-W. Park, D.-J. Lee, J.-H. Park, I.-S. Song, C.-W. Kim, C.-M. Song, Y.-H. Lee, C.-J. Lim, B.-K. Ju, "A Novel Low-Loss Wafer-Level Packaging of the RF-MEMS Devices", *Proc. The Fifteenth IEEE International Conference on Micro Electro Mechanical Systems*, Las Vegas, NV, USA, January 20–24, 2002, pp. 681–684.

[6] J. Chae, J. M. Giachino, K. Najafi, "Wafer-Level Vacuum Package with Vertical Feedthroughs", *Proc. The Eighteenth IEEE International Conference on Micro Electro Mechanical Systems*, Miami, FL, USA, January 30 – February 3, 2005, pp. 548–551.