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Application of a semiconductor tip to capacitance microscopy

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A semiconductor tip has been applied to the scanning capacitance microscopy (SCM). Local electrostatic fields are measured through depletion of carriers at the tip end. A Si microcantilever with the sharp end is employed. This SCM technique has been used in a capacitance observation of a dielectric/electrode sample. Potentiometry using this technique is demonstrated in an experiment of charge injection recording on a polymer film.
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The scanning capacitance microscope (SCM) is a powerful tool for observation of electronic materials and devices.[1–7] The SCM has been also applied in a scanning probe microscopy memory,[4,6] aimed at very high data density.

One of the major drawbacks in the SCM is, at present, that the lateral resolution is not very good because the capacitance is a long distance interaction. Another is that the capacitance sensitivity is seriously reduced by the stray capacitances, which add to the input capacitance of the capacitance sensor. The stray capacitance in the conventional SCMs is on the order of 10^{-14}–10^{-13} F, while the local capacitance to be detected is 10^{-19}–10^{-17} F. So far, a number of techniques have been developed to improve the lateral resolution and the sensitivity: capacitance modulation to obtain the differential capacitance[2–6] and active shielding of the probe to reduce the stray capacitances.[7] A completely different approach is to integrate a very small sensor of electrostatic fields with the tip at its end. Then the sensor is sensitive only to local fields at the tip end, regardless of the stray capacitances. In this letter, we demonstrate such a new SCM technique using a semiconductor tip.

Figure 1 shows a block diagram of the proposed SCM technique. The system as a whole is a combined capacitance/force microscope[4–6] in contact mode. The new technique features a semiconductor tip unlike the conventional SCMs, which use a metallic tip. As shown in Fig. 1, the end of a Si probe, a force microscope cantilever, is used as the semiconductor tip. The tip-sample system constitutes a metal–insulator–semiconductor (MIS) diode for insulator/electrode structures and also for uncovered electrodes if the Si tip is covered with an insulator, e.g., SiO_2. The degree of depletion of carriers in the tip end changes according to the dc bias voltage applied to the tip-sample system. Then the local tip-sample capacitance and the potential at the sample surface (including any additional dc bias) are measured through the depletion capacitance. The variation in the depletion capacitance is sensed with a capacitive pickup[1–6] consisting of an ultrahigh frequency LC resonator. For high sensitivity, the depletion capacitance is modulated with an ac bias voltage and then lock-in amplified. The sensitivity can be further improved by replacing the MIS diode with a MIS transistor, which directly senses the local field without being affected by the stray capacitances. Interestingly, the potentiometry using the proposed technique is made in contact mode, which means that the measurement speed can be much higher than that in the dynamic mode force microscopy potentiometry.[8,9]

The experimental setup is the same as that in our previous work[6] except for the Si probe. For the probe, we have batch-fabricated microcantilevers from a Si(100) wafer (*n*-type, 1–10 Ω cm), in a manner similar to that previously reported.[10] The microcantilevers are also good force sensors because of the excellent mechanical properties of single-crystal Si, for which, in fact, Si cantilevers are widely used.[10,11] Figure 2 is a scanning electron micrograph of a fabricated cantilever. The key process in the cantilever fabrication is Si anisotropic etching, by which one side of the wafer is first etched to pattern the cantilevers and then the other is etched to release them. The etchant was a tetramethyl ammonium hydroxide (TMAH) solution,[12] compatible with MIS device fabrication. As shown in Fig. 2, the corners of the cantilever are very sharp because they are determined by crystallographic planes. The tip, the end of the cantilever, is successfully tapered and sharpened by taking advantage of the convex corner cutting,[13] which progresses in ⟨221⟩ directions under the SiO_2 mask. This technique is easy, simple, and gives practically 100% reproducibility of the tip shape. The tip width is on the order of several tens of nanometers at the apex. The size of the cantilevers used in the following experiments is 1000 μm×100 μm×10 μm. As shown in Fig. 1, the tip is approached to the sample with an angle of 6–10° relative to the sample surface. The back of the canti-

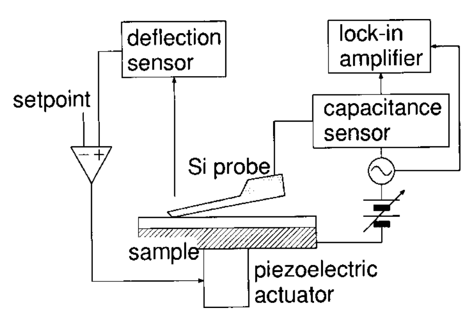

FIG. 1. Block diagram of the proposed SCM technique.

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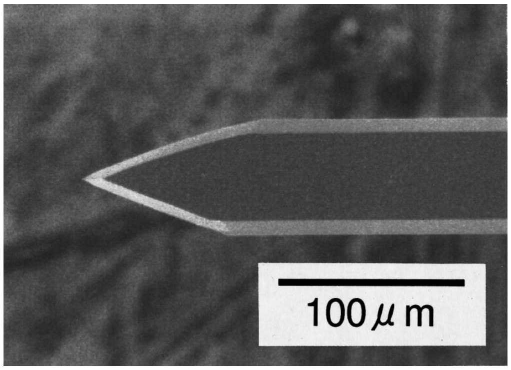

FIG. 2. Micromachined Si probe. Part of a 500-μm-long cantilever is shown. The taper of the end is determined by the two {221} sidewalls.

lever is coated with an Al film about 100 nm thick in order to reduce the resistance.

The performance of the new SCM can be well demonstrated by observing a dielectric film having steps. We have observed a thermally grown SiO_2 film on a highly doped *n*-type Si wafer [(100), 0.01–0.02 Ω cm], in which the depletion layer thickness is negligible. The thickness of the SiO_2 film is varied periodically (250 and 120 nm, 5 μm line/space). The dc and ac bias voltages during the measurement were 0 and 3 V_{p-p} at 100 kHz, respectively. Figure 3 shows topographic and capacitance images of the sample. The capacitance image reflects the local tip-sample field determined by the film thickness.[5] The capacitance signal for the thickness of 120 nm was larger than that for 250 nm by the factor of about 1.5. The small increase and decrease in the capacitance signal seen on each side of the edge are geometric effects.

Figures 4 shows the differential capacitance–voltage

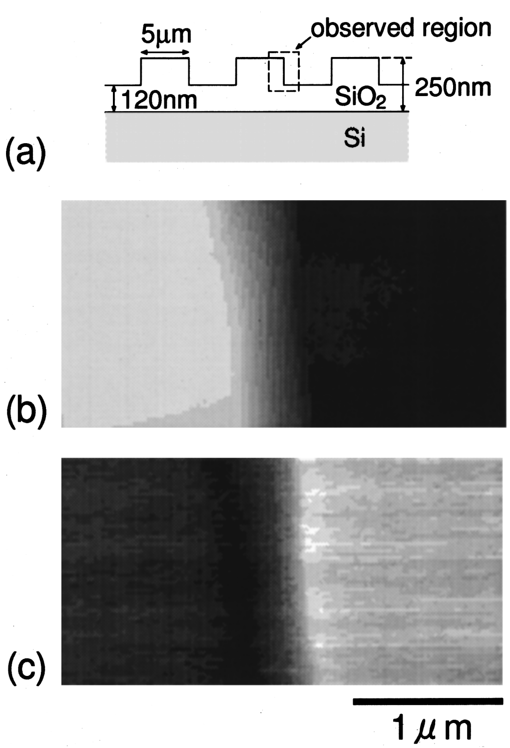

FIG. 3. (a) Cross section of the SiO_2/Si sample. (b) Topographic and (c) capacitive images of the sample.

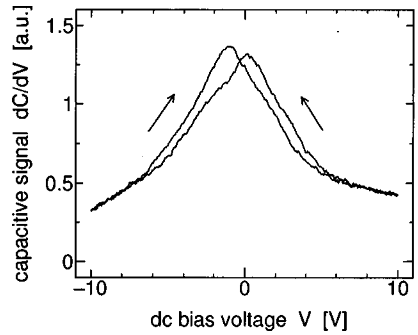

FIG. 4. $dC/dV-V$ curve for the PMMA/Si sample.

($dC/dV-V$) curve for a 80-nm-thick polymethylmethacrylate (PMMA) film on the same Si wafer as in the above experiment. The measurement was made in contact mode. The ac bias voltage was 2 V_{p-p} at 100 kHz. The measurement time for the curve was 3 s. As shown in Fig. 4, the $dC/dV-V$ curve exhibits hysteresis, i.e., a horizontal shift, which shows that charges were moved from the tip to the film and trapped by the film.[14] The charges tunnel through the thin (native) oxide on the Si tip as in a nitride–oxide–silicon structure.[4,6] The curve shift depends on the magnitude and duration of the applied voltage. Figure 5 shows a surface potential image for the same sample obtained after pulsed voltages were applied to it with the tip in contact with the sample. The voltages were 80 V. The pulse widths were 50 and 10 μs for the left and right marks, respectively. The written marks reflect the tip shape. They are not a result of surface contour changes, according to the simultaneously obtained topographic image. The ac bias voltage was 2 V_{p-p} at 100 kHz during the imaging. The dc bias voltage, which greatly changes the image contrast, was adjusted to a point where a peak capacitance signal was obtained in other regions than the marks. According to the image contrast and the curve in Fig. 4, the potential changes caused by writing the marks are estimated to be 1 V at most. As shown in Fig. 5, in addition, the two marks are different in size and signal strength. They are probably determined by the amount of trapped charges.

The lateral resolution of the proposed probe microscopy is determined by the tip size and the depletion area at the tip. For a sufficiently sharp tip, the depletion area can be further reduced by increasing the dopant density of the tip. An interesting way to improve the lateral resolution is to confine the lateral spreading of the depletion area by setting the dop-

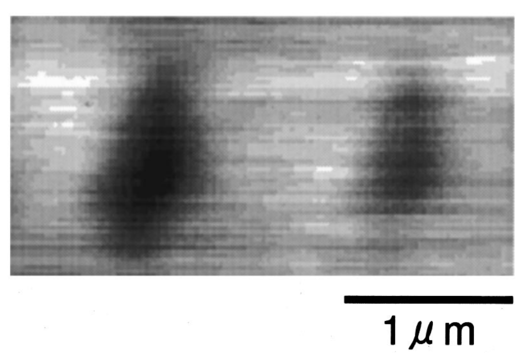

FIG. 5. Surface potential image of the PMMA film obtained after the charge injection with the Si tip.

ant density of the tip low at the apex and very high around it.[4] This technique enables one to improve the lateral resolution of a dull tip. For such applications as charge injection recording, which in fact our work is aimed at, the sample is flat and such a dull tip can be used without a serious problem, and may even be desirable in terms of durability. This fact still holds if the MIS diode is replaced by a MIS transistor sensor.[15] The use of a MIS transistor has an advantage that the sensitivity is not reduced with the sensing area, because the MIS transistor is consistent with the scaling law, according to which the source-drain resistance, which determines the output, does not change with the reduction of the transistor size. Furthermore, dc mode field sensing could be possible, whereby the sensing speed is improved and the measurement setup is simplified. It is believed that a MIS transistor with the sub-100-nm sensing region can be integrated with a tip. Actually, MOS transistors with the gate length of less than 100 nm have been reported.[16]

In conclusion, we have introduced a semiconductor tip to the SCM. A Si cantilever was used to detect local fields through depletion of carriers at the sharp end. The proposed microscopy has been successfully employed to image the local capacitance and the surface potential of insulator/electrode structures in contact mode. This technique is promising for the use in high-speed observation of electronic devices and in charge injection memory.

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