1/f Noise Suppression of pMOSFETs Fabricated on Si(100) and Si(110) Using an Alkali-Free Cleaning Process

$1/f$ Noise Suppression of pMOSFETs Fabricated on Si(100) and Si(110) Using an Alkali-Free Cleaning Process

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***Abstract*—This paper reports that the low-frequency noise in p-channel MOSFETs fabricated on (110) and (100) crystallographic oriented silicon is related to the microroughness of the silicon surface. Since the conventional RCA cleaning process makes the surface rough, especially in the case of (110) orientation, the authors developed the so-called 5-step room temperature cleaning process that does not use alkaline solution. The combination of this new cleaning process with the microwave-excited high-density plasma oxidation process for the formation of the gate oxide, instead of the standard 900 °C thermal oxidation process, leads to a reduction of the microroughness and a drop in the $1/f$ noise level of more than one decade. Furthermore, this reduction is not only observed for the (110) orientation but also seen, albeit to a much lesser extent, for (100) if it is treated in the same way.**

***Index Terms*—Cleaning process, MOS transistor, silicon, surface microroughness, surface orientation, $1/f$ noise.**

I. Introduction

NOISE is a limiting factor for all electronic devices, especially for analog and RF circuits. Actually, a signal that is too weak will not be transmitted because it is shrouded in the intrinsic device noise floor. For decades, researchers have studied and simulated noise [1]–[10] in order to understand its origin and to suppress it. Among the several types of electronic noise, the one attracting the largest attention of researchers now is low frequency noise, which is also called $1/f$ noise. In recent years, with the continuous and drastic reduction in device feature size, low frequency noise is irreparably increasing. Its suppression or hypothetically its complete eradication is of prime importance for the development of new devices and circuits. This would lead the electronic world into a new era of ultra-low power consumption devices handling very small signals.

The origin of the $1/f$ noise has not yet been understood and is still being discussed within the scientific community [7]–[10]. However, even if the schools of thought are in agreement that $1/f$ noise can be explained by the fluctuation of conductivity, one school attributes this noise to a bulk phenomenon induced by the mobility fluctuation in the lattice [7], while the other school explains it by the fluctuation in the number of carriers caused by interface traps [8]. During the 1990s, a third theory was developed that is a combination of both of the above models that included mobility and number fluctuations [9], [10].

In the quest for the realization of future high-speed analog and digital circuits, the improvement of the working frequency and the reduction of the signal/noise ratio are two of the parameters of prime importance. Although the current drivability of pMOSFETs fabricated on (110)-oriented silicon is 2.5 times larger than that on (100) [11]–[14], the $1/f$ noise level is still too high to establish it as a viable competitor or even a future replacement for the current CMOS technology on (100) silicon.

The alkaline solution used during the conventional RCA cleaning process before the fabrication of the gate oxide makes the silicon surface rough [15], [16]. This is especially true for (110) surfaces. Therefore, we have developed an alkali-free 5-step room temperature cleaning process [17] that produces a better quality surface that can be further processed to produce devices with suppressed low frequency noise levels.

The purpose of this paper is to show that the suppression of the $1/f$ noise in pMOSFETs can be achieved for (110) and (100) orientations due to the improvement in the microroughness resulting from the alkali-free cleaning process. Consequently, it is demonstrated that the $1/f$ noise is closely related to the quality of the Si/SiO_2 interface [18]. Furthermore, an even stronger reduction of the noise can be obtained when using the 5-step cleaning in combination with the microwave-excited high-density plasma oxidation process [19] for the fabrication of the gate oxide instead of the standard 900 °C thermal oxidation process. Also, it is worth noting that the suppression in the $1/f$ noise level is much more pronounced for the (110) orientation, meaning that the divide between the noise levels of (110) and (100) pMOSFETs has also been greatly reduced.

II. Experimental

Each step of the fabrication was carried out in the super clean room at Tohoku University. pMOSFETs fabricated on (100) and (110) silicon-oriented N-type wafers were employed for this experiment.

(100) and (110) surface p-channel transistors were fabricated using either alkali-free 5-step room temperature cleaning or, for comparison, RCA cleaning as the pregate oxidation cleaning method. Fig. 1 explains each step of the RCA cleaning process, which has a total of more than ten steps in which it is

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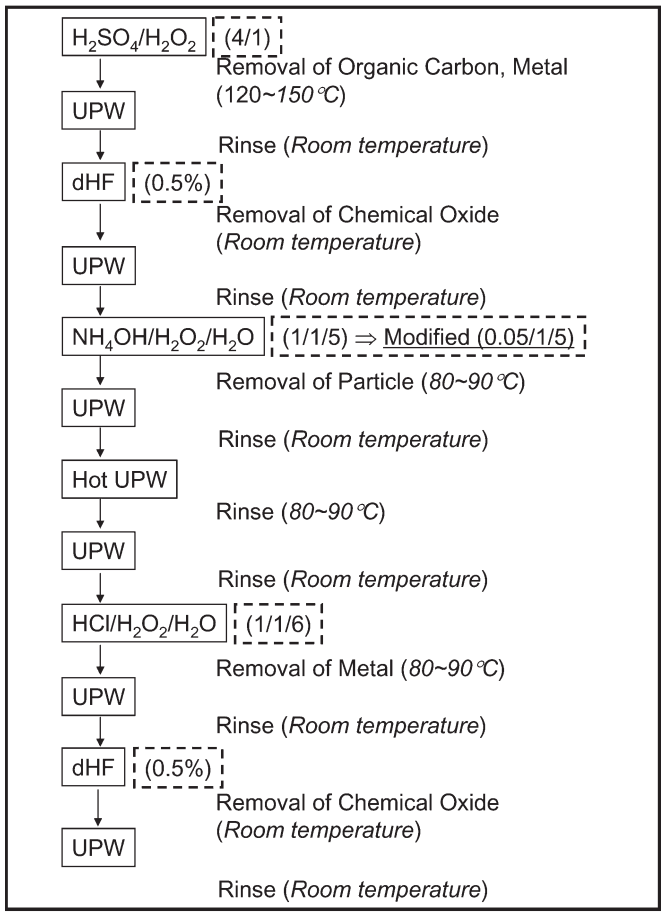

Fig. 1. Conventional RCA cleaning procedure with modifications [15], [16].

necessary to rinse after the use of each chemical. This means that the conventional RCA cleaning process is time consuming and is not environmentally friendly. Also, it cannot be carried out at room temperature.

A 5-nm-thick gate oxide was formed by using microwave-excited high-density plasma oxidation at 400 °C, or, for comparison, by using thermal oxidation at 900 °C. We used p-doped poly-silicon as the gate electrode.

Drain–current noise measurements were carried out using a Vector Signal Analyzer (AGILENT 89410 A) connected to a low-noise preamplifier (Princeton Applied Research 5184) with contacts directly taken on wafer. pMOSFETs were initially biased by a modular dc source (HP 4142 B) in order to find the target bias point parameters. This source was then replaced by an ultra-low noise dc source (SHIBASOKU PA14A1) for the final noise measurements. All transistors had low frequency $1/f^{\nu}$ noise with $1 < \nu < 1.1$ in the measurement range from 10 to 100 000 Hz.

III. Results and Discussion

As clearly shown in the $I_d - V_d$ curves in Fig. 2, the interesting feature of (110) pMOSFETs over (100) ones is current drivability, which is 2.5 times higher for the (110) orientation. Although this feature promises faster working frequencies, (110) CMOS digital and analog circuits may not be competitive without reducing its $1/f$ noise. As we can see in Fig. 3, the noise level of (110) pMOSFETs in the saturated regime is still nearly two decades higher when the devices were fabricated through the conventional RCA cleaning as compared with the one of (100) pMOSFETs, and this level must be severely reduced.

As a replacement for RCA cleaning, we developed the alkali-free 5-step room temperature cleaning process. As explained in Fig. 4, this new technique has a very simple procedure, with only one rinse at the end of the cleaning. Further, it can be carried out without any temperature elevation in less than 5 min.

The impact of this new cleaning method on (110)-oriented surface quality is obvious when compared with the RCA cleaning as shown in the results obtained from the scanning tunneling microscope (STM) analysis presented in Table I. The improvement in surface quality when using the 5-step cleaning is found to be around 30% in the average microroughness (Ra) and in peak to valley height (P–V). As noted previously, in addition to the numerous steps and high temperature involved in RCA cleaning, a further problem is that it requires the use of an alkali solution, which leads to the anisotropic removal of silicon atoms from the surface, resulting in greater surface roughness. This occurs because bond cleavage leads to the formation of (111)-oriented microstructured inhomogeneities at the surface that build up over time. On the contrary, the 5-step cleaning is an alkali-free process, which produces a smoother homogeneous surface.

The evaluation of the impact of the 5-step cleaning on $1/f$ noise in (110) pMOSFETs was carried out for two different oxidation processes. The results of noise measurement are presented in Fig. 5 for $V_d = -2$ V, and in Fig. 6 for $V_d = -100$ mV. In both cases, we observed that the alkali-free cleaning process gave a pronounced improvement in the $1/f$ noise level, which decreased by almost two decades compared to the RCA cleaning method. This is due to the formation of a surface with reduced microroughness compared to that obtained with RCA cleaning. It was also found that plasma oxidation results in a lower noise level than achieved from thermal oxidation.

After the successful demonstration of $1/f$ noise suppression in (110) pMOSFETs, for comparison, the same evaluation process was carried out for the (100) silicon-oriented wafers. The results of the STM analysis are presented in Table II. When comparing the results within Table II, it is obvious that the use of the alkali-free 5-step cleaning again results in an improvement in surface quality. However, the surface quality improvement for the (100) orientation was only 10% in the microroughness when changing from the RCA cleaning to the 5-step cleaning process compared with the 30% improvement seen for the (110) surface in Table I. This result indicates that the (100) silicon surface is more resistant to the alkaline solution than the (110) silicon surface. In summary, the comparison of Tables I and II shows us that the use of the RCA cleaning process on a (110) silicon surface leads to inferior quality in terms of microroughness than when the processing is carried out on the (100) orientation. This degradation of the interface can be explained by the fact that the alkali solution etching rate on (110) surfaces is faster than on (100) [20]. Most importantly, for both orientations, the use of the RCA cleaning method

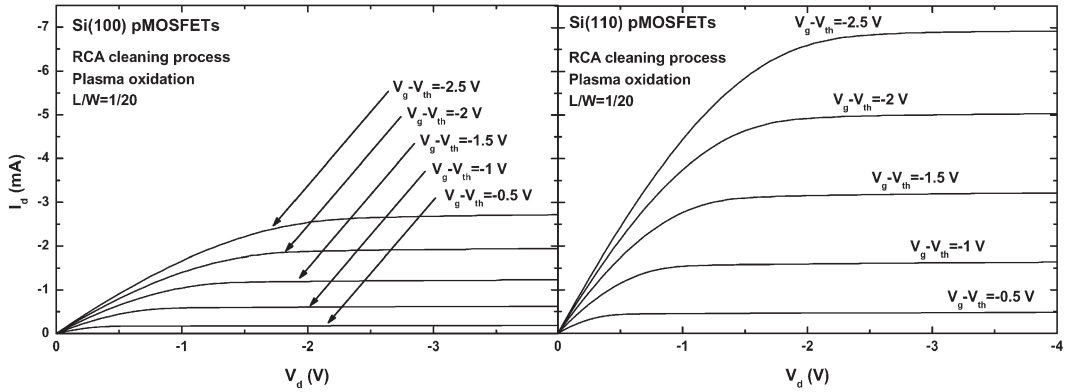

Fig. 2. $I_d - V_d$ characteristics of (100) and (110) pMOSFETs for different gate overdrive voltages [13].

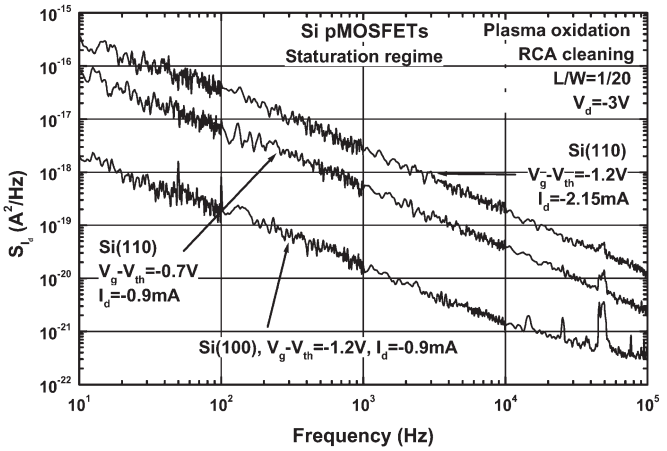

Fig. 3. Comparison of spectral density in drain–current of pMOSFETs based on (100) and (110) for a same drain–current or the same gate overdrive voltage in the saturated regime when conventional RCA cleaning is used. The (100) pMOSFET is taken as reference.

deteriorated the quality of the initial interface whereas the 5-step cleaning improved it.

The results of $1/f$ noise measurements on (100) pMOSFETs, using the same procedure described for (110) pMOSFETs, are presented for $V_d = -2$ V and $V_d = -100$ mV, respectively, in Figs. 7 and 8. In this case, for both operating conditions, by simply changing the pregate formation cleaning process to the alkali-free 5-step method, the $1/f$ noise level was again reduced but in less proportion than for the (110) surfaces. Further decreases in $1/f$ noise could be achieved if we used the plasma oxidation method.

In summary, when fabricated through the conventional RCA cleaning method, (110) pMOSFETs had far higher $1/f$ noise levels than (100) pMOSFETs, but this seems to be simply the result of the evolution in the processing methodologies and not an intrinsic property of the surfaces, since by simply replacing the RCA cleaning method with the alkali-free 5-step room temperature method the divide in $1/f$ noise level between both orientations can be greatly reduced as shown in Fig. 9.

Also evident from the data presented here is that the choice of the oxidation process used in the fabrication of the gate oxide can also play an important role in reducing $1/f$ noise. Plasma oxidation yields better results than thermal oxidation in term of electronic noise. In fact, the first advantage of plasma oxidation

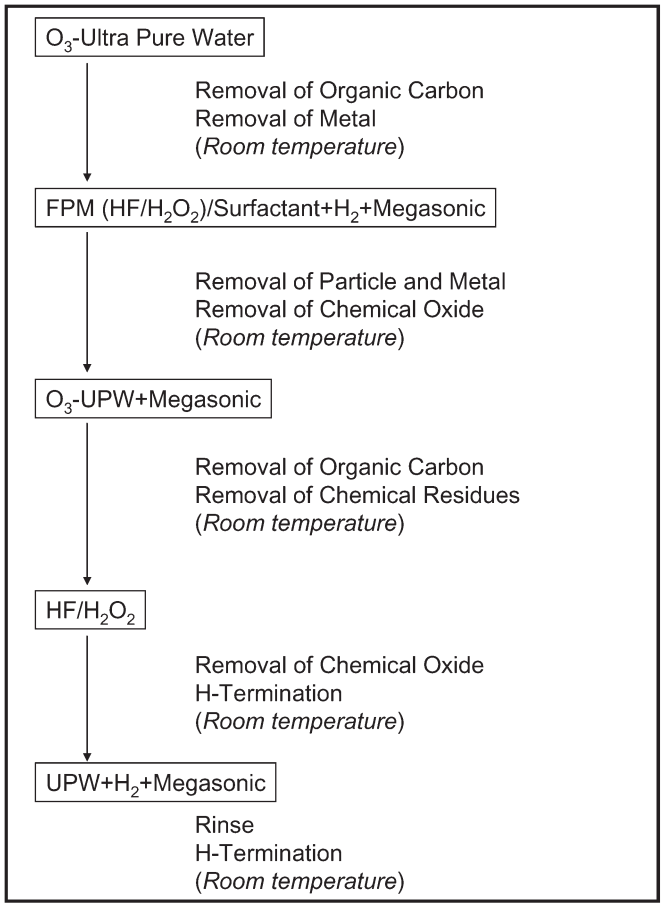

Fig. 4. Procedure of the alkali-free 5-step room temperature cleaning [17].

TABLE I
STM PARAMETERS: Ra (MICROROUGHNESS) AND P–V (PEAK–VALLEY MAXIMUM AMPLITUDE) OF A (110)-ORIENTED SILICON SURFACE BEFORE AND AFTER THE CLEANING PROCESS

Si(110) surface	Ra (nm)	P-V (nm)
Reference (before cleaning)	0.114	1.314
After 5-step cleaning	0.113	1.244
After RCA cleaning	0.144	1.779

over thermal oxidation comes from an improvement in interface trap density [21]. In Fig. 10, we show the interface trap density achieved for different oxidation processes for all three primitive

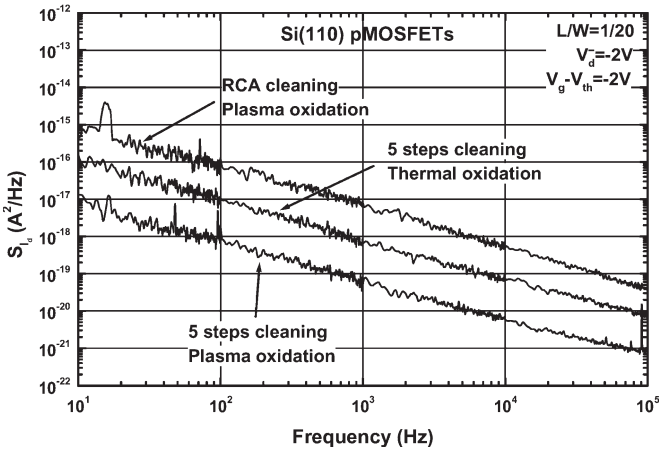

Fig. 5. Spectral density in the drain–current of different (110) pMOSFETs as a functions of several combinations of cleaning and oxidation processes for $V_d = -2$ V and $V_g - V_{\rm th} = -2$ V.

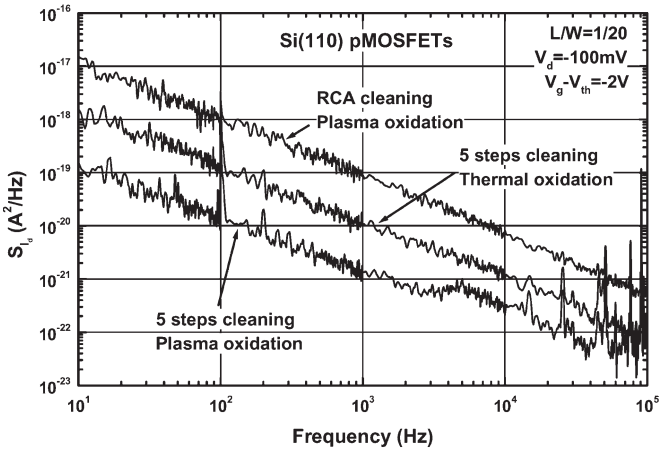

Fig. 6. Spectral density in the drain–current of different (110) pMOSFETs as a function of several combinations of cleaning and oxidation processes in the linear regime.

TABLE II
STM PARAMETERS: Ra (MICROROUGHNESS) AND P–V (PEAK–VALLEY MAXIMUM AMPLITUDE) OF A (100)-ORIENTED SILICON SURFACE BEFORE AND AFTER THE CLEANING PROCESS

Si(100) surface	Ra (nm)	P-V (nm)
Reference (before cleaning)	0.102	1.154
After 5-step cleaning	0.099	1.094
After RCA cleaning	0.108	1.19

orientations. From this figure, it is evident that, regardless of the orientation, the use of plasma oxidation reduces the interface trap density. Furthermore, its impact is much more pronounced for (111) and (110) orientations than for (100). The reduction is found to be around 60% for the (100) orientation compared to 85% for the (110) orientation. In addition to the lower interface trap density, the second advantage in using the plasma process for gate oxide fabrication comes from the fact that it has a uniform growth rate. As shown in Fig. 11, while the oxidation rate strongly depends on the surface orientation when it is thermally induced, the oxidation rate becomes independent of the surface orientation when plasma oxidation is employed for the

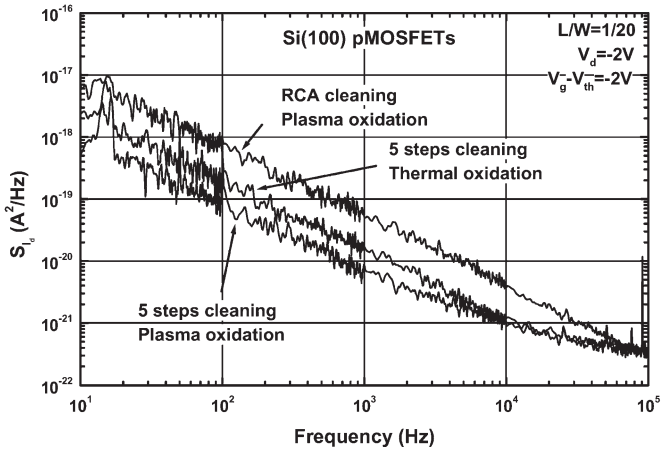

Fig. 7. Spectral density in the drain–current of different (100) pMOSFETs as a function of several combinations of cleaning and oxidation processes for $V_d = -2$ V and $V_g - V_{\rm th} = -2$ V.

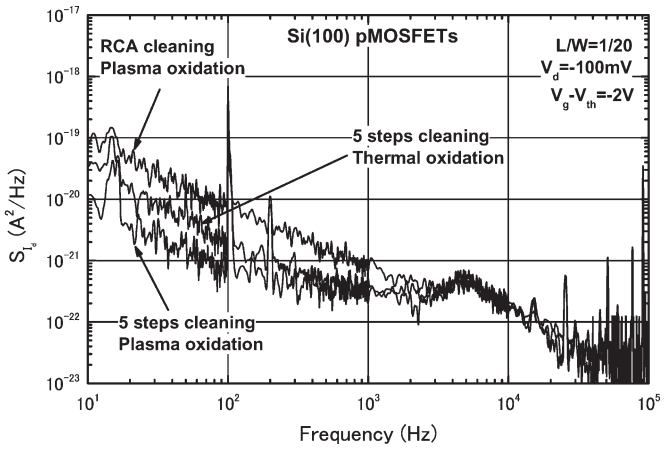

Fig. 8. Spectral density in the drain–current of different (100) pMOSFETs as a function of several combinations of cleaning and oxidation processes in the linear regime.

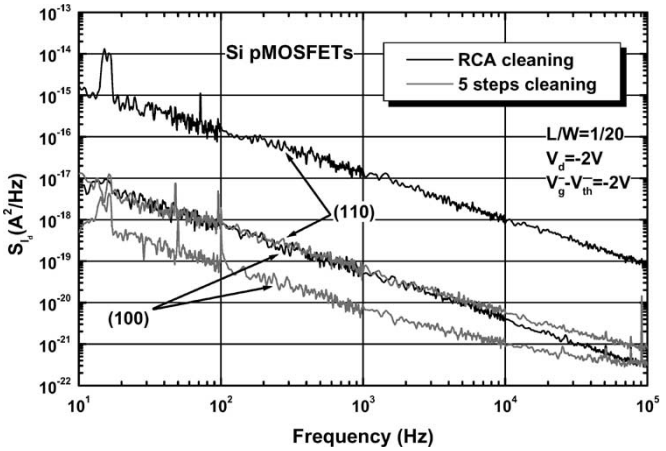

Fig. 9. Improvement and decrease of the noise level divide between (110) and (100) pMOSFETs when the pregate cleaning process is changed from the RCA one to the 5-step one.

formation of thin oxides [14]. As a result, the amplification of (111) microsurface inhomogeneities, in terms of surface roughness, will tend to increase when using the alkaline solution,

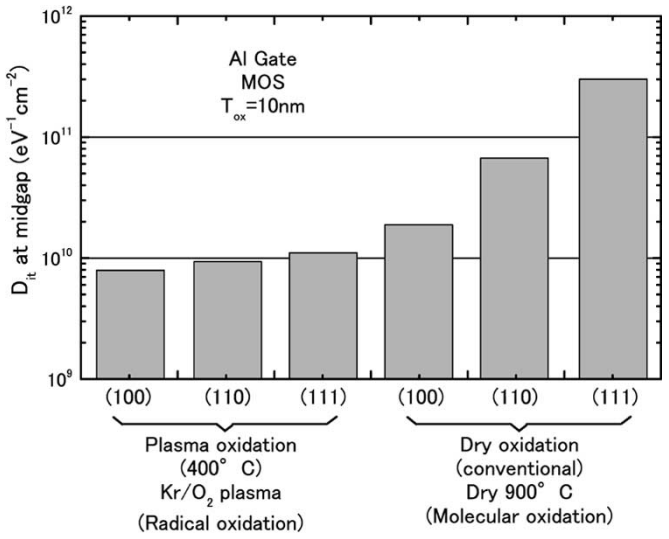

Fig. 10. Interface trap density at midgap for the three main silicon crystallographic orientations when the gate oxide is fabricated with the plasma process or the thermal process [21].

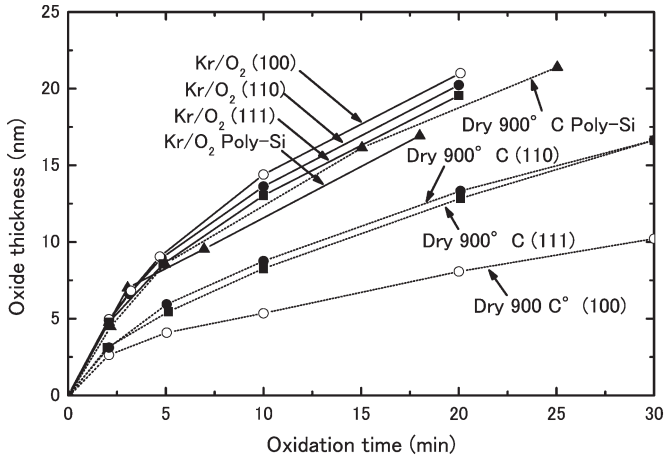

Fig. 11. Oxidation growth rate for the three main silicon crystallographic orientations as a function of the oxidation process [14].

used in RCA cleaning. In contrast, for plasma oxidation, since the growth rate is independent of the orientation of the surface, rough interfaces with (111) defects will tend be flatter with time, resulting in a more uniform and smoother interface.

The significant change in noise level has its origin in the cleaning process and the resulting surface quality, and in particular the change in the microroughness. In turn, this can be attributed to the increased degradation of the (110) surface, caused by the alkaline solution used during the RCA cleaning compared to the lower degradation of the (100) surface under the same conditions. Thus, the choice of the cleaning method can have a significant effect, which may be amplified, in terms of the interface quality and the resulting $1/f$ noise level during the gate formation step. This will be especially true in the case of thermal oxidation.

IV. Conclusion

The interface microroughness at the Si/SiO_2 interface and the $1/f$ noise in different pMOSFETs have been studied. We successfully demonstrated that the combination of alkali-free 5-step room temperature cleaning and plasma oxidation processes leads to significantly suppressed $1/f$ noise levels due to the formation of a smoother interface and a more uniform oxide layer. The advantage of (100) pMOSFETs over (110) pMOSFETs, in terms of the $1/f$ noise level, has been reduced so much that, considering the improved drivability of (110) pMOSFETs, the (110) CMOS can establish itself as a viable competitor or even a future replacement for the current silicon CMOS technology which only uses (100)-oriented surface.

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Tadahiro Ohmi (M'81–SM'01–F'03) was born in Tokyo, Japan, on 1939. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Tokyo Institute of Technology, Tokyo, in 1961, 1963, and 1966, respectively.

Prior to 1972, he was a Research Associate at the Department of Electronics, Tokyo Institute of Technology, where he worked on Gunn diodes such as velocity overshoot phenomena, multivalley diffusion, and frequency limitation of negative differential mobility due to an electron transfer in the multivalleys, high-field transport in semiconductor such as unified theory of space charge dynamics in negative differential mobility materials, Bloch oscillation-induced negative mobility and Bloch oscillators, and dynamics in injection lasers. In 1972, he moved to Tohoku University, Sendai, Japan, and is currently a Professor at the New Industry Creation Hatchery Center. His research activities are summarized as 2000 original papers and 1800 patent applications. He is currently engaged in researches on high-performance ultralarge scale integration (ULSI) free from gate and drain leakage currents, threshold voltage fluctuations of MOS transistors, and $1/f$ noises by introducing Si(110) surface directly nitrided Si3N4 gate insulator as a high-k gate dielectric nonporous fluorocarbon film having a dielectric constant of less than 1.90 as an intermetallic dielectric. He is also studying metal substrate silicon-on-insulator ULSI and large sized flat-panel displays (FPDs). Advanced semiconductor and FPD process technologies such as the radical reaction-based semiconductor and FPD manufacturing based on the microwave-excited very low-electron temperature high density plasma free from change up damages and bombarding ion induced damages are also being studied.

Dr. Ohmi is a member of the Institute of Electronics, Information and Communication Engineers of Japan (IEICE, Fellow), the Japan Society of Applied Physics, the Electrochemical Society (ECS). He received the Ichimura Award in 1979, the Inoue Harushige Award in 1989, the Best Paper Award of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING in 1989, the Ichimura Prizes in Industry-Meritorious Achievement Prize in 1990, the Okouchi Memorial Technology Prize in 1991, The Minister of State for Science and Technology Award for the promotion of invention 1993, the Invention Prize and 4th International Conference on Soft Computing (IIZKA'96) Best Paper Award in 1996, the IEICE Achievement Award in 1997, the Werner Kern Award in 2001, and the ECS Electronics Division Award, the Medal with Purple Ribbon from Government of Japan, and the Best Collaboration Award (the Prime Minister's Award) in 2003.