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Article

The Implementation of Active Power Filter using Proportional plus Resonant Controller

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Abstract. This paper presents the harmonic elimination using an active power filter (APF) for three-phase system. The design and performance comparison study of the compensating current controllers are explained. The performance of the PI controller and the proportional plus resonant (P+RES) controller are compared in the paper. Moreover, the hardware implementation of the considered system is also presented in this paper. For the experimental results, the P+RES controller can provide a good performance to control the compensating current compared with using the PI controller.

Keywords: Harmonic elimination, active power filter, PI controller, proportional plus resonant controller.

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1. Introduction

Power quality problems have an effect on the domestic and industrial electric systems. The harmonics are a part of the serious problems. The voltage source connected nonlinear loads can generate the harmonics into the electric systems. These harmonics cause many disadvantages [1-8] such as loss in transmission lines and electric devices, protective device failures, measuring instrument malfunction and short-life electronic equipment in the system. Nowadays, there are several nonlinear loads. These loads can suddenly change. Therefore, the active power filter (APF) is used in the paper. The APF can provide the efficiency and flexibility [9-11] for the harmonic elimination.

The harmonic elimination system using the APF is shown in Fig. 1. From Fig. 1, there are four parts. In the first part, the considered power system is the balanced three-phase system. The second part is the APF topology [12]. In this paper, the three-leg split-capacitor topology [13, 14] is used to inject the compensating currents for harmonic elimination. The third part is the harmonic identification by using DQF method [15]. The last part is the control strategy. The aim of this paper is the performance improvement of the compensating current controller. Because it is significant to achieve the good performance for harmonic elimination. This paper presents the performance comparison of the compensating current controllers. The proportional plus resonant (P+RES) controller [16, 17] is considered to compare the performance with the proportional integral (PI) controller [18]. These controllers provide a small tracking error in steady state. However, when the non-linear load is changed, the P+RES controller can be adapted to control the compensating currents following on the significant harmonic orders in the system. Therefore, the P+RES controller can provide better results compared with PI controller.

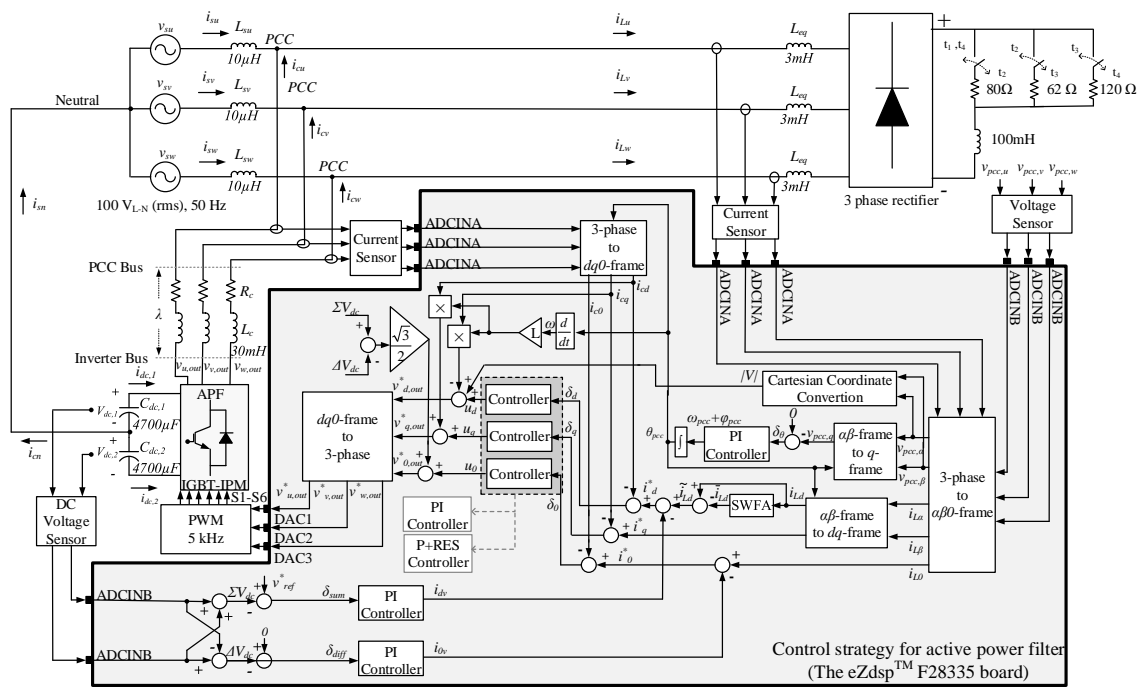


Fig. 1. Considered power system and control strategy.

This paper presents the implementation of APF in order to verify the performance comparison of the PI and P+RES controllers. From the literature reviews, the control strategy for APF can be implemented by analog circuits (one cycle control [19], PI control [20], quasi steady state control [21]) and digital techniques (adaptive linear element (Adaline) control [22], PI control [23], hysteresis control [24], fuzzy logic control [25], predictive control [26], one cycle control [27]). The advantages of analog circuits are fast computational time (no sampling time) and low cost. However, when the considered power system is changed, the control structure and parameters of analog circuits should be redesigned. Therefore, it is difficult and complicated. The design of control strategy is convenient and flexible to operate with the digital implementation. Moreover, the digital techniques provide a good control performance. In the paper, the proposed control strategy is performed by the digital signal processor (eZdsp™ F28335).

The paper is structured as follows. The design of the PI and P+RES controllers are described in Section 2. The experimental setup is expressed in Section 3. In Section 4, the experimental results and discussion are also shown. Finally, Section 5 concludes the advantage of the P+RES controller.

2. The Compensating Current Control

2.1. The Design of The PI Controller

The discrete design approach [28] is used to design the PI controller. This approach is suitable for the digital control. The block diagram to design the PI controllers on $dq0$ -frame are illustrated in Fig. 2.

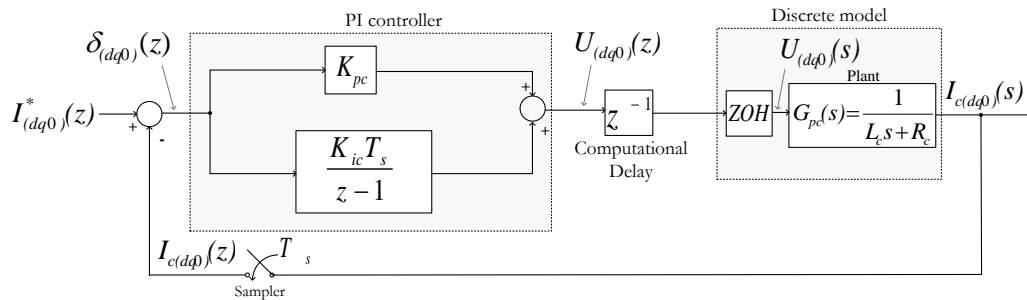


Fig. 2. The block diagram to design the PI controllers on $dq0$ -frame.

From the block diagram in Fig. 2, the closed-loop transfer function can be derived in Eq. (1). From Eq. (1), the parameters of α and K_{pc} are calculated by using the root-locus technique on Z-plane as shown in Fig. 3.

$$\frac{I_{(dq0)}(z)}{I_{(dq0)}^*(z)} = \frac{\left(\frac{K_{pc}}{R_c}\right)\left(1 - e^{-\frac{R_c T_s}{L_c}}\right)(z - \alpha)}{z^3 - \left(e^{-\frac{R_c T_s}{L_c}} + 1\right)z^2 + \left(e^{-\frac{R_c T_s}{L_c}} + \left(\frac{K_{pc}}{R_c}\right)\left(1 - e^{-\frac{R_c T_s}{L_c}}\right)\right)z - \left(\frac{K_{pc}}{R_c}\right)\left(1 - e^{-\frac{R_c T_s}{L_c}}\right)\alpha} \quad (1)$$

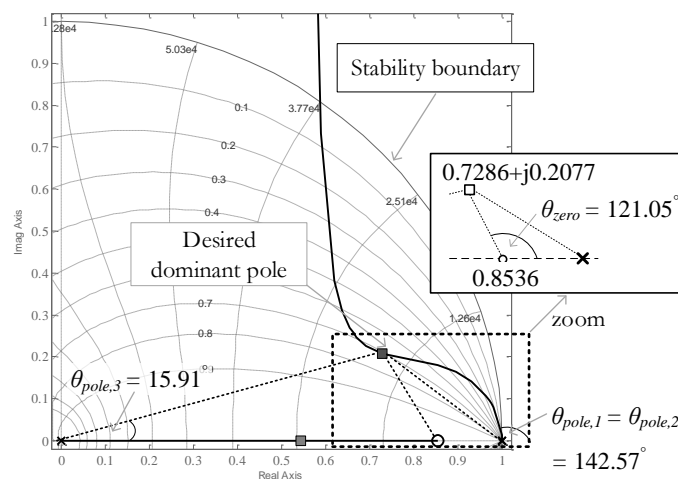


Fig. 3. The root – locus of the compensating current control.

The desired dominant pole can be calculated in Eq. (2). The sampling time (T_s) and damping ratio (ζ) are defined to 25 μ s and 0.7, respectively. The range of the considered harmonic frequencies for the compensating current control is 2500 Hz (50 harmonic orders). Therefore, the bandwidth of the current loops control (ω_{ni}) are equal to 15.71 rad/s.

$$z = e^{T_s(-\zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2})} = 0.7286 \pm j0.2077 \tag{2}$$

For $\alpha = 0.8536$ and $K_{pc} = 262.66$, the appropriate PI controller parameters are $K_{pc} = 262.66$, $K_i = 1.54 \times 10^6$. The details of the PI controller design can be found in the previous publications [18].

2.2. The Design of The Proportional plus Resonant Controller

The P+RES controller is developed from the PI controller [16]. The block diagram considered the discrete design approach is depicted in Fig. 4. From Fig. 4, the root locus can be explained by using the closed-loop transfer function in Eq. (2). The placement of poles and zero on Z-plane are shown in Fig. 5. The poles of the closed-loop transfer function in Eq. (2) must be located in the stability boundary (unit circle on Z-plane).

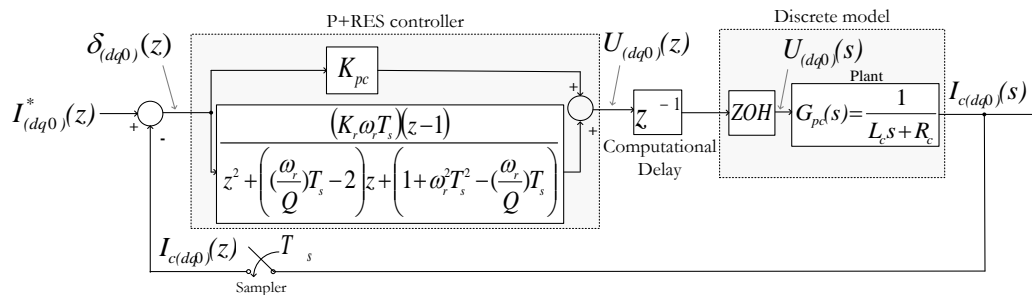


Fig. 4. The block diagram to design the P+RES controllers on dq0-frame.

$$\frac{I_{(dq0)}(z)}{I_{(dq0)}^*(z)} = \frac{\frac{K_{pc}L_c}{T_s} \left(z^2 + \left(B + \frac{A}{K_{pc}} \right) z + \left(C - \frac{A}{K_{pc}} \right) \right)}{z^4 + (B-1)z^3 + \left(\frac{K_{pc}L_c}{T_s} + C - B \right) z^2 + \left(\frac{K_{pc}L_c}{T_s} B + \frac{L_c}{T_s} A - C \right) z + \left(\frac{K_{pc}L_c}{T_s} C - \frac{L_c}{T_s} A \right)} \tag{2}$$

where $A = K_r \omega_r T_s$, $B = (\omega_r / Q) T_s - 2$, $C = 1 + \omega_r^2 T_s^2 - (\omega_r / Q) T_s$

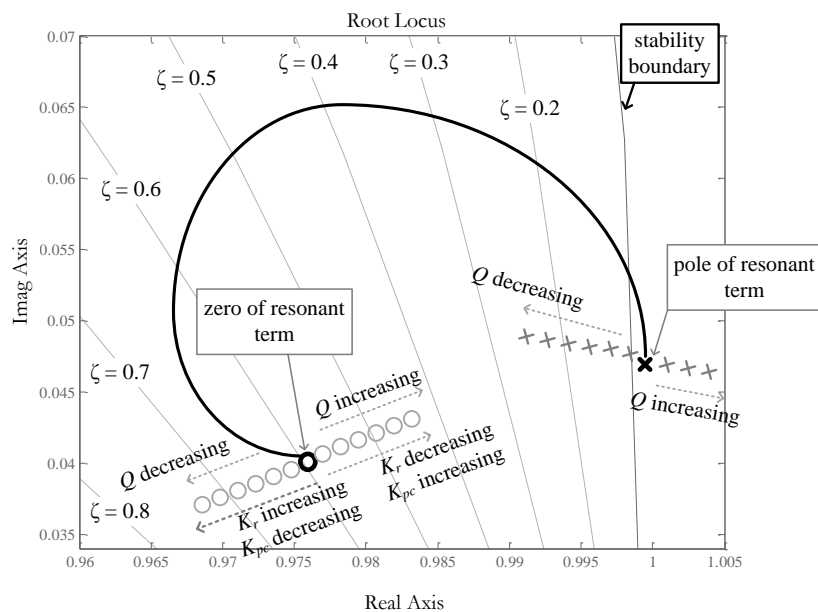


Fig. 5. The placement of zero and pole on Z-plane.

The parameters of the P+RES controller consist of the proportional gain (K_{pc}), the gain of resonant term (K_r), the resonant frequency (ω_r) and the quality factor (Q). The resonant frequency (ω_r) in the P+RES controllers can be adjusted depending on the significant harmonic frequency on $dq0$ -frame. The spectra of the reference currents on $dq0$ -frame (i_d^*, i_q^*, i_0^*) are shown in Fig. 6. Therefore, the ω_{rd} , ω_{rq} and ω_{r0} are set to $2\pi \times 300$, $2\pi \times 300$ and 0 rad/s, respectively.

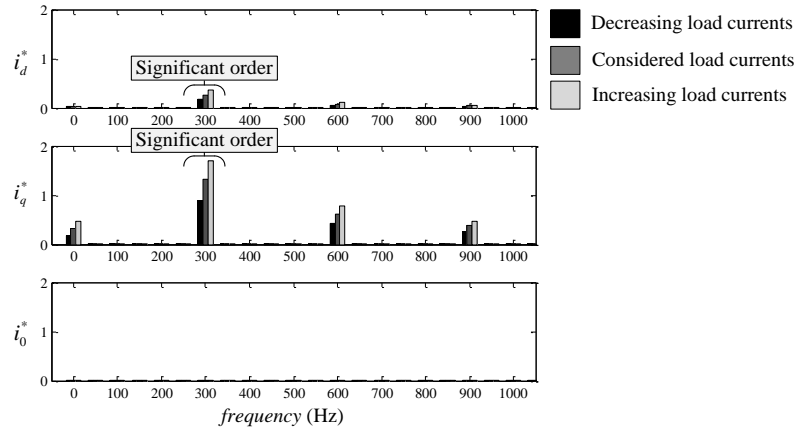


Fig. 6. The spectra of the reference currents on $dq0$ -frame.

For example on dq -axis ($\omega_r = 2\pi \times 300$ rad/s), the K_{pc} and K_r are designed depending on specific values ($\omega_{ni} = 2\pi \times 300$ rad/s, $\zeta = 0.7$). The root locus technique on Z-plane is used to obtain the desired dominant pole. ($K_{pc} = 414$, $K_r = 517.5$) as shown in Fig. 7.

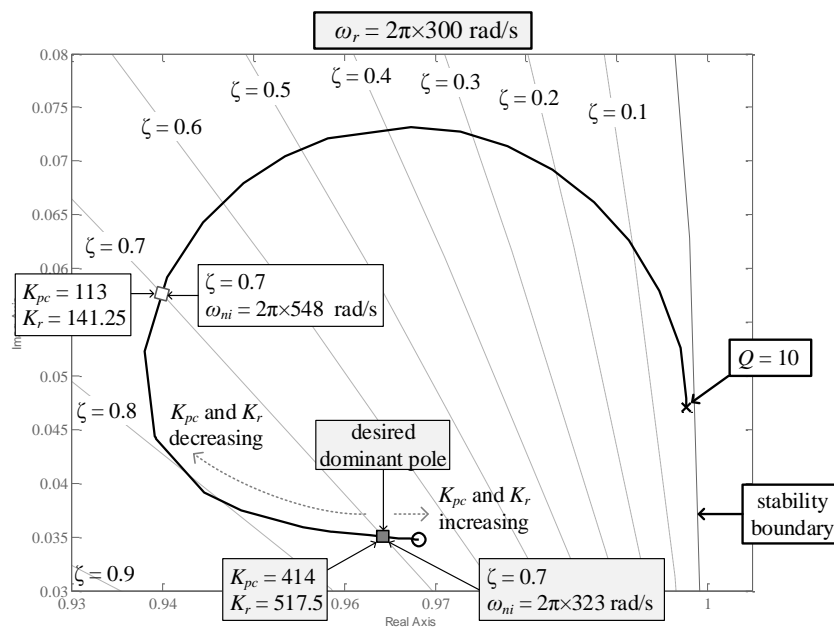


Fig. 7. The criteria for designing K_{pc} and K_r .

The characteristic of quality factor (Q) is shown in Fig. 7. The Q can be calculated by Eq. (3). From this equation, the f_r , f_H and f_L are the resonant, high and low frequencies, respectively. The suitable Q

should be selected in the boundary as shown in Eq. (4). The boundary of Q in this case is $1.5 < Q < 150$. Therefore, The Q is defined to 10 ($f_r = 300$ Hz, $f_H = 315$ Hz, $f_L = 285$ Hz). Moreover, according to Fig. 7, the pole of resonant term at $Q = 10$ is located in the stable region.

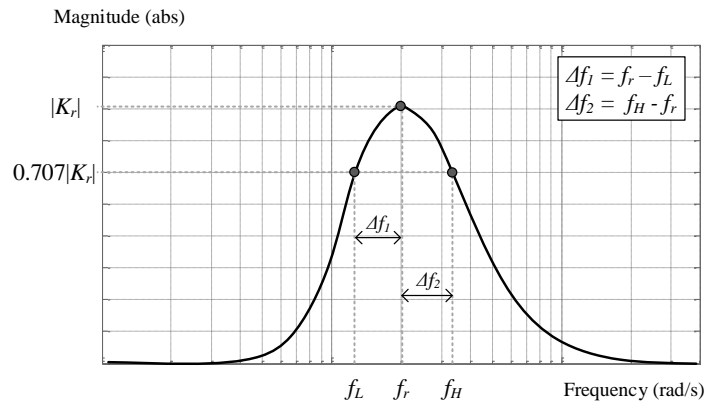


Fig. 8. The characteristic of quality factor (Q).

$$Q = \frac{f_r}{f_H - f_L} \quad (3)$$

$$Q_{\min} < Q < Q_{\max} \quad (4)$$

$$\text{where } Q_{\min} = \frac{f_r}{\Delta f_2 - \Delta f_1} = \frac{f_r}{(f_r + 100) - (f_r - 100)} \text{ and } Q_{\max} = \frac{f_r}{\Delta f_2 - \Delta f_1} = \frac{f_r}{(f_r + 1) - (f_r - 1)}$$

3. Experimental Setup

The experimental setup for the harmonic elimination system using an APF consists of two main parts. The first part is the experimental rig as shown in Fig. 9. It can be seen in Fig. 9 that the experimental rig can be decomposed into four sections. The first section is the considered power system. The three-phase voltage source connected with the three-phase rectifiers is shown in number 1 to 5. The second section is the voltage/current sensors and signal conditioning circuits as shown in number 6. The PCC voltages ($v_{pcc,(uvw)}$) are measured by using the transformers ($220V_{ac} / 15V_{ac}$). The DC bus voltages ($V_{dc,1}, V_{dc,2}$) are measured by using the voltage transducers (LEM LV25-P). The load currents ($i_{L(uvw)}$) and compensating currents ($i_{c(uvw)}$) are measured by using the current transducers (LEM HX10-P). The range of all measured signals ($v_{pcc,(uvw)}, V_{dc,(1,2)}, i_{L(uvw)}, i_{c(uvw)}$) for the DSP board are adjusted by signal conditioning circuits. The third section is the control platform as shown in number 7 and 8. This section consists of three processes to generate the pulse signals (S1-S6). First, the host computer provides the user interface to the DSP board. The eZdsp™ F28335 board calculates the reference voltages of APF ($v_{(uvw),out}^*$) from the proposed control strategy. Second, the D/A converters (DAC712P) are used to transform the $v_{(uvw),out}^*$ from the digital signals to the analog signals. Third, the analog signals of $v_{(uvw),out}^*$ (reference signals) are sent to compare with the triangular carriers in PWM modulator. The pulse signals (S1-S6) from the PWM technique are sent to drive the insulated-gate bipolar transistors (IGBTs) of the APF. The fourth section is the APF topology as shown in number 9 to 11. The capacitors ($C_{dc,1} = C_{dc,2} = 4700 \mu F$) are connected with IGBT-Intelligent Power Module (IPM) (6MBP50RA-120) on the DC side. The APF inductances ($L_{c(uvw)} = 18$ mH) are connected with IGBT-IPM on the AC side. The APF injects the $i_{c(uvw)}$ into the considered power system at the PCC points (number 3).

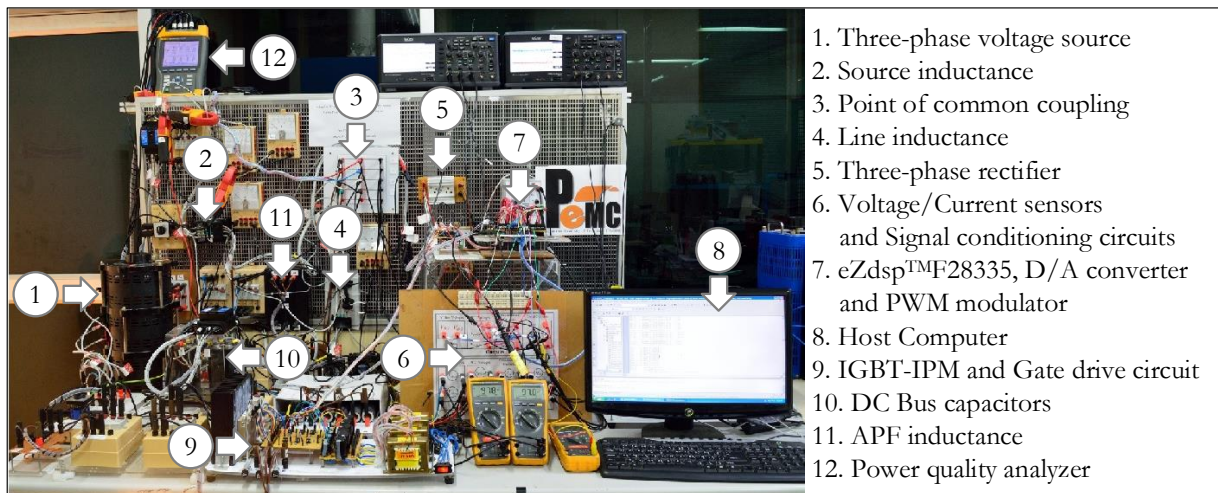


Fig. 9. The overall of experimental rig.

The second part is the software for the control of the APF. The code composer studio (CCS v3.3) is used to program on eZdsp F28335 board. The overall flowchart to control the APF can be described in Fig. 10. The phase locked loop algorithm, the DQF harmonic detection, the DC bus voltage control (PI), the compensating current control (PI, P+RES) and control strategy on $dq0$ -axis are written in C programming languages by using the CCS v3.3.

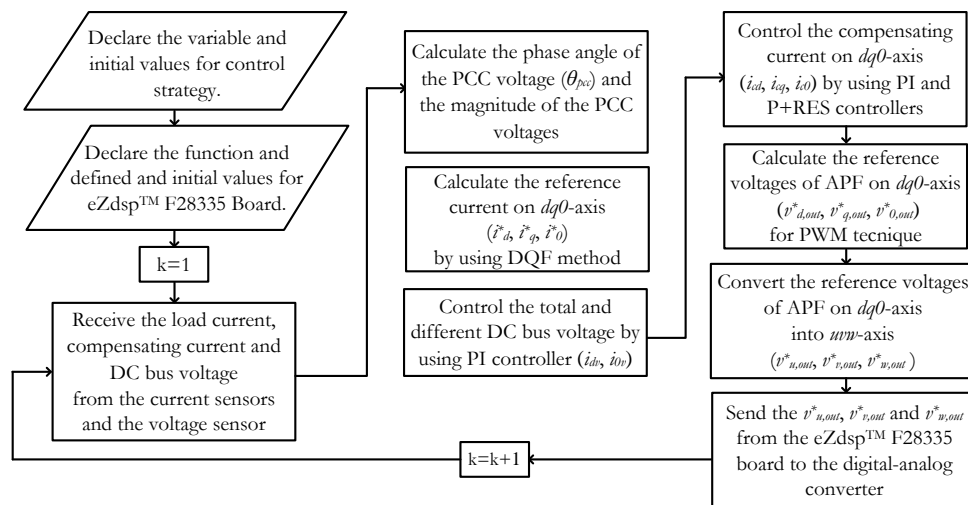


Fig. 10. Flowchart of the harmonic identification and control strategy.

4. Experimental Results and Discussion

The harmonic identification and control strategy in Fig. 1 are supported by the hardware implementation. The APF parameters are designed following on the previous researches [29, 30]. The harmonic elimination results for the balanced three-phase system are depicted in Fig. 11–12.

The performance of the proposed controller for harmonic elimination using the APF are tested with three load conditions. The first load condition is the amplitude of load currents at $2 A_{(peak)}$ ($R_L=120 \Omega$, $L_L=0.1H$). The second load condition is the amplitude of load currents at $3 A_{(peak)}$ ($R_L=80 \Omega$, $L_L=0.1H$). The third load condition is the amplitude of load currents at $4 A_{(peak)}$ ($R_L=62 \Omega$, $L_L=0.1H$).

The testing results of the harmonic elimination using a PI controller in Fig. 11 (a)-(c) show that this controller can control the compensating current even though the load is dynamic condition. From Fig. 11 (a)-(c), the load currents (i_{Lu} , i_{Lv} , i_{Lw}) before compensation are highly distorted waveform. The average total

harmonic distortion ($\%THD_{av}$) of this current is equal to 29.3 %, as shown in Fig. 13 (a). After compensation, the APF injects the compensating current (i_{cu}, i_{cv}, i_{cw}) into the considered power system at a PCC point. The source currents after compensation (i_{su}, i_{sv}, i_{sw}) are nearly sinusoidal waveform. The $\%THD_{av}$ is equal to 10.66 %, as shown in Fig. 13 (b). According to Fig. 11(a)-(b), for the dynamic load testing, when the non-linear load resistor (R_L) is changed from 120Ω to 80Ω and 80Ω to 62Ω , the waveforms of $i_{s(uvw)}$ after compensation are oscillating sinusoidal waveform. The peak amplitude of i_{su} is equal to $5.80 A_{(peak)}$ ($4.10 A_{(rms)}$) and $7.35 A_{(peak)}$ ($5.20 A_{(rms)}$), respectively. In the steady state condition, the i_{su} is constant at $4.20 A_{(peak)}$ ($2.97 A_{(rms)}$) and $4.95 A_{(peak)}$ ($3.5 A_{(rms)}$), respectively. From Fig. 11(d), the total DC bus voltage loop control can regulate the total DC bus voltage ($\sum V_{dc}$) following on the total DC bus voltage reference ($\sum V_{dc}^*$) even though the loads are varied. It can be seen from Fig. 11(d) that the $V_{dc,1}$ and $V_{dc,2}$ are equal to 120 V. Therefore, the $\sum V_{dc}$ is constant at 240 V. The results in Fig. 11(d) confirm that the PI controllers of the DC bus voltage control provide good performance.

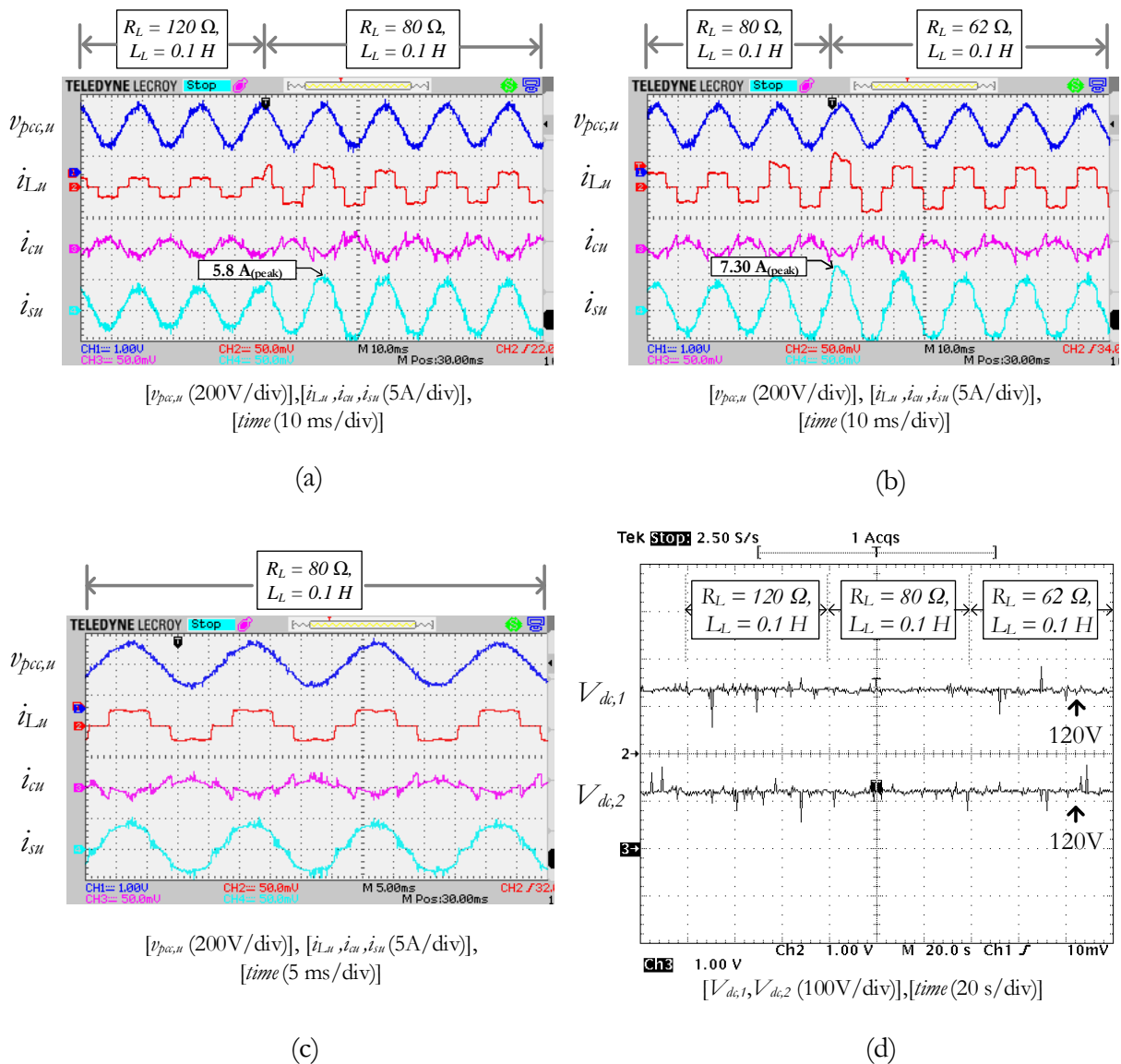


Fig. 11. The testing results of harmonic elimination with PI controller. (a) The peak amplitude of load current changing from $2 A_{(peak)}$ to $3 A_{(peak)}$, (b) The peak amplitude of load current changing from $3 A_{(peak)}$ to $4 A_{(peak)}$, (c) The amplitude of load currents at $3 A_{(peak)}$, (d) The performance of the DC bus voltage control.

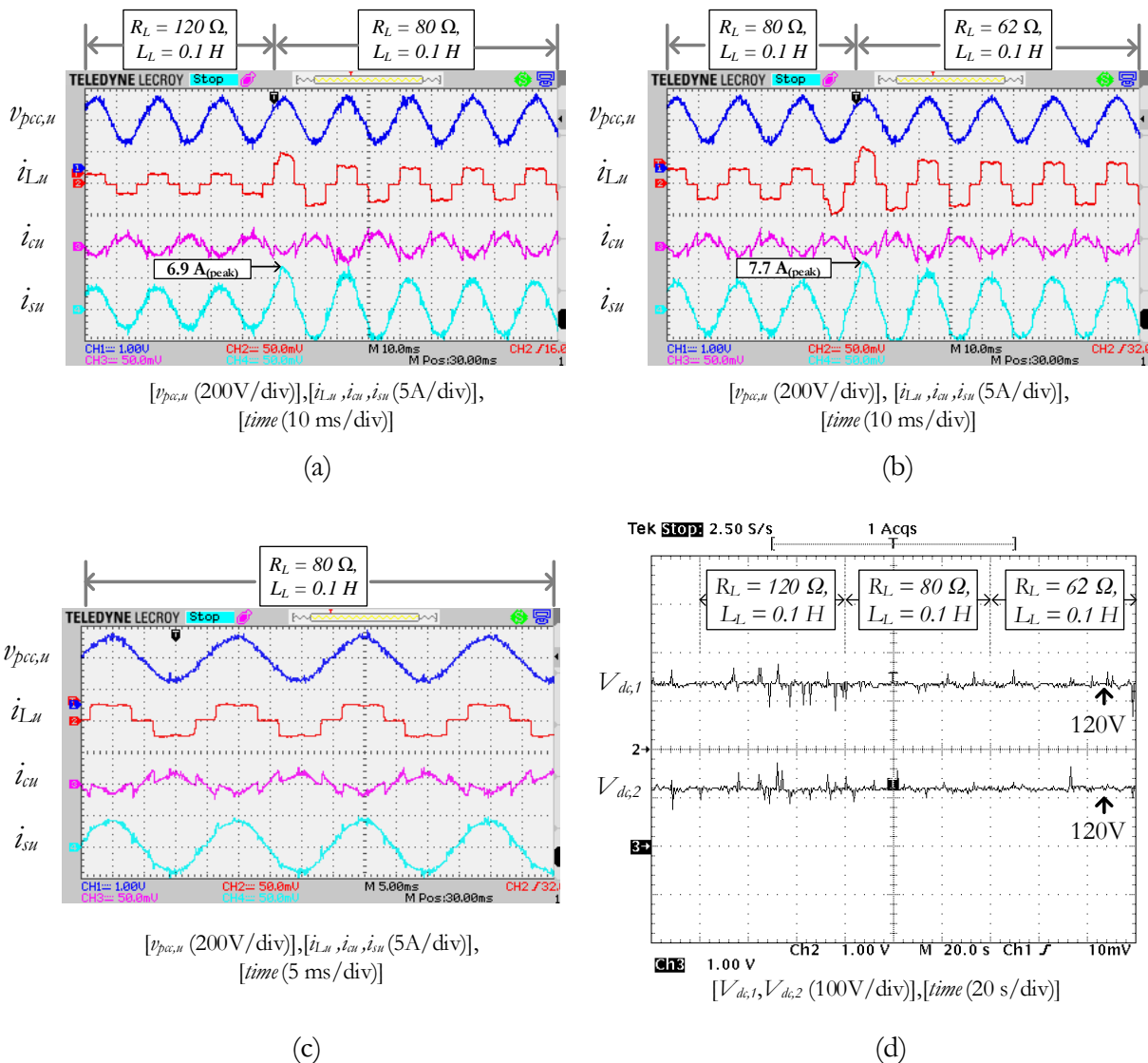


Fig. 12. The testing results of harmonic elimination with P+RES controller. (a) The peak amplitude of load current changing from $2 A_{(peak)}$ to $3 A_{(peak)}$, (b) The peak amplitude of load current changing from $3 A_{(peak)}$ to $4 A_{(peak)}$, (c) The amplitude of load currents at $3 A_{(peak)}$, (d) The performance of the DC bus voltage control.

The results of the harmonic elimination using a P+RES controller are shown in Fig. 12 (a)-(c). From the results in Fig. 12 (a)-(c), this controller provides the good performance for harmonic elimination. The $\%THD_{av}$ after compensation is equal to 9.28 %, as shown in Fig. 13 (c). Therefore, the performance of the harmonic elimination with the P+RES controller is better than that from the PI controller. From the dynamic load testing, fig. 12 (a) and (b) show the waveform of $i_{s(uvw)}$ to a step change of the R_L from 120Ω to 80Ω and 80Ω to 62Ω , respectively. It can be seen that the waveforms of $i_{s(uvw)}$ are oscillating sinusoidal waveform. The peak amplitude of i_{su} is equal to $6.90 A_{(peak)}$ ($4.88 A_{(rms)}$) and $7.70 A_{(peak)}$ ($5.44 A_{(rms)}$), respectively. In the steady state condition, the i_{su} is still constant at $4.20 A_{(peak)}$ ($2.97 A_{(rms)}$) and $4.95 A_{(peak)}$ ($3.5 A_{(rms)}$), respectively. As a result, the transient response of the i_{su} from P+RES controller are nearly the same as the transient response of the i_{su} from PI controller. However, the focus of this paper is to achieve the performance of the harmonic elimination ($\%THD$). From the results in Fig. 12 (d), the $V_{dc,1}$ and $V_{dc,2}$ can be varied following on the command values. In particular, the overall results are proposed in Table 1.

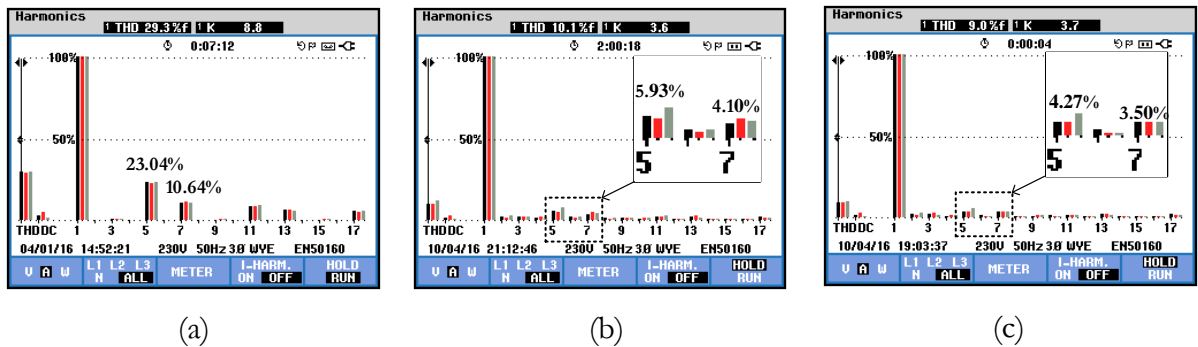


Fig. 13. The spectrum of source currents. (a) Before compensation, (b) After compensation (PI controller), (c) After compensation (P+RES controller).

Table 1. The performance of the source currents before and after compensations.

Performance Index	Phase	The decrease of the amplitude of load currents (2 A _(peak)) (R _L = 120 Ω, L _L = 0.1 H)		The load currents (3 A _(peak)) (R _L = 80 Ω, L _L = 0.1 H)			The increase of the amplitude of load currents (4 A _(peak)) (R _L = 62 Ω, L _L = 0.1 H)		
		Before Comp.	After Comp. PI P+RES	Before Comp.	After Comp. PI P+RES	Before Comp.	After Comp. PI P+RES		
%THD	u	29.5	9.9 8.9	29.3	10.1 9.0	29.2	11.3 10.2		
	v	29.2	10.3 8.2	29.0	10.1 8.9	28.8	11.3 9.4		
	w	29.8	12.9 8.5	29.6	11.7 9.9	29.4	12.5 10.3		
	ave	29.5	11.11 8.53	29.3	10.66 9.28	29.1	11.71 9.97		

In addition, the APF topology as shown in Fig. 1 can compensate the harmonic current in the unbalanced three-phase system. But the testing for the harmonic elimination in this work is only considered in the balanced three-phase system. However, the authors will test the unbalanced three-phase system in the future work.

5. Conclusion

The PI and the proportional plus resonant (P+RES) controllers are designed by discrete design approach. The design of PI and P+RES controllers are fully presented in this paper. The harmonic elimination system with the three-leg split-capacitor APF and the overall control strategy on *dq0*-axis have been implemented. In the paper, the performance comparison of the compensating current control using the PI and the P+RES controllers is tested with dynamic load changing. The experimental results confirm that the proposed control strategy based on digital control is very useful to mitigate the harmonics in the system. The results show that the P+RES controller can provide the good performance of the harmonic elimination compared with the PI controller in term of %THD.

Acknowledgements

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