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Harmonic Reduction in Multilevel Inverter Based on Super Capacitor as a Storage

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Abstract

Cascaded H-Bridge multilevel inverterhas become more attractive to generate high power in an electrical distribution system. This paper discusses the control of five level cascaded H-bridge multilevel inverter with super capacitor as a Dc energy storage. The control of the multilevel inverter using PI and space vector pulse width modulation (SVPWM) controllers based on the modelling and Simulink of cascaded H-bridge can observe the effectiveness of the proposed control to reduce harmonic contents of the multilevel inverter output.High frequency ripple from the inverters can be removed from the system using lowvoltage filter. Total harmonic distortion (THD) for both current and voltage is quite low to meet the IEEE standard. Modelling of the system has been done using MATLAB/Simulink.

Keywords: *super capacitor (SC), total harmonic distortion (THD), space vector pulse width modulation (SVPWM)*

1. Introduction

Multilevel inverter has become more attractive to generate high power and high voltage application. The multilevel inverter requires a number of isolated Dc supplies, each of which feeds a power cell,as has been discussed [1, 2]. The modular structure for multilevel inverter is composed of multiple units of identical H-bridge power cell, which is an effective means for reducing the manufacturing cost. Output voltage inverter waveform is formed by several small voltage levels, and distributed sinusoidal over time, resulting in a low THD and *dv/dt* is described in detail in [3]. Multilevel inverters have three topologies: Cascaded H-bridge (CHB) Diode–Clamped (NPC) Flying Capacitors (FC) Cells with separated DC sources conventional, which are discussed in [4, 5]. The power cells are connected in cascaded H-bridge to withstand high Ac voltage, number of voltage levels in a cascaded H-Bridge inverter, *m,* can be found from *m= (2H+1),* where *H* is the number of H-bridge cells per phase. The power cells in one inverter phase are normally connected in cascaded H-bridge on their Ac output side to achieve high voltage operation and low harmonic distortion, which was discussed [6]. In this proposal, the controller used a systemthat combines the controller PI and SVPWM control. In the PI controller implementation Super capacitor energy storage system (ESS), the controller has been designed using MATLAB/Simulink.Super capacitor has matured significantly over the last decade and has emerged with the potential to facilitate major advances in energy storage, which was developed in [7, 8]. The aim of this paper is to achieve high performance for modelling control (SVPWM) cascaded H-bridge multilevel inverter fivelevel to reduce cost and total harmonic distortion (THD) by using super capacitor storage.Space vector modulation is a more attractive candidate and its advantage is the six sector voltage $(V_1 - V_6)$ that operates starting from each switching vector as a point in complex (α β) space and consists of six sectors, with each having an angle of 60 degree. Each sector consists of $(n-1)^2$ triangle SVPWM diagram of an n-level inverter, which consists of 125 five-level, as proposed in [9]. There are many types of dc storage applied to multilevel inverters such as battery, fly wheel and another related dc source meet of three phases of dc source have their charge and limitation in reducing harmonic distortion in the selected network.Design of a dynamic model multilevel inverter based on Super capacitor, Dc bus and various losses has been discussed in [10]. Five level diode clamped inverter based on

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super capacitor and battery investigation PV energy has been developed in [11]. Three level inverter with Third Harmonic Injection PWM (THIPWM) dynamic performance of super capacitor and batteryto generated DC output voltage or current of the DC side to solve the problem of unbalanced neutral line voltage of three-level inverterwas proposed [12]. The novelty of this paperproposes that harmonic content in a multilevel inverter can be investigated by generating SVPWM signal based on super capacitor (SC) as storage replaced by traditional dc source to generated high harmonic distortion.The circuit structure and switching states of a five-level cascaded H-bridge inverter are introduced. The proposed modulation is a five-level cascaded inverter to solve problem high total harmonic distortion, and the cost consists of four lookup table 24 switching based on super capacitor storage source inverter. It can observed that the voltage and current's THD for the super capacitor is considered low at 5% as specified by IEEE 519 standard on reduce harmonic distortion level. The proposal has been implemented using MATLAB/SIMULINK.It only consists of four switching cell cascaded H-Bridge and four super capacitor energy storages are achieved to five level inverter with R-L load. It provides a measure of the thermal influence of the harmonic, or it is the ratio of the RMS value of the harmonics to the fundamental.

2. Space Vector Algorithm Based on Super Capacitor Storage

The general space vector modulation is applied in the presented three-phase n-level CHB inverter. $h\ (0.866=\sqrt{3}/2)$ [13] is the height of a sector Si, which is an equilateral triangle of unity side as shown in Figure 4. Space vector selection and switching state sequence of the inverter are discussed. The line-to-line voltage, v_R, v_S, v_T can be obtained through the inverter phase voltage:

$$V_R = m\sin(2\pi fs + 90) \tag{1}$$

$$V_S = m\sin(2\pi fs + 90 - \frac{2\pi}{3}) \tag{2}$$

$$V_T = m\sin(2\pi fs + 90 + \frac{2\pi}{3}) \tag{3}$$

According the three-phase to two-phase frame transformation, the output voltage of the three-level N-level cascaded H-bridge inverter can be represented by a space vector in the $\alpha\ \beta$ frame:

$$\begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{3} \\ 0 & \sin\frac{2\pi}{3} & \sin\frac{4\pi}{3} \end{bmatrix}\begin{bmatrix} V_R \\ V_S \\ V_T \end{bmatrix} \tag{4}$$

Where v_α and v_β are the real and imaginary components of the space vector respectively. $/\bar{V}/$ is the magnitude and γ is the phase angle of the space vector. The space vector, reference vector, two-level inverter, on-time calculation within a sector $Si, i = 1, 2, .., 6.$ for a two-level inverter volt-second equation is discussed in [14]: To apply SVPWM technique, first, the angle (γ) and sector (S_i) of $Vref$ need to be determined by using:

$$\gamma = rem\ \left(\frac{\theta}{\pi/3}\right) \tag{5}$$

$$S_i = int\ \left(\frac{\theta}{\pi/3}\right) + 1 \tag{6}$$

In Equation (6) and (7), $0(0^\circ \le 0 \le 360^\circ)$ is the angle of the reference vector with respect to α axis, $\gamma(0^\circ \le \gamma \le 60°)$ is the angle within the sector and $S_i (1 \le S_i \le 6)$ is its sector operation, and *int* and *rem* are standard mathematical functions of integer and reminder, respectively [8]. On-times

$t_a(tA_a), t_b(tA_b),$ and $t_o(tA_o)$ are calculated using Equation (8)-(10), where the required operation is only (8)-(9). Identify triangle in a sector and the on-times are calculated using:

$$T_a = T_S\left[V_X^Z - \left(\frac{V_\beta^Z T_S}{2h}\right)\right] \quad (7)$$

$$T_b = T_S\left[\frac{V_\beta^Z}{h}\right] \quad (8)$$

$$T_o = T_s - T_a + T_b \quad (9)$$

Figure 1 shows the space vector diagram for five-level inverter.The switching instant of a SVPWM pulse waveform is shown in Figure 2.

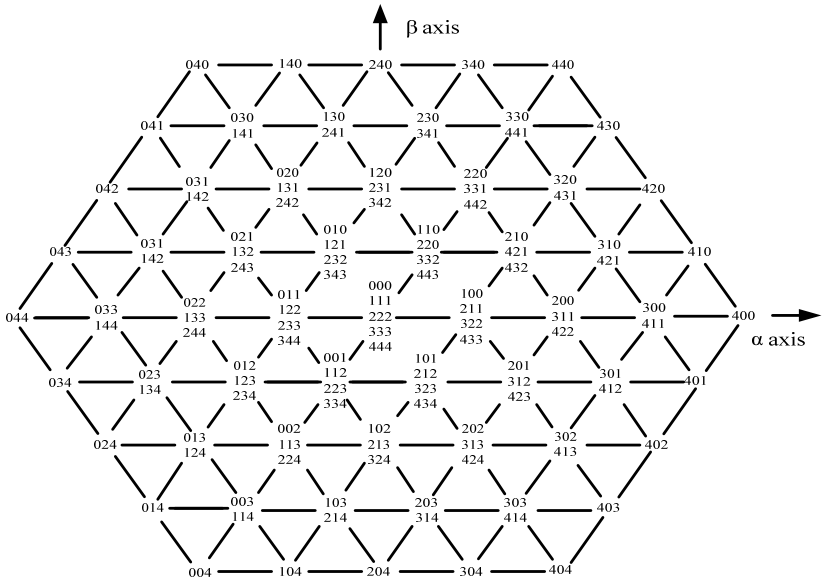


Figure 1. The space vector diagram for five-level inverter [8]

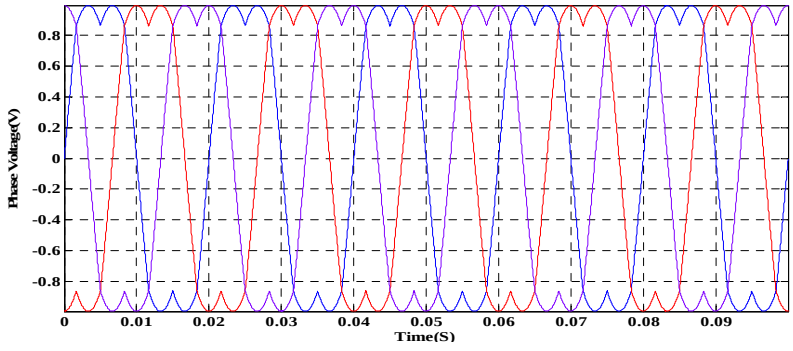


Figure 2. Switching instant of a SVPWM pulse waveform

A super capacitor can be modeled tousecircuit standard components as shown in Figure 3. This design circuit usesa similar circuit as presented in the data sheet for the supercapacitor from EPCOS and the recommendations from the project supervisor in [15].

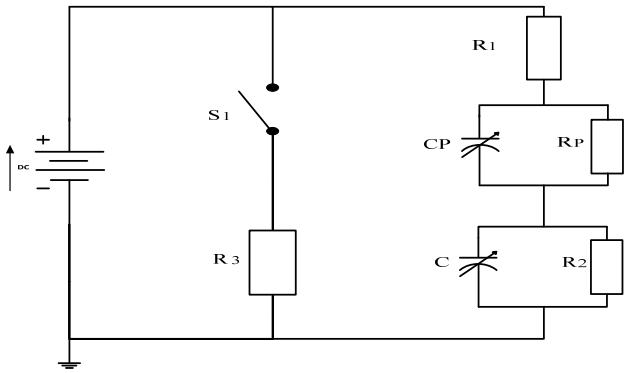


Figure 3. The Basic Circuit Model of the Super Capacitor (EPOCS)

The design uses supercapacitor instead of battery because battery is insufficient to supply real power charge and discharge conditions. Supercapacitor uses circuit RC connected series formed by a capacitor constant and a resistance constant. The capacitance and the serial resistance of the super capacitor are dependent on frequency, temperature and voltage. The simulations have been designed, the time for simulation is short and thus the effect of the temperature and voltage difference can be neglected because they are almost constant. The self-discharge has been neglected due to the same reason. The frequency variations of the supercapacitor current are low enough to assume that the capacitor value is also constant, super capacitors can operate even at low temperature (e.g. -20°C). Super capacitor can be supplied to high voltage charge and discharge is neglected because the frequency, temperature and voltage are constant, high performance SC apply modeling can reduce THD. The capacitance C is responsible for the most important phenomenon in the model. It determines how charge is handled in the circuit. The amount of energy stored and the rate of energy level variations are both determined mainly by the capacitance value. The resistance R2 that is connected in parallel with the capacitor is meant to represent the self-discharge effect. The series resistance R1 represents the losses during charge and discharge. These losses occur because the conducting element in the super capacitor has a resistance, so the connection is not ideal. The over voltage protection provided by R3 and the switch controlling its connection to the circuit is necessary to prevent damage to the capacitor elements by balancing the voltage level. The voltage balancing is needed because otherwise the voltage in one separate cell can increase higher than the others, resulting in gassing or explosion. This voltage difference can occur if one cell has a lower capacitance than the others, since those results in more energy being stored. The resistance Rp and the capacitance Cp are included in the circuit to model some of the fast dynamics in the behavior of the super capacitor.

$$R1 = \frac{\Delta u}{\Delta i} \tag{10}$$

$$R3 = \frac{\Delta t}{-\ln\left(\frac{v_1}{v_\circ}\right)C} \tag{11}$$

$$u(t) = \int \frac{i(t)}{C} dt \tag{12}$$

The creation of a first Simulink model to use the supercapacitor according to the basic circuit is described in Figure 3. A simple circuit initial model testing is done consisting of a capacitance and resistance in parallel with a resistance in series. This base circuit manages to show the basic function of the super capacitor [15]. By adding more components until the circuit described in Figure 3 is achieved, the accuracy of the model is improved. This block diagram that is used considered the basic model of the supercapacitor as shown in Figure 4. The controls block relay the switch that connects the resistance balancing *R3* to the circuit [16]. To calculate *R1, R3*, lookup table to be determined by using:

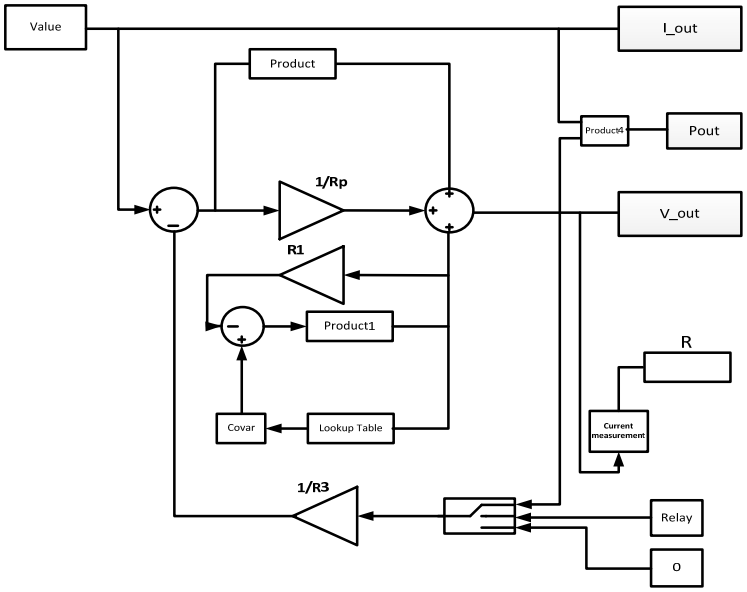


Figure 4. Block Diagram of super capacitor (SC)

When high currents are used, other effects than the capacitance can affect the voltage level. These effects can cause the calculated capacitance value to be incorrect [7].

$$Q = i(t)dt \quad (14)$$

Where; Q = stands for charge,

The charge in a capacitor can be calculated using the integral of the current during one charging cycle [17]. The capacitance value can then be calculated using:

$$C = \frac{\Delta Q}{\Delta u} \quad (15)$$

Where; Q and u = The differences in charge and voltage [17][18].

3. The Proposed Control Method of a Cascaded H-Bridge Multilevel Inverter

The proposal of this model to design three phase cascaded H-Bridge (CHB) five level inverter control space vector pulse width modulation (SVPWM) based on super capacitor as storage (SC) was developed as shown in Figure 5. Space vector modulation (SVM) for five-level inverter consists of 16 triangles, in which triangle one has 13 switching states vectors, triangle two-four have 10 switching states vectors, while triangle three has 11 switching states vectors. Triangle five-seven-nine have 7 switching states vectors, triangle six-eight have 8 switching states vectors, triangle ten-twelve-fourteen- sixteen have 4 switching states vectors and triangle eleven-thirteen-fifteen have 5 switching states vectors [19]. This proposed simulation diagram for five level inverter using algorithm SVPWM technique to generate cascaded H-Bridge inverter consists of 24 switch IGBT and four super capacitor source as shown in Figure 6. Algorithm SVPWM can generate any level to extend three-five level. The harmonic and THD profiles of the output voltage and current of the CHB inverter are investigated. Three phase R-L load contains a balance, in which the values of the resistance R=3.69 and inductive L=2mH. The fundamental frequency *f*is 50Hz and the inverter switching frequency is 3 kHz. Figure 7 presents three phase switching IGBT five level inverter phase A, B and C. The parameters of the multilevel inverters used MATLAB/SIMULINK.

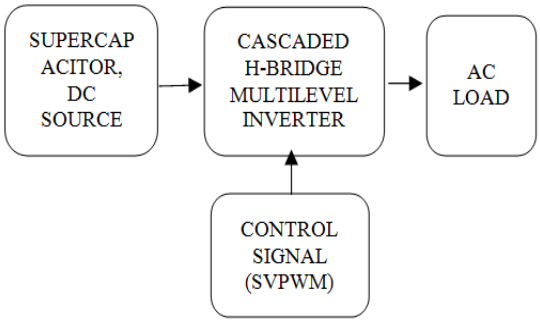


Figure 5. Block diagram of the proposed technique

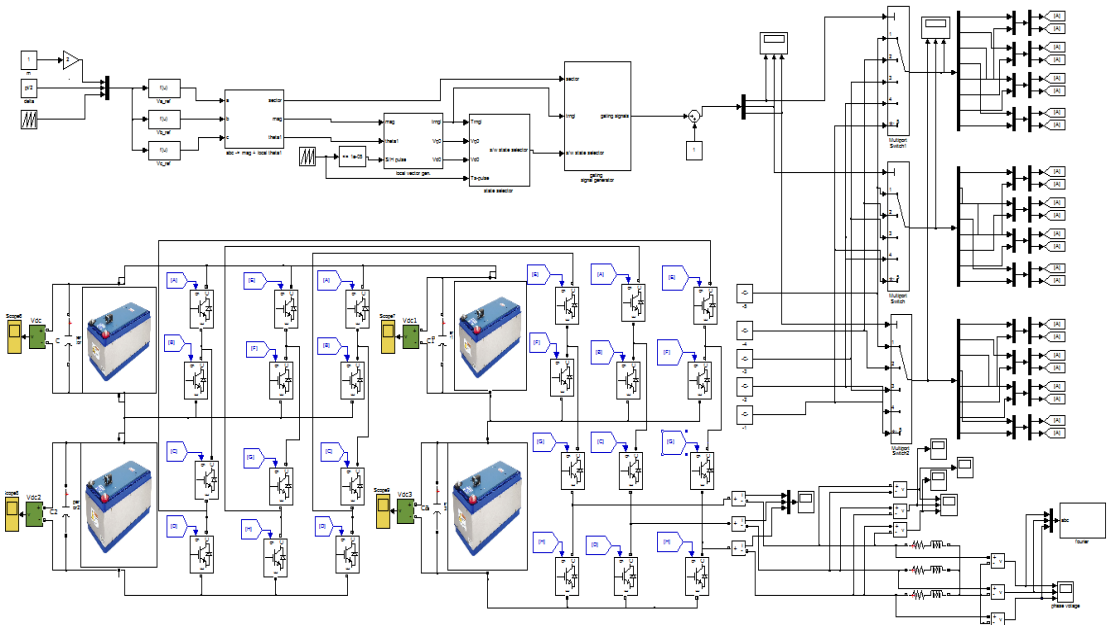
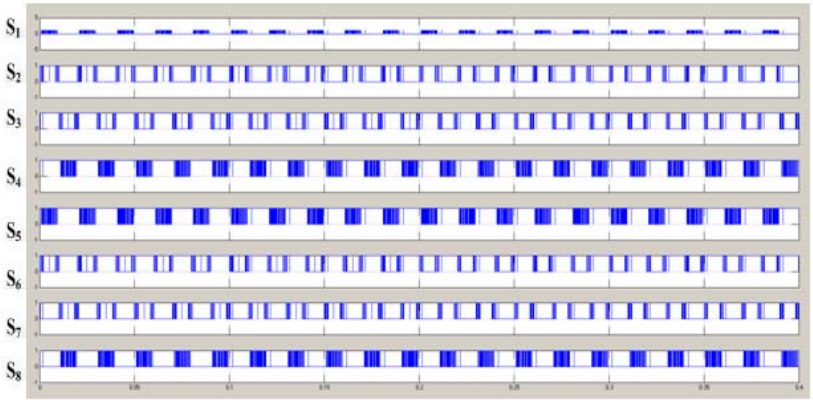
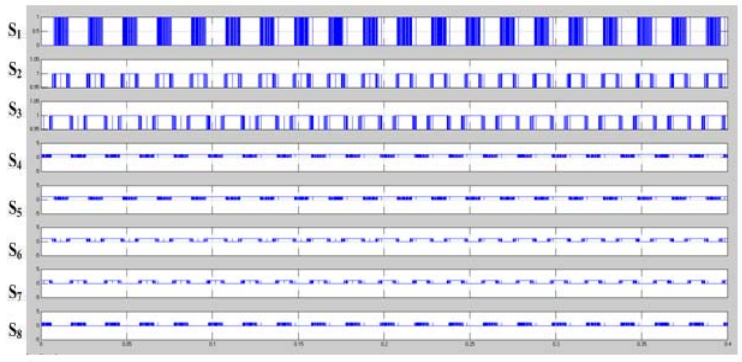


Figure 6. Design SimulinkModel SVPWM five level CHB Inverter with Super capacitor (SC) source

Phase A



Phase B



Phase C

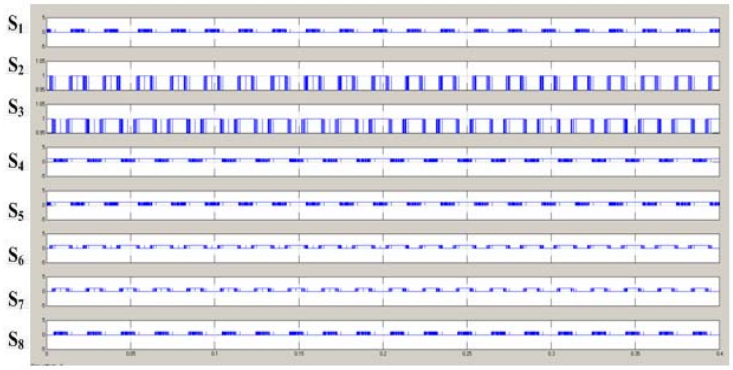


Figure 7. Three phase Switching IGBT Five level (SVPWM) InverterPhase A, B and C

4. Simulation Result

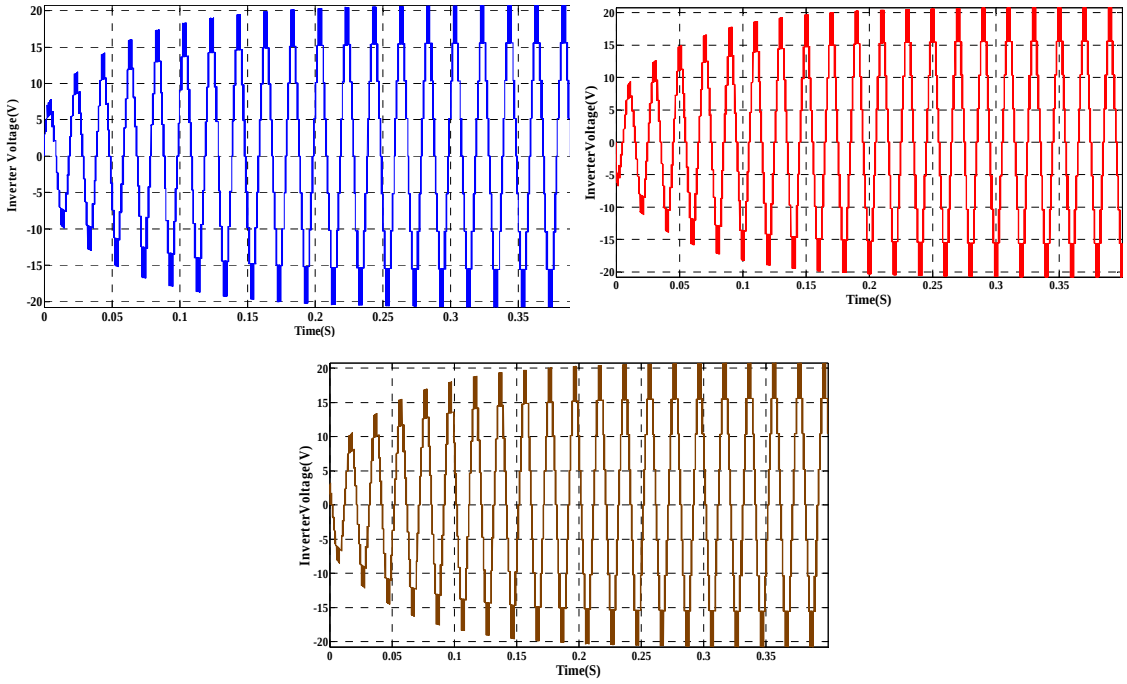


Figure 8. Three phase output voltage Five level SC inverterPhase A, B and C

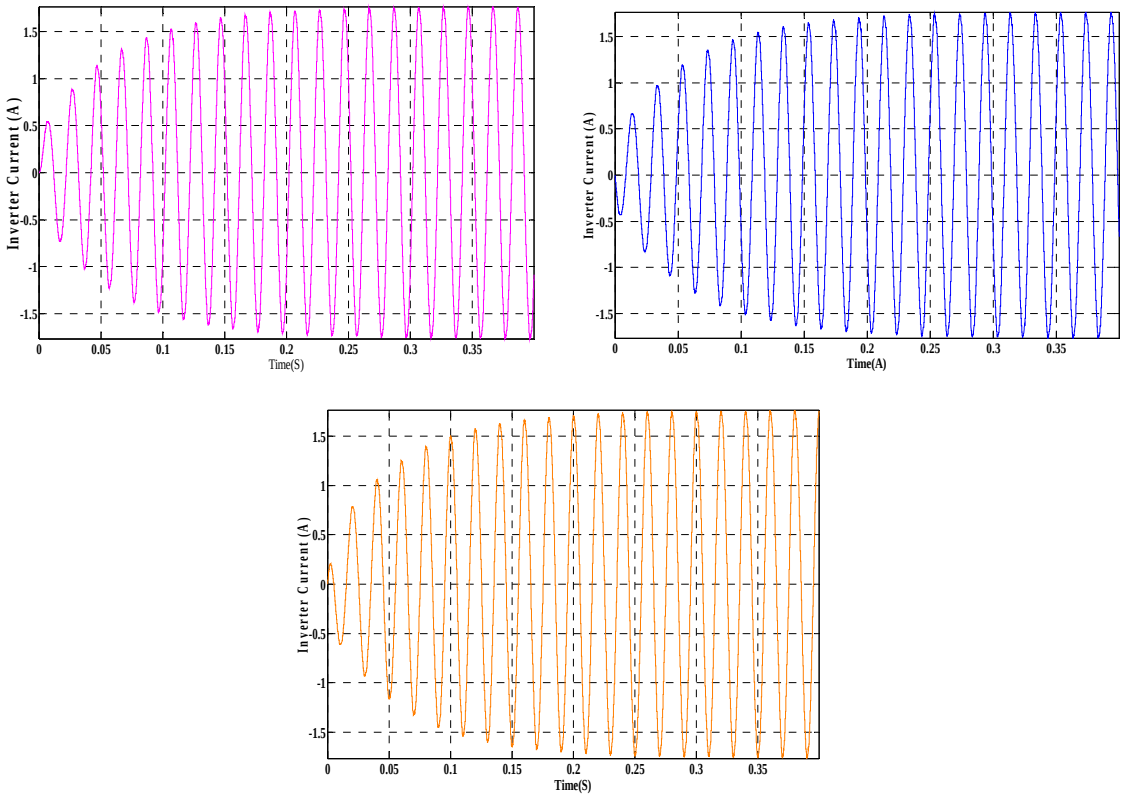


Figure 9. Three phase output Five level SC inverter current Phase A, B and C

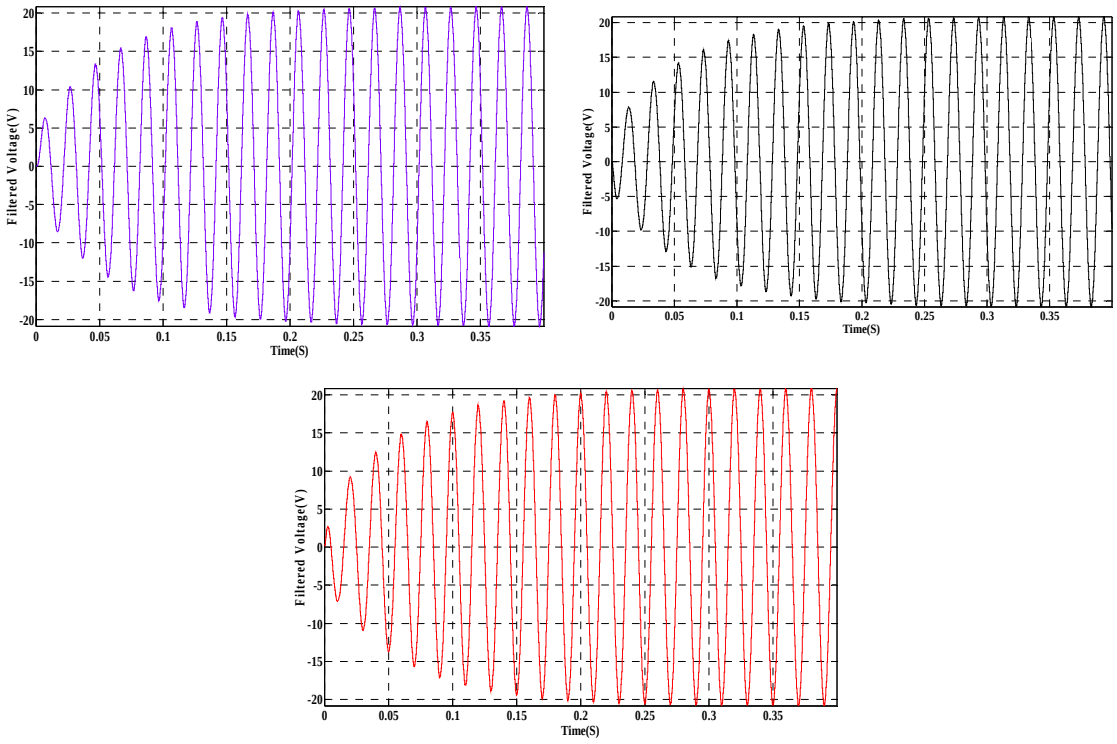


Figure 10. Three phase output Five level SC Filtered voltage inverter Phase A, B and C

It can observed that the total harmonic distortion (THD) of super capacitor voltage and current isconsidered low at 5%, as specified by the IEEE 519 standard on harmonic distortion level as shown in Figure 11. THDv equals to 18.69%, and THD_A equals to 1.14%as shown in Figure 12. Three-phase THD_A load filtered voltage equals to 0.56% as shown in Figure 13. Total harmonic distortion (THD) of super capacitor Dc voltage implementation after the time (Ts) is set from 0.5 to 0.6s equal to 80.41% as shown in Figure 14. Model for super capacitor (SC) produces a fixed value of voltage equals to 5.2 V as shown in Figure 15. Output current equals to 0.89 A as shown in Figure 16.

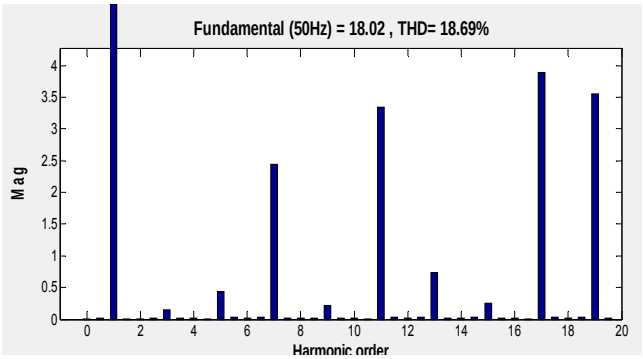


Figure 11. THDv of SC inverter voltage

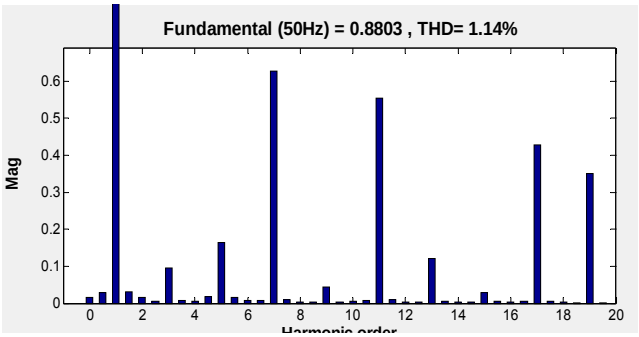


Figure 12. THD_A of SC inverter current

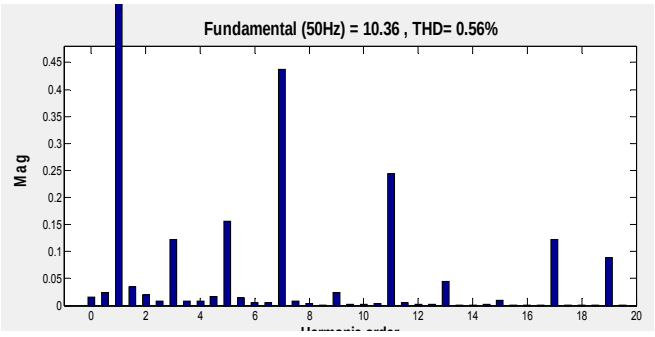


Figure 13. THDv of SC inverter filtered voltage

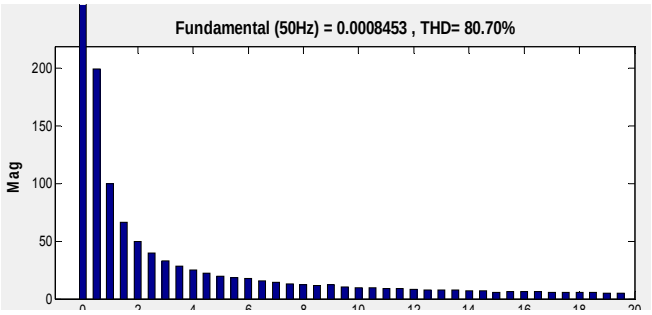


Figure 14. THDv of SC Dc Voltage (Ts= 0.5 to 0.6)

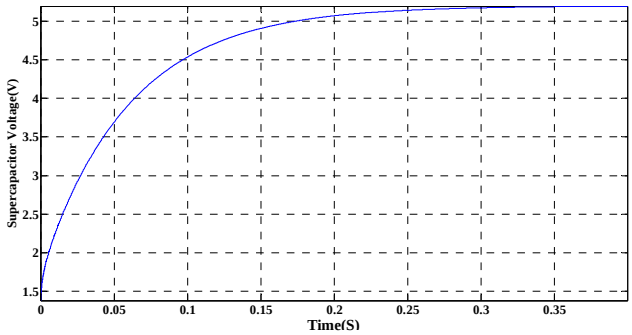


Figure 15. Super Capacitor DC Voltage

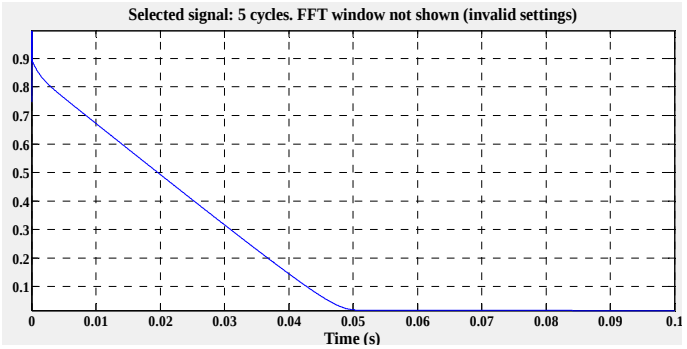


Figure 16. Super Capacitor DC Current

5. Conclusion

In this paper, total harmonic distortion (THD) of three phase space vector pulse width modulation (SVPWM) cascaded H-Bridge five level inverter based on super capacitor (SC)dc source as storage is reduced.It can observed that the Voltage and current THD for the super capacitor is considered low at 5% as specifiedby IEEE 519 standard on harmonic distortion level. The proposedmodel has investigated better harmonic distortion for voltage and current.In the next step, the prototype willbe developed based on the inverter of cascaded H-Bridge with super capacitor. This simulation will be validated through experiments in order to ensure the effectiveness of using Super capacitor as a storage compared to other dc source.

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