Faculty of Manufacturing Engineering

WIP CONTROL AT END OF LINE OF SEMICONDUCTOR INDUSTRY USING CONWIP

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DECLARATION

I declare that this thesis entitled "Wip Control At End Of Line Of Semiconductor Industry Using Conwip" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : .....

Name : LIM KE SIN

Date : 25/9/14

APPROVAL

I hereby declare that I have read this dissertation/report and in my opinion this dissertation/report is sufficient in terms of scope and quality as a partial fulfillment of Master of Manufacturing Engineering (Industrial Engineering).

Signature : .....

Supervisor Name : DR. CHONG KUAN ENG

Date : 25/9/14

DEDICATION

To my beloved family members

ABSTRACT

Advancement of technology and trends in globalization has resulted in higher customer demands and expectations. Manufacturers now offer mass customization to stay competitive. In the semiconductor industry, where product mix and volume are high, production is further complicated by the different process routes and processing times for different product families. Coupled with rapid changeovers of products, it is essential to keep the work in process (WIP) low in order to reduce the inventory level on the shop floor. Constant WIP (CONWIP) is a production control strategy applicable in many manufacturing environment that use cards to control WIP level. This research was conducted in a semiconductor manufacturing company facing difficulty in reducing the variation in WIP on the shopfloor. The objectives of this research are to design and develop simulation models for single loop CONWIP, multi loop CONWIP, hybrid CONWIP, single loop CONWIP and multi loop CONWIP with buffer size optimization based on the environment in the case company. With the developed models, the maximum throughput (TH) and minimum WIP were determined. Discrete event simulation models were developed using the Witness Software for processes at the End of Line (EOL) production in the company. Experiments were conducted using these models to compare the current system with the single loop, multi loop, and hybrid CONWIP control mechanisms. In addition, buffer optimization incorporating single loop and multi loop control were also examined. Performance parameters of TH and WIP level were compared in all experiments. The results show that CONWIP production control is more effective in reducing WIP level compared to the current system. Secondly, the single loop CONWIP showed the least number of cards in the system. However, hybrid CONWIP is more robust and provides a better control mechanism compared to the single and multi loop system. Buffer optimization control can further reduce the number of cards in the single and multi loop control. The developed simulation models are useful to determine the number of cards in the system and buffer size for each process. With these models, the production personnel can monitor and control the WIP dynamically to meet current demands and utilize the shopfloor space for more productive purposes.

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LIST OF ABBREVIATIONS

ACRONYM	DEFINITION
AHP	Analytic hierarchy process
AV	Auto Vision
BAP	Buffer allocation problem
BAV	Buffer Auto Vision
BMould	Buffer Moulding
BPlate	Buffer Plating
BPMC	Buffer Post Mould Curing
BTBC	Buffer Tie Bar Cut
BTNF	Buffer Trim and Form
CAD	Computer Aided Design
CAPP	Computer Aided Process Planning
CONLOAD	Constant Load
CONWIP	Constant WIP
CT	Cycle time
DES	Discrete Event Simulation
EDD	Earliest due date
EOL	End of line
EVA	Economic value added
FCFS	First come first serve
FIFO	First in first out
FOL	Front of line
GA	Genetic Algorithms
JIT	Just in time
MI	Manual Inspection

ACRONYM	DEFINITION
MOLD	Moulding
MSRD	Multiple objective scheduling and real time dispactching
MTO	Make to order
MTS	Make to stock
OBA	Optimal buffer allocation
PLATE	Plating
PMC	Post Mould Curing
POLCA	Paired-cell Overlapping Loops of Cards
QTMU	Queue time maximum un-matches
SA	Simulated Annealing
SC	Supply chain
SME	Small Medium Enterprise
SPC	Statiscal process control
SPT	Short time processing
STC	Statiscal throughput control
TBC	Tie Bar Cut
TH	Throughput
TNF	Trim and Form
TS	Tabu Search
UPH	Unit per hour
VMI	Vendor managed inventory
WIP	Work in process

LIST OF PUBLICATION AND AWARDS

Lim, K.S., 2012. CONWIP Simulation Model for EOL Processes in Semiconductor Industry. Malaysia Melaka Technical Universiti, Melaka, Malaysia, 22 February 2012, Won Silver Medal in UTeMeX 2012.

Chong, K.E and Lim, K.S., 2012. CONWIP Based Control of a Semiconductor End of Line Assembly. Malaysian Technical Universities Conference on Engineering & Technology 2012, Perlis, Malaysia, 20-21 November 2012, MUCET 2012.

Chong, K.E and Lim, K.S., 2013. CONWIP Based Control of a Semiconductor End of Line Assembly. Procedia Engineering, vol.53, pp. 607 - 615.

CHAPTER 1

INTRODUCTION

1.1 Background

In the highly competitive and globalized market, companies strive to ensure high levels of customers' satisfaction. On time delivery, qualities with minimum cost are the performance indicators that most customers emphasize on. At the same time, companies always try to maximize the utilization of the equipment, reduce lead time and unnecessary waste in order to increase the profit margin. In the lean manufacturing approach, inventory is one of the wastes and the most challenging part that exists in most companies.

Semiconductor manufacturing involves complicated processes, routes, and parameters (Miyashita and Gautam, 2010). Work in Process (WIP) is a critical issue for the semiconductor industry. WIP are parts that have been started but are not completed during the processes or sequence or routes within the factory. The accumulations of WIP and control policies are a challenge to the industry as holding or accumulation of WIP incurs cost to the company and often causes long process lead time. Proper WIP control and monitoring policies are critical to ensure that the company remains efficient and competitive.

1.2 Background of the Study

In this research, the study will be conducted in a semiconductor company located at Batu Berendam, Malacca. The case company produces a variety of semiconductor products which include DRAMS, small signal devices, as well as power and logic devices. The

products are mainly supplied to the automotive manufacturers. There are 2 main categories of products namely the small package and the big package. The plant produces and final tests for the products.

1.2.1 Manufacturing Processes in Case Company

The major manufacturing processes in the case company can be categorized into 3 groups which are front-of-line (FOL), end-of-line (EOL), testing and marking (TEST MARK) and, finally, quality check and packing processes as shown in figure 1.1.

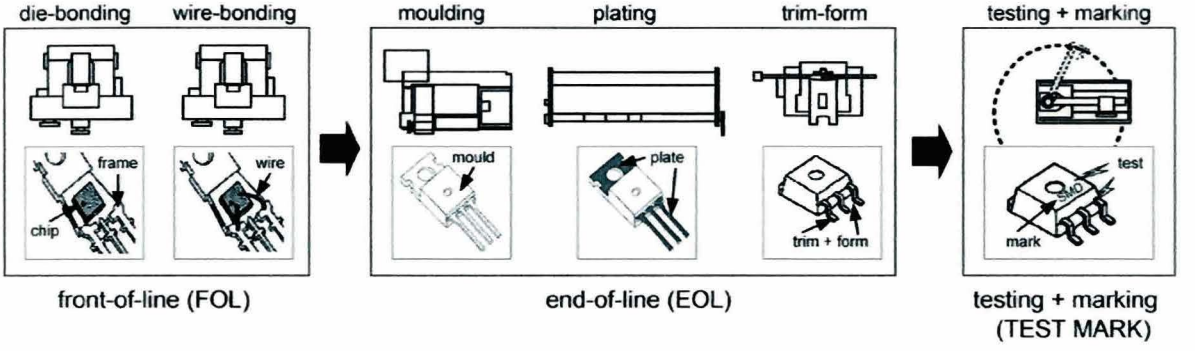

Figure 1.1: Major Processes in the Case Company

FOL major processes which includes are the die bonding and wire bonding are take places in a clean room environment. The operators are enforced to wear full face cover uniform to avoid contamination of particle. In general, die bonding is a process assembly of a die from wafer which has been blade sawed into individual dies and attach to the package or a lead frame. For the wire bonding is a process of making interconnections between a die and package or lead frame of semiconductor devices assembly. The wires are to connect the bonding pad of each device to the lead frame which these wires generally made of gold, aluminium or copper.

EOL processes which also the important part that in this research including the major processes as moulding, electroplating and trim-form. In later part of the chapter, will further expand the process which takes places. These processes are not conducted in a clean-room environment like FOL and involves with heavy machinery in the EOL module, as injection moulding machines, cutting and forming tools and electroplating machines. The moulding is the process of sealing a microchip die with a ceramic or plastic enclosure to prevent physical damage or corrosion. This is process take places after the wire-bonding has been completed at the FOL. Operators load and unload magazines which is a metal boxes that containing up to 40 lead frames to the moulding machine.

Plating is the process for a surface-covering in the semiconductor industry. It is a method whereby the metals in ionic form are supplied with electrons to form a non-ionic coating (plate) on a desired substrate. For trim-form process consists in a moulded strip of components being loaded into a machine that cuts it into individual units called integrated chips (IC). After trimmed, the same machine will perform "leg forming" where IC legs are bent, cut and formed into a desired shape.

The third major processes of testing and marking processes, all the ICs are tested 100%with a machine. The test includes placing the IC in cold or hot temperature, and inducing electrical stress to test IC robustness and its functions. The marking process is incorporated in a testing machine where good ICs will be marked with product information (product codes, date, logo, etc.) immediately after testing.

1.2.2 EOL manufacturing processes

This study is conducted on the End of Line (EOL) manufacturing processes. As shown in Figure 1.2 the end of line actually involves 7 processes which include moulding

(MOULD), post mould curing (PMC), plating (Plate), manual inspection (MI), tie bar cut (TBC), trim and form (TNF) as well as auto vision (AV). The moulding process is to encapsulate the frame into the plastic form. The process of plating is completed by a sub-contractor which outside the plant. On completion of the plating process, the lot will be sent back to the factory for manual inspection by an operator. Next, the lot will be sent for the tie bar cutting process and then the trim and form where all the units on the frame will be trimmed into pieces. Before the lots are sent for final testing, the lots will undergo the auto vision process which is an automated inspection process.

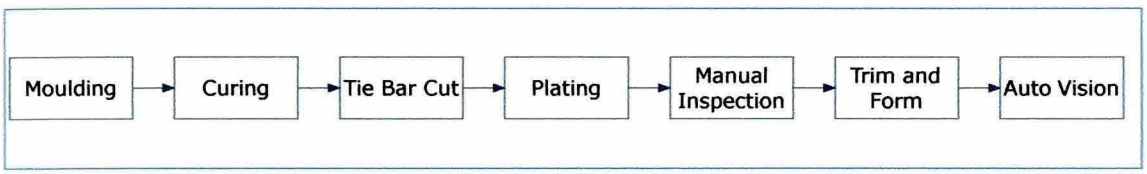

Figure 1.2: EOL Process Flow in the Case Company.

1.3 Problem Statement

The case company is a semiconductor manufacturer of high mix and high volume products. In one quarter of the production period, case company had produed 17788 lots with only one product family. This one product family carried 85 diferrent of products type which have different product routes and parameter. The processes are complex and the routes are different for each product which depends on the requirements or demands of the customers.

With average TH per day around 193 lots, the WIP in the system lies at around 550 – 650 lots everyday. As the volumes are high, the production department monitors the work stream to ensure that the WIP levels are within control. However, it is difficult to closely monitor the WIP level as the work streams are only updated at the end of every shift. Production engineer want to reduce the variation of WIP that float in the system so that the

WIP can be controlled at the satisfactory level. With lesser variation from the production floor, engineer can be response quickly when any problems occurs.

Therefore, the company would like to determine a suitable way to control the WIP in the production lines. In addition, the company wants to identify the opportunities to reduce the cycle time and the waiting time of the lots inside the production.

1.4 Research Objectives

In this research, the main aim is to investigate the WIP level using the CONWIP control mechanism based on the performance measures of maximum throughput (TH) and lowest WIP. The research objectives are:

1. to design and develop simulation models for single loop CONWIP, multi loop CONWIP, hybrid CONWIP, single loop CONWIP and multi loop CONWIP with buffer size optimization based on the environment in the case company.

2. to determine the maximum TH and minimum WIP from each of the developed models.

1.5 Research Scope

The scope of this research is limited to the EOL of the case company. One of the most frequent product family which consist 85 products will be taken into account to ensure that the simulation model represents the real environment. The key performance indicators for the research are WIP and throughput.

The operational models for the proposed scenarios for different CONWIP control mechanisms are evaluated using the WITNESS simulation software with optimizer, while statistical analysis will be conducted with the Minitab Statistical Software.