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Efficient ultra-high-voltage controller-based complementary-metal-oxide-semiconductor switched-capacitor DC–DC converter for radio-frequency micro-electro-mechanical systems switch actuation

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Abstract: Achieving wireless connectivity in ever smaller, lower power portable devices with increasing number of features and better radio-frequency (RF) performance is becoming difficult to fulfill through existing RF front-end technology. RF micro-electro-mechanical systems (MEMS) switch technology, which has significantly better RF characteristics than conventional technology and has near-zero power consumption, is one of the emerging solutions for next generation RF front-ends. However, to achieve satisfactory RF MEMS device performance, it is often necessary to have an actuating circuitry to generate high direct current (DC) voltages for device actuation with low power consumption. In this study, the authors present an RF MEMS switch controller based on a switched-capacitor (SC) DC–DC converter in a 0.35 μm CMOS technology. In this design, novel design techniques for a higher output voltage and lower power consumption in a smaller die area are proposed. The authors demonstrate the design of the high-voltage (HV) SC DC–DC converter by using low-voltage transistors and address reliability issues in the design. Through the proposed design techniques, the SC DC–DC converter achieves more than 25% higher boosted voltage compared to converters that use HV transistors. The proposed design provides 40% power reduction through the charge recycling circuit. Moreover, the SC DC–DC converter achieves 45% smaller than the area of the conventional converter.

1 Introduction

Radio-frequency (RF) micro-electro-mechanical systems (MEMS) are an emerging technology that has shown significant promise in providing robust, higher power handling and low-cost transduction capabilities. More important, RF MEMS switches exhibit near-zero power consumption. With these advantages, RF MEMS switches have an extremely broad range of applications in aerospace and defence. Recently, RF MEMS switches have also begun to be considered for integration into the strong growth of global portable smart devices with their significantly better RF characteristics than conventional P–I–N diodes or field effect transistor (FET) switches [1]. However, the operation of RF MEMS requires a switch controller which can provide high direct current (DC) actuation voltages ranging from 20 to 100 V. Furthermore, the switch controller for RF MEMS is required to meet several other specifications such as small size, low power consumption and linearity. The small feature size can be solved by the continuous shrinkage available in current silicon-based complementary-metal-oxide-semiconductor (CMOS) technologies. However, it may be more challenging to deal with the requirement of high DC voltage, which is much higher than the supply voltage of CMOS technology and low power consumption. In addition, the whole design should fit in a small die area to reduce the overall cost. In this paper, these challenges will be addressed and solutions will be proposed. By accommodating the requirements of RF MEMS switches, it is possible to integrate RF MEMS devices with core signal processing circuitry leading to the implementation of compact high-performance RF front-ends.

The switch controller will be based on a switched-capacitor (SC) DC–DC converter. An SC DC–DC converter is an inductorless converter that uses only switches and capacitors without involving amplifiers or transformers to step up or step down the voltage. This approach has the advantages of light weight, small size and high-power density. Among various phases of SC converters, 2-phase SC converter appears as one of the most promising topologies because of its simpler switching circuitry when

integrated with RF MEMS switches in portable devices. There are several types of topologies for SC converters such as linear voltage gain [2, 3], doubler voltage gain [4–6], and Fibonacci voltage gain [7, 8]. When implemented in CMOS technology, the linear voltage gain shows the best performance among these topologies [9]. Previous research in linear voltage gain SC converters is targeted at non-volatile memory where the focus of the research is on low voltage (LV) operation and high-output currents [3, 5, 10–12]. However, these design merits are not suitable for a high-voltage (HV) SC converter targeted at RF MEMS applications. Most commercially available SC converters are limited to maximum output voltages between 12 and 15 V. To achieve higher output voltages, bulky and costly solutions based on external discrete components tend to be used. This paper presents a complete design, analysis and synthesis of an HV SC converter for low power consumption and small die area in CMOS technology.

In Section 2, an overview of the operation of RF MEMS switches using high actuation voltage is presented. The operation of the SC DC–DC converter that generates the required high actuation voltage is presented in Section 3. Two adaptive biasing circuits are proposed for the implementation of the SC DC–DC converter using LV transistors in HV CMOS technology as presented in Section 4. In Section 5, we identify the figures of merit for high-output voltage and low power consumption through analysis and synthesis. The performance of the SC DC–DC converter has been improved based on the techniques of using low threshold voltage (V_{TH}) switches and a charge recycling circuit as demonstrated in Section 6. The proposed design strategies are verified with the fabrication ready post-layout simulation in Cadence environment using the 0.35 µm Austriamicrosystems (AMS) technology as presented in Section 7. Section 8 benchmarks the presented work against previous research works. Finally, the integration of the RF MEMS switch with the HV SC DC–DC converter in a package, as subjected to future work, is illustrated in Section 9.

2 RF MEMS switch

RF MEMS switches are surface-micromachined devices which use a mechanical movement to achieve an electrical change in the RF transmission-line. They are designed to operate at RF to mm-wave frequencies (0.1–100 GHz). They are composed of a thin metal membrane which can be electrostatically actuated to the RF line using a high DC voltage. The basic operation of the RF MEMS switch discussed here is a shunt capacitive switch [13]. When the membrane is in the up position, the signal line observes a small value of capacitance; when the membrane is pulled down by actuated voltage, the signal line observes a high-value capacitance. The equivalent electrical circuit of RF MEMS is shown in Fig. 1. The capacitance of the RF MEMS (CMEMS) can be switched from 2 to 9 pF using 0 and 30 V, respectively. This range of capacitances has great RF applications such as antenna mismatch tuner [14], oscillator and filter.

3 Operation of HV SC DC–DC converter

RF MEMS switches require an actuation voltage in the range of 0–30 V, which is controlled by a customised SC DC–DC converter. The area of the SC converter has to be small for the integration with the RF MEMS in a single package. To reduce the output ripple and gate oxide stress, we apply an interleave structure linear voltage gain SC converter topology [10, 11], as shown in Fig. 2. The initial design of this converter is for an LV converter application [10, 11]. In this paper, we design an HV SC converter based on the enhanced LV interleave topology. Each stage of the SC converter is composed of an nMOS transistor (NM), a pMOS transistor (PM), and a charging capacitor (C). The second row has the same topology as the first row. Clock 1 (CLK1) and clock 2 (CLK2) are non-overlapped clocks. When CLK1 is HIGH, a boosted signal ($P1$) is obtained at the source terminal (S) of the transistors, as shown in Fig. 2. The waveform of $P1$ follows CLK1, whereas $P2$ follows CLK2. These boosted signals ($P1$ and $P2$) are used to trigger the MOS transistors to switch on or off, to form the alternating charge flow across the capacitors for phases 1 and 2. For instance, $P1$ is HIGH when CLK1 in the 1st stage of the SC converter is HIGH. HIGH $P1$ will switch on NM_{21} and switch off PM_{21} in the 2nd row of the SC converter. Similarly, when CLK2 in the second row is LOW, it will switch off NM_{11} and switch on PM_{11}. The off state of PM_{21} and NM_{11} will block the charge from going back to the previous stage, whereas the on state of PM_{11} and NM_{21} will pass the charge to the next stage. $P1$ and $P2$ in this interleave structure provide effective gate switching potentials for boosting up the charge. Different biasing techniques to control the n-type potential (V_{B_N}) and the p-type potential (V_{B_P}), and the bulk-substrate potential (V_{B_S}) of the transistors in inter and final stages are discussed in the next section.

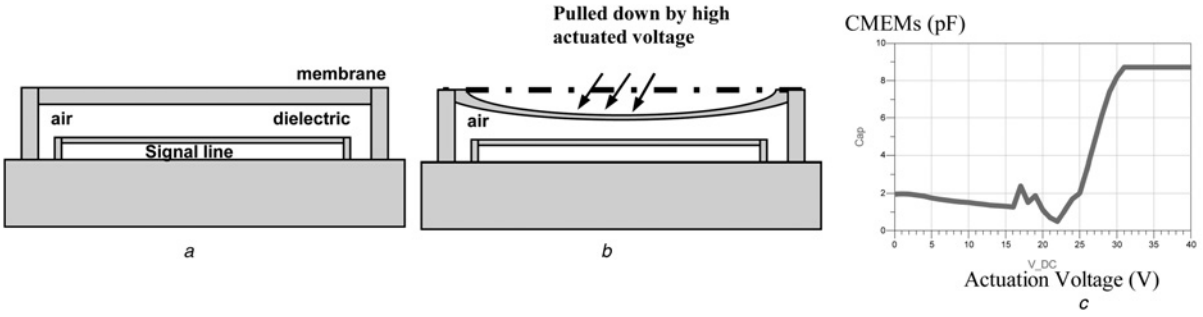

Fig. 1 *Operation of RF MEMS*

a With the membrane in the up position
b With the membrane in the down position
c The equivalent capacitance–voltage graph

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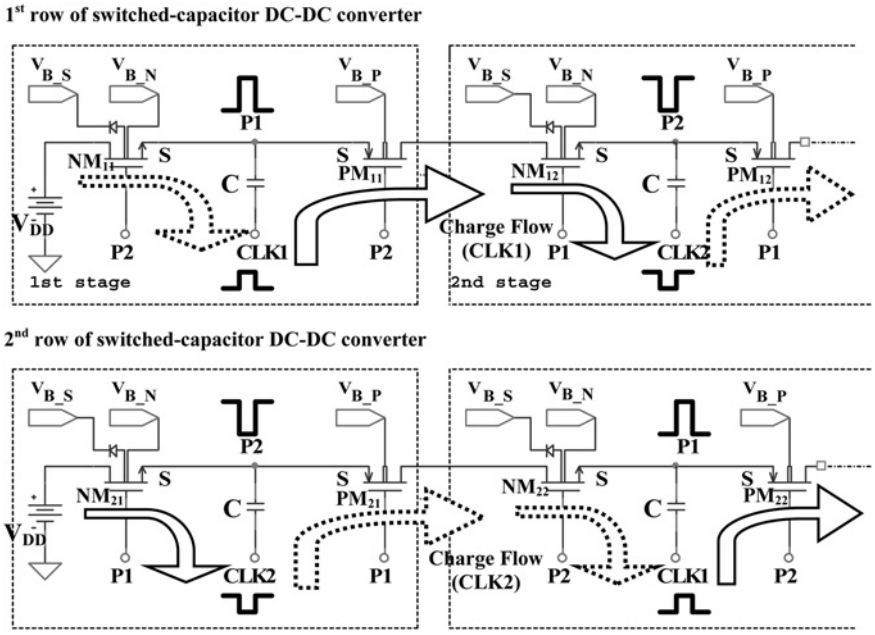

Fig. 2 *Circuit diagram of an interleave structure linear voltage gain SC DC–DC Converter*

4 Design of HV SC DC–DC converter

The bulk potential of the transistors needs to be properly biased when LV transistors are employed in an HV design in order to avoid circuit latch-up and break-down. In [10], the bulk of NMs, and PMs are recommended to be connected to their source. Improvements in operating PMs are recommended in [11], but the designs are still limited to LV applications only. In this paper, we propose two adaptive bulk-biasing circuits for inter and final stages of the SC DC–DC converter. Through the proposed adaptive bulk-biasing techniques, we eliminate the leakage current and maintain a LV drop across the transistors in a large number of stages of the SC converter.

4.1 Adaptive bulk-biasing circuit

The proposed inter stage adaptive bulk-biasing circuits for LV PM and NM are shown in Fig. 3*a*. In the case of a small

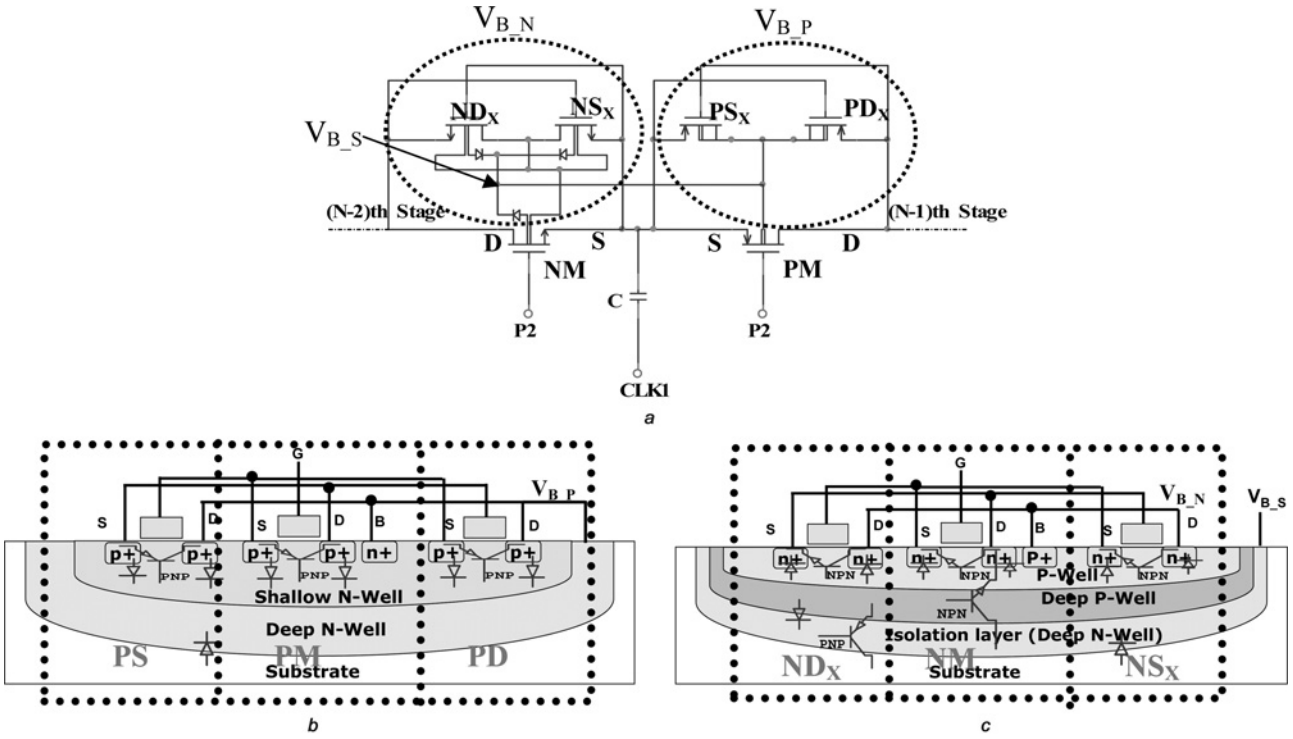

Fig. 3 *Single stage of SC DC–DC converter with the adaptive bulk-biasing circuit*

a Schematic
b Equivalent cross-section in floating LV pMOS transistors
c Equivalent cross-section in floating LV nMOS transistors with parasitic elements

conversion ratio SC converter, the bulk of the NMs (V_{B_N}) was grounded. However, for a larger conversion ratio SC converter, if V_{B_N} is still at zero potential, not only it will increase its bulk effect significantly but also may cause the transistor to break down when the potentials between the drain-bulk, source-bulk and gate-bulk are greater than the technology specific voltage limits. Thus, two auxiliary NMs (ND_X and NS_X) are used to adaptively set the V_{B_N} to the lowest potential between its drain (D) and source (S) in every stage, as shown in Fig. 3*a*. For instance, when the potential of the drain of NM is higher than its source, NS_X becomes forward-biased, and sets the V_{B_N} approximately to NM's source potential. On the other hand, when the potential of the drain of NM is lower than its source, ND_X sets the V_{B_N} to NM's drain potential. By having this adaptive bulk-biasing circuit, the V_{B_N} will always be at the lowest potential and within the technology limit. Similarly but in an opposite way, two auxiliary transistors (PS_X and PD_X) are used to set the bulk voltage of PM (V_{B_P}) to the highest between its drain and source, as shown in Fig. 3*a*. Through the proposed biasing circuit, the source-bulk voltage in each stage of the SC converter no longer increases. Thus, the threshold voltage (V_{TH}) remains almost constant even with a large number of stages.

The cross-section views of two types of transistors (PM and NM) in a single stage SC DC–DC converter are illustrated in Figs. 3*b* and *c*. In this design, the conventional substrate-based (standard) LV transistor is replaced by a floating LV transistor. The substrate-based LV transistor generates substrate noise and collects substrate current [15]. The floating LV transistor has an additional isolation layer, which is not found in standard transistors, is to cater for the technology allowable limit between bulk-substrate from 7 to 50 V. In addition, the floating LV transistor is more robust against substrate noise. The floating LV transistor is available for all HV process options. The process option used in this design is the 0.35 µm 50 V CMOS design kit. The area penalty for the floating LV transistor is negligible.

The PM is a floating LV pMOS transistor with deep and shallow N-wells on p-type substrate as shown in Fig. 3*b*. The deep N-well is the isolation layer. The shallow N-well is the bulk of the PM. Both N-wells have to be biased with the highest potential (V_{B_P}) to avoid switching on the junction diode and further triggering the parasitic PNP bipolar transistor as shown in Fig. 3*b*. Thus, this illustrates the importance of two auxiliary transistors (PD and PS) laid on both sides to bias the bulk and substrate of PM to the highest potential to ensure that no leakage current is drawn to the substrate.

Fig. 3*c* shows the cross-section view of a single floating LV nMOS transistor biased by two auxiliary transistors (ND_X and NS_X). This additional isolation layer will be biased by the substrate potential (V_{B_S}) which is obtained from the V_{B_P} as shown in Fig. 3*a*. For the bulk biasing in the NM, it is similar to the PM but in an opposite way. The bulk of the NM has to be biased to the relatively lowest potential through ND_X and NS_X to avoid switching on the parasitic NPN transistor.

Through this adaptive biasing technique, the HV SC converter can be prevented from latch-up, which guarantees the reliability of the HV SC converter design using LV transistors. The work presented here is not limited to floating LV transistors and can be extended to other standard/substrate-based LV transistors by ensuring the targeted output voltage of the design is within the technology allowable limits of the transistor models.

4.2 Output stage of the SC DC–DC converter

The proposed adaptive biasing circuit for the output stage of the converter has been carefully designed to accommodate the voltage ripples when driving the variable capacitive MEMS load, as shown in Fig. 4. The bulk of the PM at the final stage of the converter is biased by the voltage that is slightly higher than the V_{out} (V_{B_F}), as shown in Fig. 4*a*. The V_{B_F} can be obtained by complementing the two boosted voltages (V_{XC1} and V_{XC2}). These boosted voltages are obtained from V_{X1} and V_{X2} that are connected to the output node (V_{out}) through two small auxiliary transistors (M_{AUX}) and capacitors (C_{AUX}), as shown in Fig. 4*b*. The magnitudes of V_{XC1} and V_{XC2} are slightly higher than V_{out} and $P1$ or $P2$, but within technology allowable limit of the transistors through the transistor (M_{CX}) and a serial large resistor (R_X). By complementing the V_{XC1} and V_{XC2} through the adaptive output reference, a rather linear V_{B_F} can be obtained. By using this output stage biasing circuit, the SC converter can directly be connected to RF MEMS switches without adding a large output capacitance to compensate the ripple because of the variable capacitive load. By avoiding the large output capacitance, our design demonstrates a smaller die area and a faster rise time.

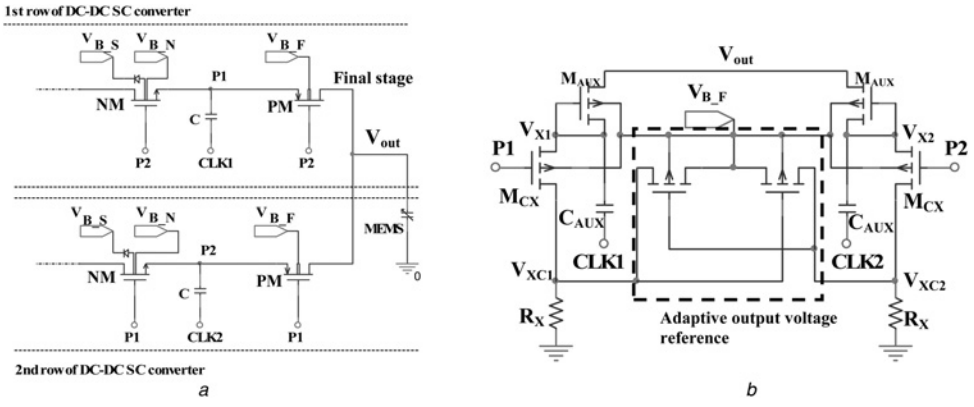

Fig. 4 *Output stage of the SC DC–DC converter with*

a Variable capacitive MEMS load

b Adaptive output stage-biasing circuit

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5 Analysis of the design parameters of HV SC DC–DC converter

5.1 Voltage gain efficiency

The main components of an SC DC–DC converter are the transistors and the capacitors. The first integrated SC DC–DC converter was introduced in [2]. For an ideal N stage SC DC–DC converter with ideal transistors and capacitors driven by a clock frequency f, the output voltage ($V_{\text{out\_IDEAL}}$) can be expressed as in the following equation

$$V_{\text{out\_IDEAL}} = (N+1)V_{DD} - \frac{NI_L}{fC} \tag{1}$$

where N is the number of stages, V_{DD} is the supply voltage, I_L is the output current, C is the charging capacitance per stage, and f is the switching frequency of the SC DC–DC converter.

The output voltage of an ideal SC DC–DC converter operating at 25 MHz with supply voltage of 3.3 V is illustrated in Fig. 5. The output voltage (V_{out}) increases with the number of stages (N) but decreases with the current (I_L) drawn from the converter. The bigger size of the charging capacitor (C) exhibits a higher load driving capability which is able to draw more current without significantly degrading the output voltage of the converter. Capacitors are the components which consume the most design area in CMOS technology. For the 0.35 µm AMS technology, the density of the capacitance in an HV environment is at least three times less than the capacitance in an LV environment. In other words, the area of the converter for an HV is significantly larger than an LV design. Since the SC converter requires a very low output current in actuating RF MEMS, small charging capacitors are used, resulting in significantly reduce die area.

For the SC converter with a linear conversion ratio, which exhibits a similar charge multiplier coefficient at each stage, equal size of charging capacitors are used in every stage. Capacitance optimisation, as in previous research work [8, 16, 17], is not suitable for this linear conversion ratio SC converter. By having an equal charging capacitor in every stage, the driving capability for a defined amount of capacitance is made optimum [18].

5.2 Power consumption

Power consumption is critical in portable devices. Thus, it is highly desirable to reduce the power consumption in the SC DC–DC converter. The power consumption of the converter can be determined by (2). Since V_{DD} is fixed, the input current, I_{power}, is the parameter to be minimised

$$P_{\text{power}} = I_{\text{power}} V_{DD} \tag{2}$$

where I_{power} is the average input current and V_{DD} is the voltage supply.

In a steady-state, the SC converter has a current consumption ($\Delta I_{\text{steady\_state}}$) which depends on the amount of the output current (I_L) and number of stages (N) as shown by the first term in (3) [18]. In a dynamic state, the current consumption ($\Delta I_{\text{Dynamic\_state}}$) depends on frequency, N and parasitic capacitance (C_{P}), as shown by the second term in (3). More analysis of C_{P} will be presented in the next subsection

$$\begin{aligned} I_{\text{power}} &= \Delta I_{\text{steady\_state}} + \Delta I_{\text{Dynamic\_state}} \\ I_{\text{power}} &= (N+1)I_L + NC_{\text{P}} f V_{DD} \end{aligned} \tag{3}$$

where I_{power} is the average input current, $\Delta I_{\text{steady\_state}}$ is the steady-state current consumption, and $\Delta I_{\text{Dynamic\_state}}$ is the dynamic current consumption.

5.3 SC DC–DC converter with losses

The performance of the SC DC–DC converter is degraded by the parasitic effects of the transistors and the charging capacitors. The parasitic effects include the non-ideality in the charging capacitors (C_{P}) and the threshold voltage (V_{TH}) in MOS transistors as given by (4) [2]. The losses because of C_{P} result by a factor of α from its bottom plate, and β from its top plate of charging capacitors [18]. The factor α is generally more than one order of magnitude higher than that of the factor β, so we will focus on α. In [2], α was obtained by measuring the ratio of the parasitic capacitance of the bottom plate of the charging capacitor and the charging capacitor itself, as described by (5); In [18], α was derived through measurements of the input and output current. More generally, α represents a term which links the loss to the total capacitance of the SC converter that appeared in real converter after realisation. The parameter α is technology dependent and varies between 0.1 in capacitors for LV applications and 0.4 for HV applications [19]. Techniques to minimise the effects of these parasitic losses will be presented in Section 6

$$\begin{aligned} V_{\text{out}} = &\left[\left(\frac{NC}{C+C_{\text{P}}}\right)+1\right]V_{DD} - (N+1)V_{\text{TH}} \\ &- \frac{NI_L}{(C+C_{\text{P}})f} \end{aligned} \tag{4}$$

$$\alpha = C_{\text{P}}/C \tag{5}$$

where N is the number of stages, V_{DD} is the power supply, I_L is the output current, C and C_{P} are the charging and parasitic capacitance per stage, V_{TH} is the threshold voltage of the switches, and f is the switching frequency of the SC DC–DC converter.

5.4 Optimisation of the design parameters

As shown by (3), the parameter N plays a significant role in optimising the power consumption. The power consumption can be reduced by optimising the number of stages based on derivation from output current (I_L). By minimising I_L, the

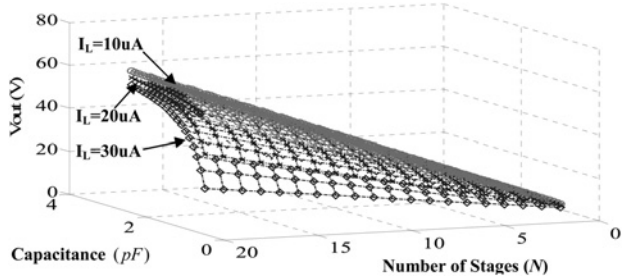

Fig. 5 *Output voltage of an ideal SC converter (without loss) operating at 25 MHz for up to 20 number of stages (N), and three different output currents (I_L)*

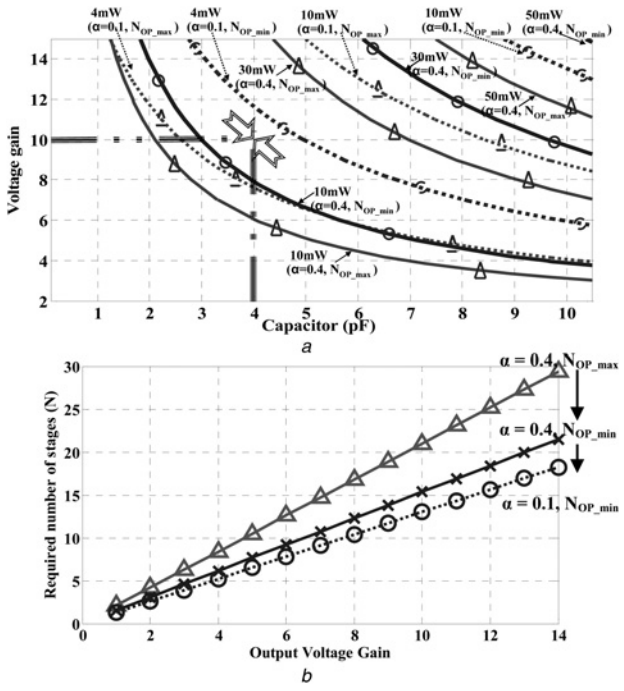

Fig. 6 *Comparison of power consumption and voltage gain by minimising $I_L(O)$ and maximising $I_L(\Delta)$ design*

a Power consumption of an SC converter with parasitic capacitance losses of $\alpha = 0.1$ (dotted line) and $\alpha = 0.4$ (solid line) and $\beta = 0.05$, threshold voltage $V_{TH} = 0.7$

b Required number of stages based on different voltage gains

optimum number of stages (N_{OP}) can be derived as given by (6) [18]. For an SC converter with maximised I_L (7) [9], significantly higher power is consumed for a similar voltage gain compared to (6) [18], as shown in Fig. 6*a*. The difference in power consumption at higher voltage gains is considerable. Higher degree of non-ideality in the HV capacitor shows higher power consumption compared to the LV capacitor which has a smaller α parameter. For instance, for a voltage gain of 10 using 4 pF per stage, the SC converter consumes more than 10 mW compared to 3 mW by having $\alpha = 0.4$ and 0.1, respectively. Fig. 6*b* shows the required number of stages for a particular voltage gain given by (6) and (7). For a particular voltage gain, the SC converter with $\alpha = 0.4$ and $\beta = 0.05$ for maximising the I_L, requires 37% more stages compared to the SC converter for minimising the I_L. Besides that, by having a lower α, we can further reduce the required number of stages for a particular voltage gain as shown in Fig. 6*b*. To reduce the effect of non-ideality in HV capacitors, a charge recycling technique which significantly improves the power consumption of the SC converter will be presented in Section 6

$$N_{\text{op\_min}} = \left(1 + \sqrt{\frac{\alpha}{1+\alpha}}\right)\left(\frac{V_{\text{out}}}{V_{DD}} - 1\right) \tag{6}$$

$$N_{\text{op\_max}} = 2(1+\beta)\left(\frac{V_{\text{out}}}{V_{DD}} - 1\right) \tag{7}$$

5.5 Design example

To better understand the use of the analysis presented, consider an SC converter for generating a 30 V voltage with a very small output current of 10 μA and an input voltage of 3.3 V. Assuming parameter $\alpha = 0.4$, we obtain the optimum number of stages as being 13, given by (6). Based on (7), the required number of stages increases to 17 if more output current is needed. For a switching frequency of 25 MHz, the charging capacitor per stage is about 0.32 pF based on (1). We rewrite (4) against N_{OP} as given by (8). The loss in transistors that was neglected in the derivation of (6) in [18] has now been considered by (8) for more accurately predicting the output performance of the SC converter. A similar or slightly lower output voltage that defined in (6) will be obtained by (8) by having a negligible loss from the transistors.

Based on the presented analysis, the design area of the SC converter for HV gain and power efficiency in a small size has been identified and developed as shown in Fig. 7. In summary, the number of stages of the SC converter depends on the required voltage gain and the technological parameter α, which gives the degree of non-ideality of the capacitor for a given technology. The size of charging capacitors is independent of the number of stages, but it depends on the required current capability of the converter. For an SC converter targeted at RF MEMS applications, a smaller charging capacitor, for example 1 pF rather than 5 pF, can be used without affecting the output voltage, as shown in Fig. 7. The presented analysis and synthesis on

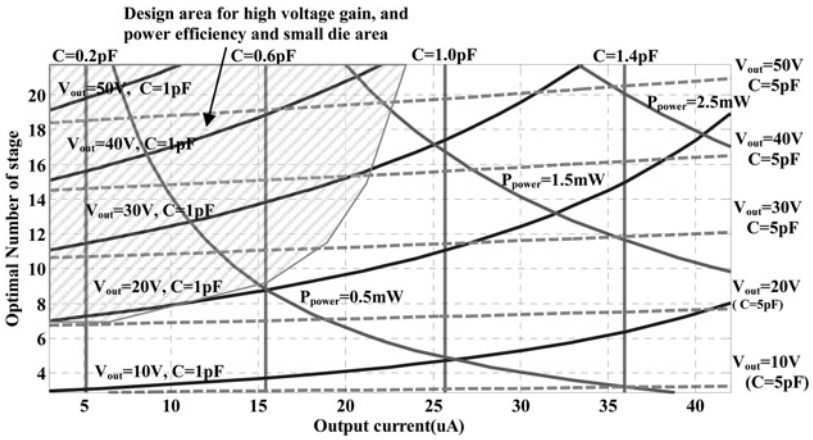

Fig. 7 *Design area of an SC DC–DC converter with an operating frequency of $f = 25$ MHz, with the assumption that parasitic capacitance loss of $\alpha = 0.4$, and a constant threshold voltage of 0.7 V from the transistors*

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the SC converter enable the design of a HV gain and low power consumption CMOS controller for RF MEMS switches in a small die area

$$V_{\text{out}} = (N_{\text{OP}} + 1)V_{DD} - (N_{\text{OP}} + 1)V_{\text{TH}} - \frac{N_{\text{OP}} I_L}{Cf} \quad (8)$$

6 Improvement to the performance of HV SC DC–DC converter

In this section, we propose two effective techniques to improve the performance of the HV SC DC–DC converter in terms of voltage gain efficiency and power consumption.

6.1 Improves the voltage gain efficiency

6.1.1 Reducing the threshold voltage of the transistors: Improvement of the voltage gain efficiency of the SC DC–DC converter can be achieved by using LV transistors as charge transfer switches. The maximum technology allowable for source-bulk potential ($V_{\text{SB\_MAX}}$) or drain-bulk potential ($V_{\text{DB\_MAX}}$) in an LV transistor is less than 5 V. Thus, we need the adaptive biasing circuits as presented in previous section to maintain the V_{SB} and V_{DB} within the limit. For HV transistors (thin and thick gate oxide HV models), the $V_{\text{SB\_MAX}}$ or the $V_{\text{DB\_MAX}}$ is 50 V. The bulk of the HV transistors can directly be connected to the highest node of the converter, which is the V_{out} in this case, without the need of the adaptive biasing circuits. Although a simpler circuit can be obtained by using the HV transistors, the bulk effect because of the increment of V_{SB} as shown by (9) [20] can no longer be ignored in this case. This bulk effect will seriously diminish the output voltage of the SC converter. Thus, a lower boosted voltage is obtained by using HV transistors. The performance of the SC converter is poorer when using the thick oxide compared to the thin oxide HV transistors with reduced current drive in the transistors. The effect of thin and thick HV transistors on the performance of the SC converter will be verified in Section 7

$$V_{\text{TH}} = V_{\text{TH0}} + \gamma\left(\sqrt{|V_{\text{SB}} + 2\phi_F|} - \sqrt{|2\phi_F|}\right) \quad (9)$$

where V_{SB} is the source-bulk potential, V_{TH0} is the V_{TH} with zero V_{SB} and $2\phi_F$ is the surface potential. $\gamma = (t_{\text{ox}}/\varepsilon_{\text{ox}})\sqrt{2q\varepsilon_{\text{si}}N_A}$ is the body effect parameter, t_{ox} is gate oxide thickness, ε_{ox} is oxide permittivity, ε_{si} is the permittivity of silicon, N_A is a doping concentration, q is the charge of an electron.

6.1.2 Increasing the transconductance of the transistors: The transconductance (g_m) of the transistors is proportional to the effective gate-to-source voltage ($V_{\text{GS\_EFF}}$) as shown in (10). Hence, HV gain efficiency has dictated the use of high $V_{\text{GS\_EFF}}$. The $V_{\text{GS\_EFF}}$ is decreasing over the stages in the SC converter. This is especially obvious if using linear MOS diode-connected structure [2, 18, 21]. Weak $V_{\text{GS\_EFF}}$ causes the transistors not able to be turned on fully, thus a higher on-resistance in the transistors and eventually a smaller charge will pass to the next stage. The interleave structure of the SC converter constantly provides a high $V_{\text{GS\_EFF}}$ over stages. This is crucial for designing the SC converter with a large number of stages for a HV gain

$$g_m = \partial\left(\frac{I_{\text{D}}}{V_{\text{GS}}}\right) = \frac{W}{L}\mu_n \frac{K_{\text{ox}}\varepsilon_0}{t_{\text{ox}}}(V_{\text{GS}} - V_{\text{TH}}) = \frac{W}{L}\mu_n \frac{K_{\text{ox}}\varepsilon_0}{t_{\text{ox}}} V_{\text{GS\_EFF}} \quad (10)$$

where I_{D} is the DC drain current, $V_{\text{GS\_EFF}}$ is the effective gate-to-source voltage, which is the difference between gate-to-source voltage and the threshold voltage (i.e. V_{GS}–V_{TH}), K_{ox} is the relative permittivity of silicon dioxide and t_{ox} is the thickness of the gate oxide, ε_o is permittivity of free space (equal to 8.854×10^{-12} F/m), W/L is the width and length ratio of the transistor and μ_n is the mobility of electrons near the silicon surface.

6.2 Reducing the power consumption in parasitic capacitance

Charge recycling technique shows a significant improvement on the current consumption of the SC DC–DC converter with low-output current [22]. This technique is suitable for the CMOS controller for RF MEMS switch which has low loading characteristic. The non-ideality in the integrated-circuit capacitor is high in the current state-of-art CMOS technology especially for HV capacitors. The parasitic parameter (α) can be up to 0.4 in an HV capacitor for the technology considered [19]. A charge recycling circuit is designed for this HV SC converter as presented in Fig. 8*a*. An nMOS (MN0) is used as a switch to connect the parasitic capacitance between the first and second rows of the SC converter in every stage. The MN0 only operates at a very short period ($V3$) as shown in Fig. 8*a*. Exceeding the defined period of $V3$ leads to a leakage of the current to ground through the MN0 and eventually more current is drawn from the input supply. The $V3$ signal is developed through a NOR gate connected between CLK1 and CLK2 to ensure the non-overlap among these signals. For the clocking circuitries (CLK1 and CLK2), PMs ($M1$ and $M2$) are used before the charging capacitors (C). As CLK1 is high and CLK2 is low, $M1$ is switched on and $M2$ is switched off. The charging capacitor and also the parasitic capacitance (αC) in the SC converter is charged to V_{DD} by CLK1. As both $M1$ and $M2$ are switched off, the charges trapped in the parasitic capacitance by CLK1 in the 1st row of the converter are recycled through MN0 to the parasitic capacitance in the 2nd row of the converter at CLK2. This equalises the potential at both parasitic capacitances to $V_{DD}/2$ before CLK2 goes high. Thus, the amount of charge drawn from the power supply for charging the parasitic capacitances is half the amount needed compared to without the charge recycling circuit. Ideally, this technique reduces the dynamic current consumption ($\Delta I_{\text{Dynamic\_state}}$) to half, as by (11) which is rewritten from (3). Fig. 8*b* demonstrates the effect of the charge recycling technique on the current consumption of the SC converter

$$I_{\text{power}Q} = \Delta I_{\text{steady\_state}} + \frac{\Delta I_{\text{Dynamic\_state}}}{2}$$
$$I_{\text{power}Q} = (N+1)I_L + \frac{NC_{\text{p}}fV_{DD}}{2} \quad (11)$$

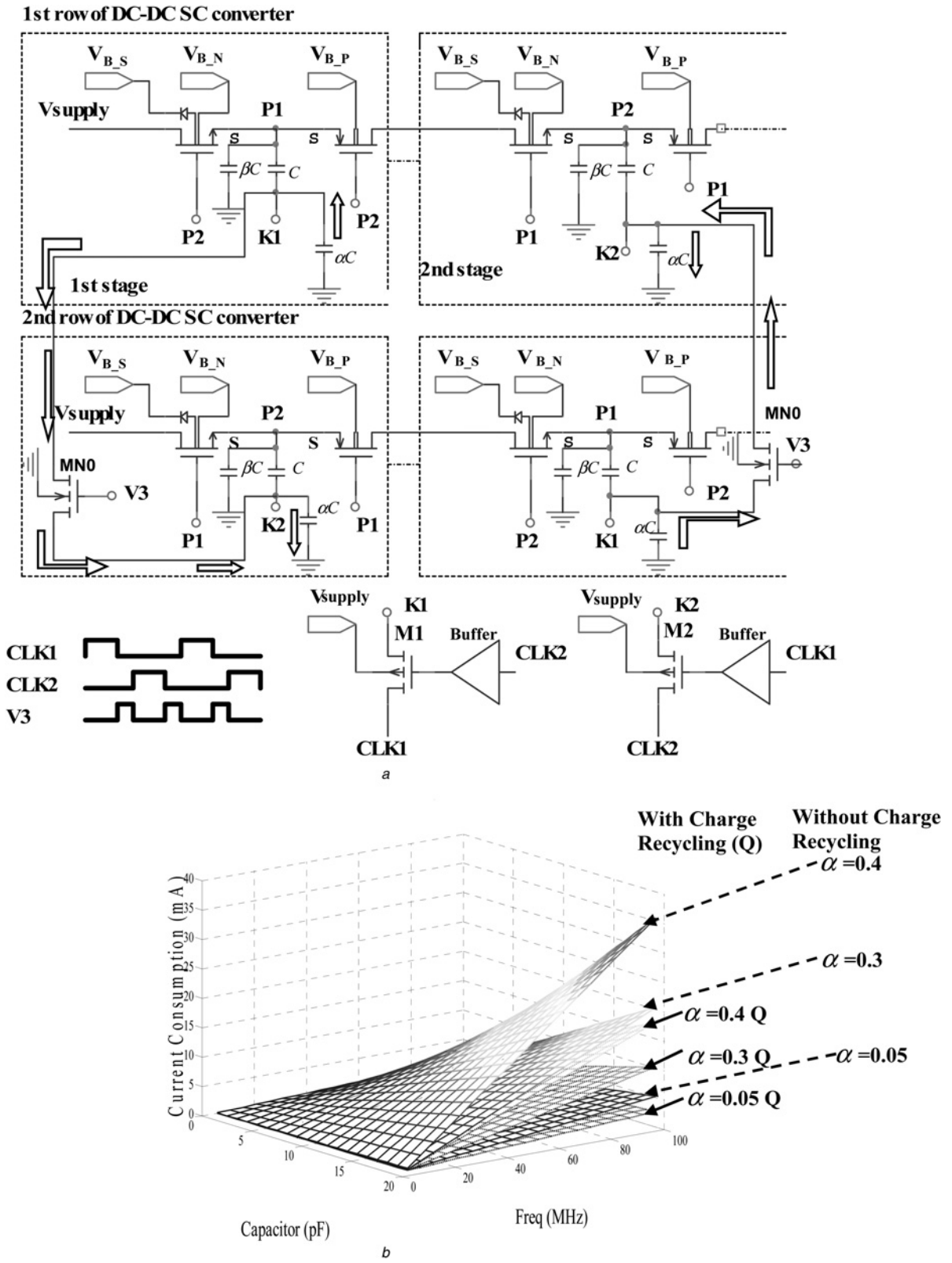

Fig. 8 *Charge recycling technique in the SC DC–DC converter*

a Circuit diagram for the implementation
b Comparison of the current consumption with and without the charge recycling technique

where N is the number of stages, V_{DD} is the power supply, I_L is the output current, C and C_P ($C_P = \alpha C$) are the charging and parasitic capacitance per stage, V_{TH} is the threshold voltage of the transistors, and f is the switching frequency.

7 Verification of the improved performance HV SC DC–DC converter

To demonstrate the effectiveness of the proposed design techniques, the HV SC DC–DC converter with a 15-stage,

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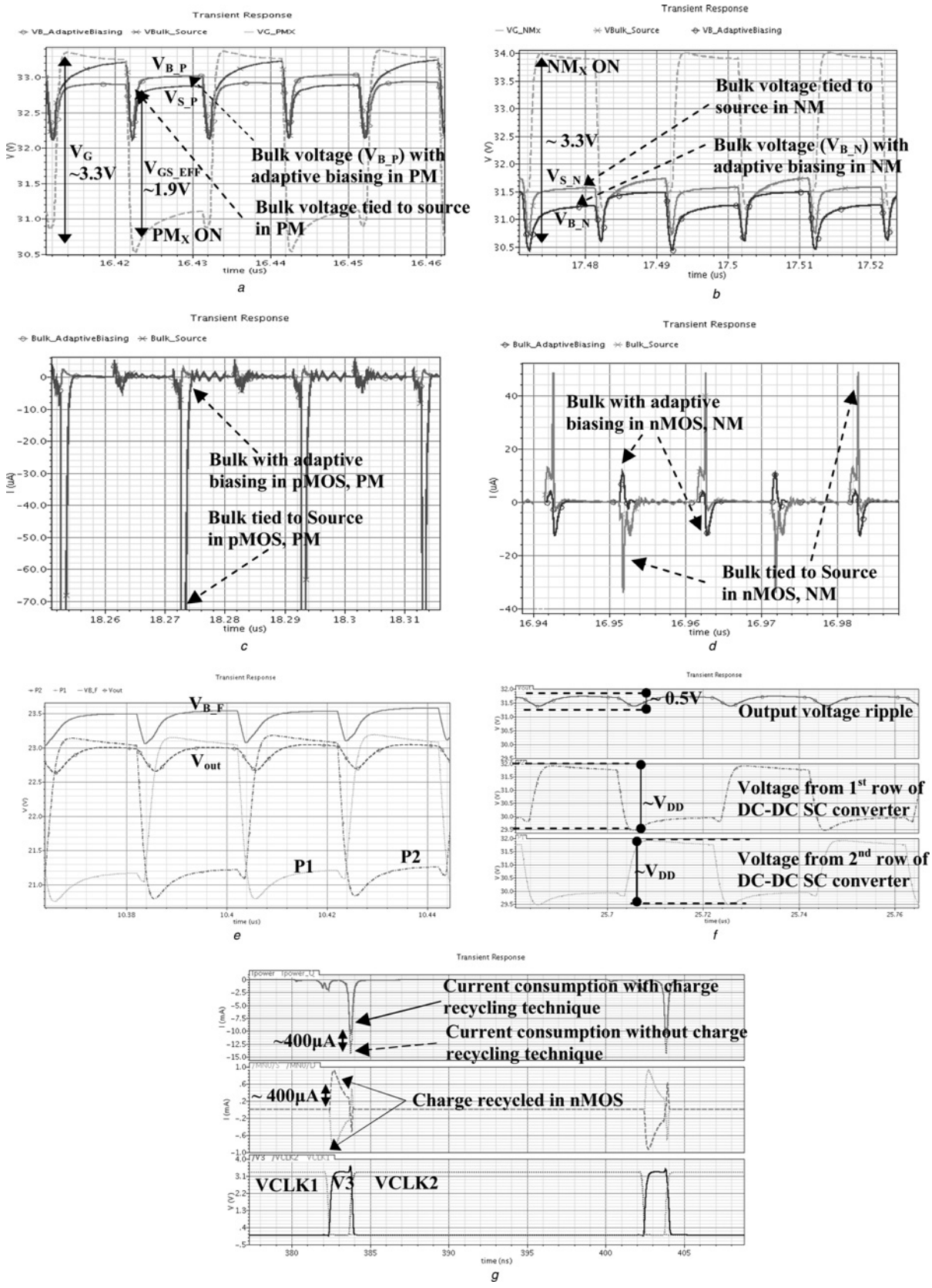

Fig. 9 *Simulation results of the proposed SC DC-DC converter*

a Bulk voltage in PM (V_{B_P}) that uses the inter stage adaptive biasing circuit is always higher than its source to switch off the vertical parasitic bipolar in PM
b Bulk voltage in NM (V_{B_N}) that uses the inter stage adaptive biasing circuit is always lower than its source to switch off the vertical parasitic bipolar in NM
c No leakage current in PM that uses the adaptive biasing circuit compared to the PM's bulk tied to its source (which have very high current peaks flowing to the substrate)
d No leakage current in NM that uses the adaptive biasing circuit compared to the NM's bulk tied to its source (which have very high current peaks flowing to the substrate)
e Bulk voltage at the output stage (V_{B_F}) that uses the final stage adaptive biasing circuit is always higher than the output voltage, *P1* and *P2* to prevent the converter from latch-up

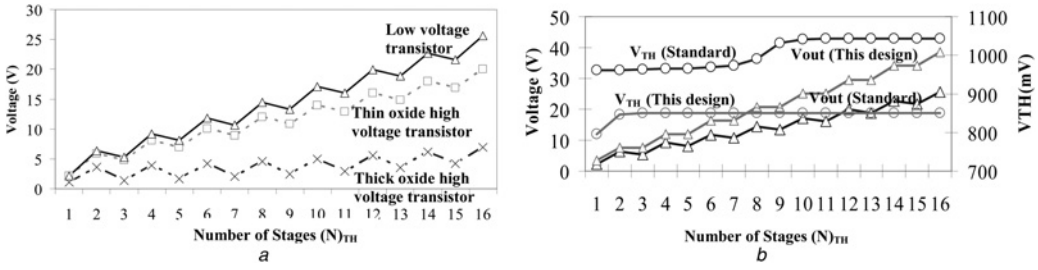

Fig. 10 *Simulation results of the SC DC–DC converter with improved voltage gain through*

a LV transistors
b Low V_{TH} in transistors

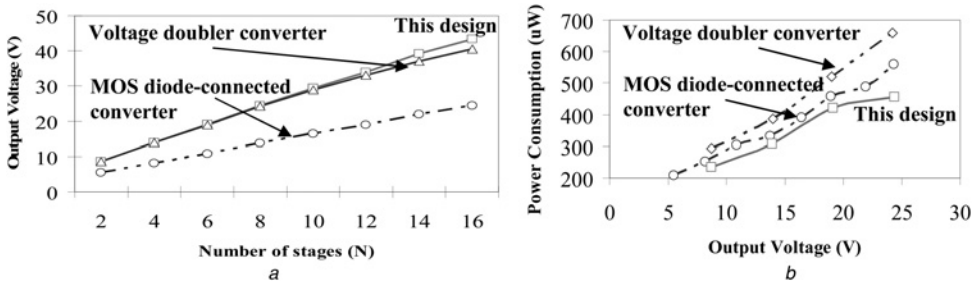

Fig. 11 *Simulation results of the improved HV SC DC–DC converter compared with the standard MOS diode-connected converter and the voltage-doubler converter, with 0.935 pF per stage at 25 MHz, in terms*

a Output voltage
b Power consumption

as presented in Fig. 2, is simulated in the 0.35 µm AMS technology. A V_{DD} of 3.3 V was supplied to the converter. The width of the PMs was set to the ratio of 2.5 to the width of the NMs in the SC converter. Since a high-output voltage of 40 V with a low output current are required, the charging capacitor (C) was set to 0.467 pF per stage per capacitor according to (6) and (1). Non-overlapping clock signals, CLK1 and CLK2, were generated for switching the converter to avoid charge leakage from short circuit paths. A floating 3.3 V LV transistor model, as presented in Section 4.1, was chosen for the SC converter. The technology allowable voltage limit (V_{GS_MAX} and V_{DS_MAX}) of the transistors is 5 V.

In this simulation, we demonstrate the effectiveness of the proposed adaptive biasing circuit for the inter- and the final-stages in the interleave structure of the SC DC–DC converter. The interleave structure of the SC converter provides a constantly effective V_{GS_EFF} for switching on and off the transistors (PM and NM) as shown in Fig. 9*a*. The V_{GS_EFF} is within the technology voltage limit of the transistor (<5 V). Thus, there is no HV overstress on the gate oxide of the devices. This V_{GS_EFF} is crucial in the SC converter with a large number of stages.

Through the inter-stage adaptive biasing circuit, the bulk of the PM (V_{B_P}) is always higher than its source (V_{S_P}) as shown in Fig. 9*a*. This eliminates the leakage current to the substrate as shown in Fig. 9*c*. Similarly, the bulk of the NM with adaptive biasing (V_{B_N}) is always lower than its source (V_{S_N}) as shown in Fig. 9*b*. Fig. 9*d* compares the leakage current in the transistors with and without using the adaptive bulk biasing. A very high-current peak is flowing to the substrate through the parasitic vertical bipolar in the transistor which without using the adaptive bulk-biasing circuit.

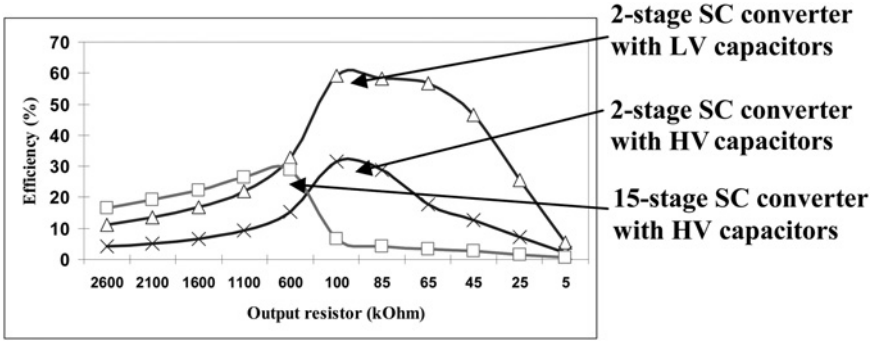

Fig. 12 *Efficiencies of a 2-stage and a 15-stage SC DC–DC converters using HV capacitors compare with a 2-stage SC converter using LV capacitors*

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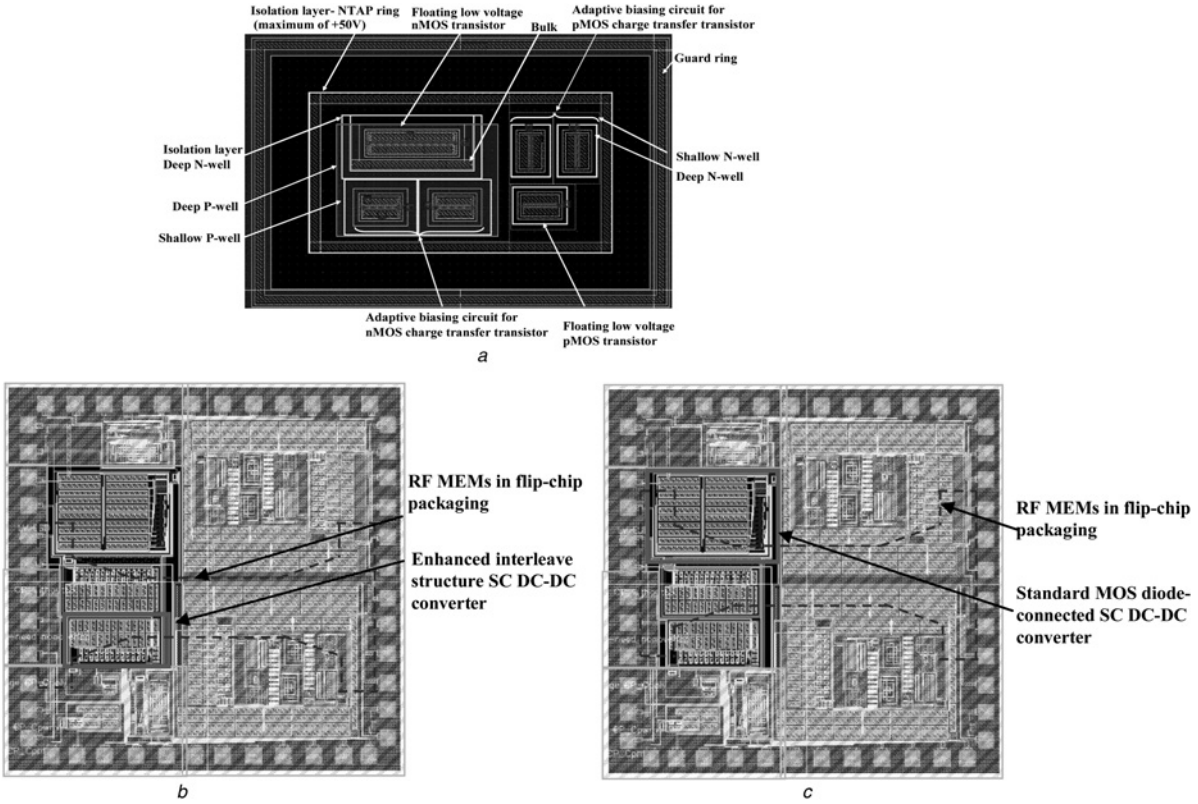

Fig. 13 *Layout of the enhanced interleave structure HV SC DC–DC converter*

a In a single stage
b In fabrication ready pad frame (with the effective area of 0.2176 mm^2)
c Compares with the standard MOS diode-connected converter that has the effective area of 0.3924 mm^2

Fig. 9*e* shows the voltages at the output stage of the SC DC–DC converter. The bulks of the pMOS (V_{B_F}) from two rows of the SC converter are biased at the highest potentials using the proposed final stage adaptive biasing circuit compared to their sources ($P1$ and $P2$) and the drain, that is V_{out} in this case as shown in Fig. 9*e*. Hence, there is no leakage current in the NM and the PM at the final stage when driving a variable capacitive MEMS load. This eliminates the SC converter from latch-up. Fig. 9*f* shows the output voltage ripple from the post-layout simulation of the converter. By complementing the voltage waveforms from the 1st and the 2nd rows of the interleave structure of the SC converter, the ripple at the output node is reduced significantly from V_{DD} to about 0.5 V.

Improvement to the power consumption of the SC converter through the charge recycling technique is presented in Fig. 9*g*. The charge was recycled between the bottom plate of parasitic capacitors through an nMOS (MN0) as described in Fig. 8*a*. The MN0 operates at a small period of non-overlapping regions of CLK1 and CLK2. A 400 µA of current is recycled between the parasitic capacitors, thus reducing the current drawn from the input supply (I_{power}) as shown in Fig. 9*g*. The saving of the current is slightly less than 50% (in ideal case) because of the losses in the additional gate and shorting in the circuit.

The improvement to the voltage gain of the SC DC–DC converter using LV transistors compared to HV transistors is demonstrated in Fig. 10*a*. More than 25% higher boosted voltage is obtained by using the LV transistors compared to the HV transistors based on same number of stages. The voltage gain of the SC converter is worse by using the thick gate oxide HV transistors. This is due to the reduced transconductance in the thick gate oxide HV transistors compared to the thin gate oxide HV transistors. The curves in Fig. 10*a* are not monotonic functions of N unlike (1) because of the charging and discharging processes in the SC converter. For instance, the even stages of the SC converter are charging, the odd stages are discharging. Thus, relatively higher voltages are obtained in the even stages, as shown in Fig. 10*a*. The differences of voltages between stages are less than 5 V which complied with the technology allowable voltage limit.

Fig. 10*b* shows the improvement to the voltage gain through reducing the V_{TH} in the transistors. V_{TH0} is a device parameter with zero V_{SB}. Increasing of V_{SB} in standard MOS diode-connected converter over stages affects the V_{TH} as described by (9). Higher V_{TH} in the transistors reduces the voltage gain of the standard MOS diode-connected converter as shown in Fig. 10*b*. A nearly constant V_{TH} is achieved by the SC converter with adaptive biasing circuit.

Figs. 11*a* and *b* show the performance of the improved HV SC DC–DC converter in this design compared to other converter's topologies. By reducing the V_{TH} and increasing transconductance of the transistors through the adaptive biasing circuits and the effective V_{GS_EFF}, the SC converter shows a higher magnitude of output voltage compared to the standard MOS diode-connected converter and the voltage doubler converter, as shown in Fig. 11*a*. The power consumption is also significantly reduced compared to the other two topologies, as shown in Fig. 11*b*.

The power efficiency (η) of the improved SC DC–DC converter is presented in Fig. 12. The maximum efficiency of a 2-stage SC converter is up to 60% by using LV capacitors and reduces nearly to half by using HV

Table 1 Summary of the design parameters and merits of performance on two-phase SC DC–DC converter

Design parameters and merits of performance	This design	[3]	[5]	[11]	[6]	[21]	[23]	[12]	[8]
Technology, μm	0.35	0.8	0.18	0.35	0.8	0.18	0.7	0.35	0.35
Number of stages	15	4	5	2	16	16	5	4	8
Capacitance per stage, pF	0.936	15	2.5	23	1	5.4	NA	6.67	Reverse Fibonacci sequence (5,3,2,1)* (33 × 1E3)
Capacitive load, pF	1	30	30	NA	28	27	NA	30	33 × 1E3
Oscillator frequency, MHz	25	5	100	25	10	75	NA	100	0.01
Voltage gain	14	3.23	5.61	2.42	10	12.33	5.4	4.611	7
Ripple ($\Delta V/V_{out}$), %	0.367	NA	16.4	0.6	0.8	1.1	NA	NA	4.3
Output current, μA	20	10	350	26	50	14.86	NA	400	NA
Current consumption, μA	249.3	NA	NA	1600	NA	NA	2800	NA	NA
Effective area, mm^2	0.2176	NA	NA	0.7888	0.33	0.72	NA	NA	NA
Proposed solutions	1. The HV design is based on an LV interleave structure 2. A small ripple (0.367%) is achieved by using a small output capacitor (1 pF) 3. A 15-stage converter is developed for a 40 V output voltage 4. LV transistors are used in the HV design for a higher voltage gain 5. Latch-up of LV transistors in an HV design is avoided through the proposed adaptive biasing circuits and the HV layout drawing 6. Charge recycling circuit is proposed to reduce the power consumption which is due to the	1. Linear structure was used in an LV operation through the internal boosted voltage 2. A large output capacitor (30 pF) was used to reduce the ripple	1. Voltage doubler structure was used to generate large output current through a high frequency 2. A 5-?stage converter was developed for a 10 V output voltage	1. Interleave structure was used 2. The design was a 2-stage converter for the output of 6.7 V and 26 μA	1. Voltage doubler structure was used 2. Voltage gain of 10 was achieved through a 16-stage of the converter 3. Two designs were developed based on LV and HV capacitors. The design which used HV capacitors consumed significant die area compared to the design using LV capacitors	1. Linear structure was used 2. A high-output voltage (14.8 V) was generated by a 1.2 V supply through a large number of stages (16) 3. Large output capacitor (27 pF) was used to reduce the ripple (1.1%)	1. Hybrid structure was used through cascoding the two linear structures 2. Medium output voltage from the 1st converter was used for pumping the 2nd converter	1. Linear structure was used 2. Positive and negative output voltages were generated through a complex clocking circuit 3. A 4-stage converter was developed for an output voltage of 8 V and a large output current of 400 μA	1. Fibonacci structure was used 2. Size of capacitors was optimised based on a reverse Fibonacci sequence 3. Large capacitors were used in the design

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capacitors. Generally, the efficiency will be significantly reduced by having higher stages as demonstrated in previous research works [5, 18]. In this work, by using presented design strategies, the maximum efficiency of the converter for a 15-stage is only slightly reduced compared to a 2-stage converter.

8 Implementation and benchmarking

8.1 Implementation

The layout for an HV design using CMOS technology is complex and not as straightforward as for an LV design [15]. Fig. 13*a* demonstrates the layout of the SC DC–DC converter in a single stage using floating LV transistors. The floating LV transistors are surrounded by an isolation layer which enables the LV transistors in an HV environment and further enhances the performance of the transistors from the substrate noise. A guard ring is drawn between the HV blocks in the layout of the SC converter. The guard ring collects the electrons emitted from a forward biased junction in the transistors and current noise from the nearby digital circuitry. The guard ring is connected to the substrate through a wide piece of metal layer to reduce substrate resistance and avoid parasitic effects. Through a proper layout drawing, we can eliminate latch-up in the LV transistors in the HV design and achieve high reliability in the SC converter.

The layouts of the improved HV SC DC–DC converter and standard MOS diode-connected converter, each providing an output voltage of approximately 40 V, are shown in Figs. 13*b* and *c*, respectively. The MOS diode-connected converter requires a 38% increase in the number of stages compared to the HV SC converter, because of the weak V_{GS_EFF} and low transconductance in the transistors. Thus, we only use a 0.2176 mm^2 die area, which is 45% smaller than the area of the standard MOS diode-connected converter.

8.2 Benchmarking

The figures of merit for the improved HV SC DC–DC converter have been compared with a number of other research works in the literature, as tabulated in Table 1. The HV SC DC–DC converter shows the lowest power consumption, the highest voltage gain and the least ripple of output voltage, even with a very small output capacitor. Furthermore, the die area in our design is small compared to previous research works. This validates the effectiveness of the proposed design strategies for a high-output voltage, low power consumption and a small size CMOS controller for RF MEMS applications.

9 Future work

The improved HV SC DC–DC converter will be integrated with RF MEMS switches through flip chip technology, which subjected to future work. The dimensions of the HV SC DC–DC converter have been customised to match exactly with the RF MEMS switches to comply with the flip chip technique. Fig. 14*a* shows the process flow for the integration of RF MEMS switches with the HV SC converter in a single package. Fig. 14*b* illustrates the integrated system underneath the encapsulation. The integrated system will result in a much smaller packaging than traditional carrier-based packaging both in area and height. The short wires in the flip chip technology will

Applications	RF MEMS	Flash-EEPROM	Flash-EEPROM	Antenna controller	NA	RF MEMS	RF MEMS	Flash memory	RF MEMS
non-ideality in HV capacitors									
7. The charging capacitors have been optimised to reduce die area (0.2176 mm^2) and power consumption (822.6 μW)									

NA – not available

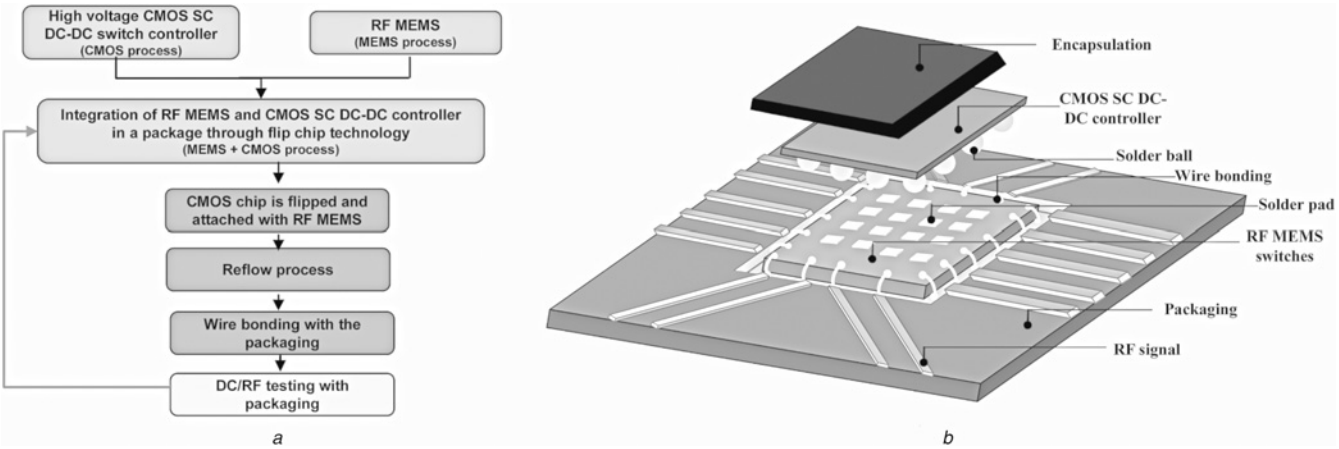

Fig. 14 *Integration of RF MEMS switches with the HV SC DC-DC converter in a single package*

a Process flow
b Illustration of the system integration between the RF MEMS switch and the CMOS SC DC-DC converter through flip chip technology

greatly reduce inductance and allow higher frequency operations. This is crucial for RF applications.

10 Conclusion

The design parameters for a high-performance CMOS-based SC DC–DC controller for RF MEMS has been analysed and synthesised. A low loading effect of the SC DC–DC converter has been identified which allows the capacitors' size and the number of stages to be optimised. Thus, this significantly reduces the die area and the power consumption of the proposed SC DC–DC converter. To further improve the performance of the SC DC–DC converter, we reduce the effects of threshold voltage drop in MOS transistors and parasitic capacitances for a higher voltage gain and lower power consumption. The adaptive biasing circuits proposed for HV SC DC–DC converters successfully eliminate the leakage current, hence avoiding latch-up that normally occurs with LV transistors when they are used in an HV design. Thus, a higher output voltage (more than 25%) is achieved with our approach compared to using HV transistors. In addition, a power saving of more than 40% is achieved through the proposed charge recycling circuit that reduces the effect of non-ideality in HV capacitors. The proposed HV SC DC–DC converter has been benchmarked against previous research and shown to have the smallest die area with a higher output voltage. In future, more work on the package integration of the HV SC DC–DC converter and RF MEMS switches will be performed.

11 Acknowledgment

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