AC VOLTAGE REGULATION OF A BIDIRECTIONAL HIGH-FREQUENCY LINK CONVERTER USING A DEADBEAT CONTROLLER

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***Abstract*—This paper presents a digital controller for ac voltage regulation of a bidirectional high-frequency link (BHFL) inverter using Deadbeat control. The proposed controller consists of inner current loop, outer voltage loop and a feed-forward controller, which imposes a gain scheduling effect according to the reference signal to compensate the steady-state error of the system. The main property of the proposed controller is that the current- and the voltage-loop controllers have the same structure, and use the same sampling period. This simplifies the design and implementation processes. To improve the overall performance of the system, additional disturbance decoupling networks are employed. This takes into account the model discretization effect. Therefore, accurate disturbance decoupling can be achieved, and the system robustness towards load variations is increased. To avoid transformer saturation due to low frequency voltage envelopes, an equalized pulse width modulation (PWM) technique has been introduced. The proposed controller has been realized using the DS1104 digital signal processor (DSP) from dSPACE. Its performances have been tested on a one kVA prototype inverter. Experimental results showed that the proposed controller has very fast dynamic and good steady-state responses even under highly nonlinear loads.**

I. INTRODUCTION

The merits of high-frequency link inverter are widely recognized. Compared to the conventional line-frequency (50-60 Hz) transformer isolated inverter, the high-frequency link inverter is lighter and smaller. In addition, due to the utilization of high-frequency transformer with less material, the cost of high-frequency link inverter could be lower. Owing to its superiority, high-frequency link inverter is now commonly used in automatic voltage regulator (AVR), uninterruptible power supply (UPS) and renewable energy source systems. In these applications, the types of loads connected to the inverter are rather uncertain. Nonlinear loads, such as rectifier in computer power supplies could cause intense distortion in the inverter waveforms. The inverter is thus required to maintain a sinusoidal output waveform, independent of the loads. This can only be achieved by employing an appropriate closed-loop control strategy.

Proportional-Integral-Derivative (PID) controller is the most commonly used in closed-loop control of many industrial systems. It is also widely applied in closed-loop regulation of pulse width modulated (PWM) inverters [1]-[3]. A method to decouple the output voltage, analogous to the "back-electromotive force (EMF)" decoupling in dc motor drive, is presented in [1]. Although digital controllers have become more prevalent over analog-based controllers, the discrete PID control is still adopted. Despite its simple structure, PID controller is known to have slow response.

Sliding mode control (SMC) has been applied for inverters control [4], [5]. It utilizes a high speed switching control law to drive the state trajectory of the plant onto a specified surface in the state-space (called sliding surface), and to keep the state trajectory on this surface for all subsequent time. Due to its discontinuous nature, SMC is insensitive to parameter variations. However, it has the drawback of chattering phenomenon. Moreover, it is not easy to locate a suitable sliding surface for the system and its steady-state response is also rather unsatisfactory [4].

Repetitive control, which provides an approach to minimize periodic disturbances, can be found in [6], [7]. In a repetitive control system, the controller is inserted in the control loop in addition to the tracking controller [7]. The repetitive action improves the steady-state response of the system when the disturbances are periodic, such as that of nonlinear rectifier loads. However, it is very difficult to obtain fast dynamic response. Furthermore, repetitive controllers usually require complicated compensation network to assure system stability.

Fuzzy logic and neural network control have grown rapidly in recent years. Extensive research has been carried out for various applications, including control of inverters [8], [9]. Fuzzy logic and neural network are nonlinear and adaptive in nature, thus provide robust performance under parameter variations and load disturbances. However, it is still lack of a systematic procedure for designing the fuzzy control rules. It depends entirely on practical experiences of the designer. On the other hand, many training examples have to be obtained for neural network control systems. The training process is usually time-consuming.

Deadbeat control is one of the most attractive control techniques as is exhibits very fast dynamic response. In this control, any nonzero error vector will be driven to zero in at most n sampling periods if the magnitude of the scalar control $u(k)$ is unbounded [10], where n is the order of the closed-loop system. Several deadbeat control schemes have been developed and applied in power electronics ever since its introduction by Gokhale *et al.* [11] for PWM inverter control. For inverters control, the deadbeat control algorithm is derived based on the state-space model of the system. Early works in [11]-[13] have derived the deadbeat solutions based on linear load assumption, thus the system performance deteriorates if a nonlinear load is applied. It is also frequently pointed out that deadbeat control is sensitive to parameter variations. To improve the system performance and robustness

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against load variations, decoupling networks have been employed [14], [15].

In this paper, a deadbeat controller is proposed for closed-loop regulation of a bidirectional high-frequency link (BHFL) [16] inverter. The proposed controller has simple structure and thus facilitates the ease of implementation. Disturbance decoupling networks have been introduced to suppress the effect of load variations and improve system robustness. The disturbance decoupling networks are derived by taking into account the model discretization effect. As such, the system has good disturbance rejection capability. This makes the system capable of handling various types of loads. In the proposed control scheme, there is no observer or estimator applied. This is an advantage because inclusion of observer might introduce estimation errors.

The paper is organized as follows: Section II describes the circuit configuration, the operating principle and the plant modeling of the BHFL inverter. Section III details the proposed deadbeat control technique, and the design of the controller. Section IV explains the realization of the proposed controller, and a solution to avoid transformer saturation. Section V shows the system verification through experimental results. Section VI concludes the entire work.

II. System Description And Plant Modeling

A. System Description of BHFL Inverter

The BHFL inverter, which is the plant to be controlled, is shown in Fig. 1. The main conversion circuits are the high-frequency PWM bridge, active rectifier and polarity-reversing bridge. On the transformer primary side, the dc source voltage (V_{dc}) is converted into a high-frequency PWM voltage (v_{HF}) by the high-frequency PWM bridge. This voltage is then isolated and stepped-up using a center-tapped high-frequency transformer. Next, the high-frequency PWM voltage is rectified using the active rectifier. The active rectifier, which consists of power switches and anti-parallel diodes, enables bidirectional power flow. For transfer of power from the source to load, the diodes are utilized and for reverse power flow, the power switches S3 and $\overline{S3}$ are turned on. A regenerative snubber circuit is used to suppress any voltage spikes caused by the leakage inductance of the transformer secondary. The snubber circuit is not shown in the figure for simplicity. The rectified PWM voltage, v_{pwm_rect} is then low-pass filtered to obtain the rectified fundamental component, v_{rect}. Finally, using the polarity-reversing bridge, the second half of the rectified sinusoidal voltage is unfolded at zero-crossing, and a sinusoidal voltage, v_o is obtained. The timing diagram for the key waveforms at the principal conversion stages is shown in Fig. 2.

The power switches of the BHFL inverter are driven by three gate control signals, namely v_{pwm}, v_s and v_u. The timing diagram of these control signals is shown in Fig. 3. These control signals will then go through a series of logic gates shown in Fig. 4, and become the gating signal for each power switch. Referring to Fig. 3, v_{pwm} is a rectified sinusoidal pulse width modulated (SPWM) pulse-train, and v_s is a square-wave signal with frequency half of v_{pwm}. The unfolding signal, v_u is a 50Hz sign waveform. In Fig. 4, it can be seen that the resulting signals of logical operations between v_{pwm} and v_s are used to drive the power switches of the high-frequency PWM bridge. Note that v_s is used to alternatively split the rectified SPWM pulses. On the transformer secondary side, v_s is used to drive the power switches of the active rectifier. The power switches of the polarity-reversing bridge are driven by v_u.

B. Plant Modeling

To design a closed-loop controller for the BHFL inverter, the plant is first modeled using the state-space averaging technique [17]. Referring to Fig. 1, it is assumed that the dc source voltage, V_{dc} is constant. The inverter switching frequency is considered to be high enough compared to the 50Hz sinusoidal modulating frequency. The high-frequency transformer is assumed to be operating in the linear area. As such, the high-frequency PWM bridge and the transformer can be modeled as constant gains. The polarity-reversing bridge is only operated at line-frequency (50Hz), thus its dynamics can be ignored. With these assumptions, the dynamics of the system can be simplified to a *LC* low-pass filter connected to the load. Choosing the filter inductor current i_L and filter capacitor voltage v_{rect} as the state variables, the state-space representation and output equation of the system are derived:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{rect}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_{rect} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} u + \begin{bmatrix} 0 \\ -\frac{1}{C} \end{bmatrix} i_{or} \quad (1)$$

$$v_{or} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_{rect} \end{bmatrix} \quad (2)$$

Based on (1) and (2), the system dynamic model is represented by the block diagram in Fig. 5. It can be seen that the load current acts as a disturbance on the output voltage, while the output voltage acts as a disturbance on the inductor current.

Since the controller is to be implemented using a digital processor, the dynamic model of the system is discretized. With a sampling period of T_s, the discrete-time state-space equations can be written as:

$$x(k+1) = Ax(k) + Bu(k) + B_d i_{or}(k) \quad (3)$$

$$v_{or}(k) = Cx(k) \quad (4)$$

where

$$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} = \begin{bmatrix} \cos(\omega T_s) & -\frac{1}{\omega L}\sin(\omega T_s) \\ \frac{1}{\omega C}\sin(\omega T_s) & \cos(\omega T_s) \end{bmatrix}$$

$$B = \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{\omega L}\sin(\omega T_s) \\ 1-\cos(\omega T_s) \end{bmatrix} \quad B_d = \begin{bmatrix} B_{d1} \\ B_{d2} \end{bmatrix} = \begin{bmatrix} 1-\cos(\omega T_s) \\ -\frac{1}{\omega C}\sin(\omega T_s) \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

$x(k)=\begin{bmatrix} i_L(k) \\ v_{rect}(k) \end{bmatrix}$ is the state vector, and $\omega=\frac{1}{\sqrt{LC}}$ is the cut-off frequency of the low-pass filter.

From (3) and (4), the discrete-time equations can be rewritten:

$$u(k)=\frac{1}{B_1}i_L(k+1)-\frac{A_{11}}{B_1}i_L(k)-\frac{A_{12}}{B_1}v_{or}(k)-\frac{B_{d1}}{B_1}i_{or}(k) \quad (5)$$

$$i_L(k)=\frac{1}{A_{21}}v_{or}(k+1)-\frac{A_{22}}{A_{21}}v_{or}(k)-\frac{B_2}{A_{21}}u(k)-\frac{B_{d2}}{A_{21}}i_{or}(k) \quad (6)$$

From (5) and (6), it can be seen that additional disturbance terms appear because of model discretization. As compared to the continuous-time model, there exist two disturbances instead of one, acting on the inductor current and output voltage. The current and voltage disturbance terms can be written as:

$$i_d(k)=-\frac{A_{12}}{B_1}v_{or}(k)-\frac{B_{d1}}{B_1}i_{or}(k) \quad (7)$$

$$v_d(k)=-\frac{B_2}{A_{21}}u(k)-\frac{B_{d2}}{A_{21}}i_{or}(k) \quad (8)$$

Based on the discrete-time equations, the digital model of the system can be represented by the block diagram in Fig. 6, where z^{-1} denotes a unit delay.

III. CONTROLLER DESIGN

Fig. 7 shows the proposed Deadbeat controller for the BHFL inverter. It consists of inner current loop controller, outer voltage loop controller and a feed-forward controller. The feed-forward controller, which imposes a gain scheduling effect according to the reference signal, is used to compensate the steady-state error of the system. From the discrete-time model of the plant in Fig. 6, it is known that there are disturbance terms acting on the inductor current and output voltage. These disturbances are compensated using additional decoupling networks in (7) and (8). With that, the Deadbeat controller has good disturbance rejection capability and improved robustness towards load variations.

A. Current Loop Controller

Fig. 8(a) shows the inner current loop controller. The current disturbance decoupling network is added to compensate the disturbances acting on the inductor current. Canceling the current disturbance coupling allows a simple gain, K_i to be applied in forming the inner current loop. Referring to Fig. 8(a), the current loop control law can be derived:

$$u(k)=K_i\left[i_{ref}(k)-i_L(k)\right]+i_d(k) \quad (9)$$

where $u(k)$ is the control signal applied to the PWM modulator, $i_{ref}(k)$ is the inductor current reference generated by the outer voltage loop, and $i_d(k)$ is the current disturbance decoupling network from (7). Fig. 8(b) shows the simplified current loop. The discrete-time open-loop transfer function is:

$$G_i(z)=\frac{B_1z^{-1}}{1-A_{11}z^{-1}}=\frac{\sin(\omega T_s)z^{-1}}{\omega L\left[1-\cos(\omega T_s)z^{-1}\right]} \quad (10)$$

The corresponding discrete-time closed-loop transfer function of the current loop is:

$$C_i(z)=\frac{i_L(k)}{i_{ref}(k)}=\frac{K_iG_i(z)}{1+K_iG_i(z)}=\frac{K_iB_1z^{-1}}{\left[K_iB_1-A_{11}\right]z^{-1}+1}$$
$$=\frac{K_i\sin(\omega T_s)z^{-1}}{\left[K_i\sin(\omega T_s)-\omega L\cos(\omega T_s)\right]z^{-1}+\omega L} \quad (11)$$

From (11), the characteristic equation of the closed-loop current controller can be written as:

$$z-\left[A_{11}-K_iB_1\right]=0 \quad z-\left[\cos(\omega T_s)-K_i\frac{1}{\omega L}\sin(\omega T_s)\right]=0 \quad (12)$$

In discrete-time control systems, the closed-loop poles or the roots of the characteristic equation must lie within the unit circle in z-plane for the system to be stable [10]. Therefore, the range of K_i for the system to be stable is:

$-1<\left[A_{11}-K_iB_1\right]<1$, $\left|\frac{A_{11}-1}{B_1}\right|<K_i<\left|\frac{A_{11}+1}{B_1}\right|$ and

$$\left|\frac{\omega L\left[\cos(\omega T_s)-1\right]}{\sin(\omega T_s)}\right|<K_i<\left|\frac{\omega L\left[\cos(\omega T_s)+1\right]}{\sin(\omega T_s)}\right| \quad (13)$$

To achieve Deadbeat response, the root is to be placed at the origin of the z-plane ($z=0$). Hence, the current loop gain, K_i is designed as:

$$K_i=\frac{A_{11}}{B_1}=\frac{\omega L\cos(\omega T_s)}{\sin(\omega T_s)} \quad (14)$$

Substituting (14) into (11) yields:

$$i_L(k)=A_{11}z^{-1}i_{ref}(k)=\cos(\omega T_s)z^{-1}i_{ref}(k) \quad (15)$$

When ωT_s is sufficiently small, $\sin(\omega T_s)\approx\omega T_s$ and $\cos(\omega T_s)\approx 1$. Therefore, (15) can be written as $i_L(k)=z^{-1}i_{ref}(k)$, which is the Deadbeat response.

B. Voltage Loop Controller

Fig. 9(a) shows the outer voltage loop controller. The voltage disturbance decoupling network is added to compensate the disturbances acting on the output voltage. This will improve the robustness of the system towards load variations, enabling various types of loads to be connected. Besides, it also acts as an additional current loop command to produce the needed load current without waiting for errors in voltage to occur.

The design procedure of the voltage loop controller is similar to the current loop controller. The voltage loop gain, K_v is applied to achieve Deadbeat response. From Fig. 9(a), the voltage loop control law is derived:

$$i_{ref}(k)=K_v\left[v_{ref}(k)-v_{or}(k)\right]+v_d(k) \quad (16)$$

where $i_{ref}(k)$ is the generated current loop command for the inner current loop, $v_{ref}(k)$ is the rectified sinusoidal voltage reference, and $v_d(k)$ is the voltage disturbance decoupling network from (8). Fig. 9(b) shows the simplified voltage loop. It can be noted that the inner current loop is viewed as a constant gain, with the condition of current loop is well designed. The corresponding discrete-time open-loop transfer function is:

$$G_v(z)=\frac{A_{21}z^{-1}}{1-A_{22}z^{-1}} \quad =\frac{\sin(\omega T_s)z^{-1}}{\omega C\left[1-\cos(\omega T_s)z^{-1}\right]} \tag{17}$$

The discrete-time closed-loop transfer function of the voltage loop is:

$$C_v(z)=\frac{v_{or}(k)}{v_{ref}(k)}=\frac{K_vG_v(z)}{1+K_vG_v(z)} \quad =\frac{K_vA_{21}z^{-1}}{\left[K_vA_{21}-A_{22}\right]z^{-1}+1}$$
$$=\frac{K_v\sin(\omega T_s)z^{-1}}{\left[K_v\sin(\omega T_s)-\omega C\cos(\omega T_s)\right]z^{-1}+\omega C} \tag{18}$$

From (18), the characteristic equation of the closed-loop voltage controller can be written as:

$$z-\left[A_{22}-K_vA_{21}\right]=0\,, \quad z-\left[\cos(\omega T_s)-K_v\frac{1}{\omega C}\sin(\omega T_s)\right]=0 \tag{19}$$

For the system to be stable, the range of K_v is:

$$-1<\left[A_{22}-K_vA_{21}\right]<1\,, \quad \left|\frac{A_{22}-1}{A_{21}}\right|<K_v<\left|\frac{A_{22}+1}{A_{21}}\right|$$
$$\left|\frac{\omega C\left[\cos(\omega T_s)-1\right]}{\sin(\omega T_s)}\right|<K_v<\left|\frac{\omega C\left[\cos(\omega T_s)+1\right]}{\sin(\omega T_s)}\right| \tag{20}$$

Similar to the current loop gain, the voltage loop gain, K_v is designed such that the root of the system can be placed at the origin of z-plane:

$$K_v=\frac{A_{22}}{A_{21}} \quad =\frac{\omega C\cos(\omega T_s)}{\sin(\omega T_s)} \tag{21}$$

Substituting (21) into (18) yields:

$$v_{or}(k)=A_{22}z^{-1}v_{ref}(k) \quad =\cos(\omega T_s)z^{-1}v_{ref}(k) \tag{22}$$

When ωT_s is sufficiently small, $\sin(\omega T_s)\approx\omega T_s$ and $\cos(\omega T_s)\approx 1$. Therefore, (22) can be written as $v_{or}(k)=z^{-1}v_{ref}(k)$, which is the deadbeat response.

C. *Feed-forward Controller*

From (22), it can be seen that there is a steady-state error in the output voltage if ωT_s is not sufficiently small. To compensate the steady-state error, a feed forward controller is added to the output of the voltage loop controller. The feed forward controller imposes a gain scheduling effect on the voltage loop controller according to the reference signal. The voltage loop with inclusion of feed forward controller is shown in Fig. 10 and the discrete-time closed-loop transfer function is derived:

$$\frac{v_{or}(k)}{v_{ref}(k)}=\frac{\left[K_v+K_f\right]A_{21}z^{-1}}{\left[K_vA_{21}-A_{22}\right]z^{-1}+1} \quad =\frac{\left[K_v+K_f\right]\sin(\omega T_s)z^{-1}}{\left[K_v\sin(\omega T_s)-\omega C\cos(\omega T_s)\right]z^{-1}+\omega C} \tag{23}$$

To ensure Deadbeat response, the feed forward gain, K_f is chosen as:

$$K_f=\frac{1-A_{22}}{A_{21}} \quad =\frac{\omega C\left[1-\cos(\omega T_s)\right]}{\sin(\omega T_s)} \tag{24}$$

Substituting (21) and (24) into (23), $v_{or}(k)=z^{-1}v_{ref}(k)$ is obtained, which ensures the Deadbeat response.

IV. Hardware Realization and Practical Issues

A 1kVA prototype inverter has been constructed. The proposed Deadbeat controller is implemented using the DS1104 digital signal processor (DSP) from dSPACE (64-bit floating-point processor with TMS320F240 Slave DSP). Hall-effect current sensors, HY10-P and voltage sensor, LV25-P are used to sense the feedback signals. The signal conditioning such as noise filtering and signal amplification are performed in software using the DS1104 DSP. Table I provides the parameters of the prototype inverter.

TABLE I: Parameters of The Prototype Inverter

Parameter	Value
Switching frequency	f_{sw} = 25kHz
Nominal input voltage	V_{dc} = 150V
Rated output voltage	v_o = 240V_{rms}
Rated output frequency	f = 50Hz
Rated output power	P_o = 1kVA
Filter inductor	L = 0.66mH
Filter capacitor	C = 6.8μF
Sampling period	T_s = 40μs

In practice, the pulse width of kth pulse and (k+1)th pulse are not equal in v_{HF} due to the SPWM switching, as shown in Fig. 11. This results in a low-frequency voltage envelope to exist over the entire waveform. The low-frequency voltage envelope may lead to possible transformer saturation, as the transformer is designed for high frequency operation. To overcome this problem, an equalized pulse PWM technique is proposed, where the pulse width of the kth pulse is equalized to the (k+1)th pulse. Through this approach, the use of dc blocking capacitor at the primary side of transformer [18] is avoided. Fig. 12 illustrates the timing diagram of the equalized pulse PWM generation. The equalized pulse is calculated using the following equation:

$$u(j)=\frac{u(k-2)+u(k-1)}{2} \tag{25}$$

where j denotes the number of control period sample, and k denotes the number of carrier period sample. Note that the real-time application of the proposed control algorithm including this equalized pulse PWM technique is implemented using a single timer. The equalized pulse is updated once in two carrier periods, where the carrier period equals to the defined timer period.

V. Experimental Results And Discussion

To verify the performances of the proposed deadbeat controller, the prototype inverter has been tested under various types of loads. Besides the resistive and inductive loads, the system is also tested under phase controlled triac load and full-bridge rectifier load. The parameters of the test loads are summarized in Table II.

TABLE II: Parameters of The Test Loads

Load	Value
Nominal resistive load	R = 62.5Ω
Inductive load at 0.7 PF	R_i = 62.5Ω L_i = 183mH
Nonlinear load (Full-bridge load)	R_d = 500Ω C_d = 470μF

The output voltage and current waveforms under resistive load are shown in Fig. 13. The output voltage total harmonic distortion (THD) is 1.5%. The output voltage and current waveforms under inductive load are

shown in Fig. 14. It can be seen that the system is capable of carrying bidirectional power flow. The output voltage THD under this condition is 2.2%.

Fig. 15 shows the output voltage and current waveforms under triac load commutated at $90^o/270^o$. It is observed that the voltage drop can be recovered quickly after the large current transient. The voltage transient is reduced to 10% in 0.32ms.

To test a worst case loading, the system is connected to a full-bridge rectifier. This type of load is considered to be the most severe type. It causes intense voltage distortion due to the highly distorted current. Fig. 16 shows the steady-state output voltage and current waveforms under full-bridge rectifier load. As can be seen, the output voltage waveform has good quality with low distortion. The output voltage THD under this condition is 3.8%. This can be attributed to the improved robustness of the system.

VI. CONCLUSIONS

A deadbeat controller for closed-loop regulation of the BHFL inverter has been described in this paper. The proposed control scheme regulates both the output voltage and inductor current using the multicolor control strategy. A feed-forward controller is incorporated to compensate steady-state error of the system. Accurate disturbance decoupling makes the system capable of handling various types of loads. An equalized pulse PWM technique has also been introduced to avoid transformer saturation caused by low frequency voltage envelopes. The proposed controller, including the pulse equalization and signal conditioning, have been realized in DS1104 DSP using a single timer. The laboratory experiments on a 1kVA prototype inverter verified the proposed control strategy. The experimental results show that the controller exhibits very fast dynamic response under cyclic step load changes. Besides, a sinusoidal voltage waveform with low distortion can be maintained even under highly nonlinear loads. The closed-loop BHFL inverter is thus suitable for wide area of applications, both in grid-connected and stand-alone configurations.

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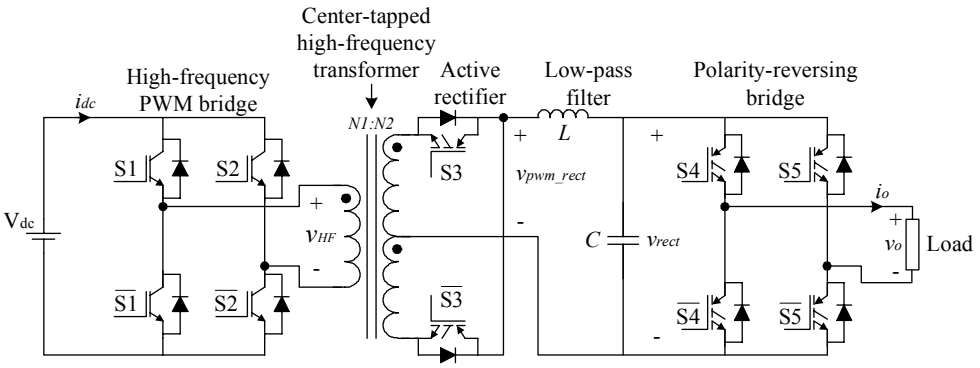

Fig. 1. Bidirectional high-frequency (BHFL) inverter.

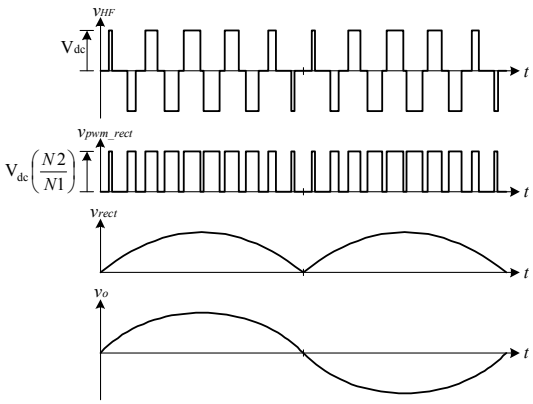

Fig. 2. Key waveforms at the principal conversion stages.

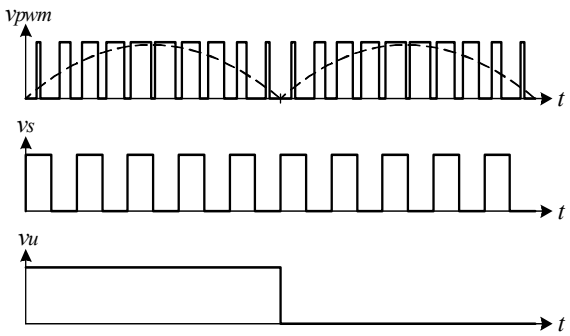

Fig. 3. Gate control signals for the BHFL inverter.

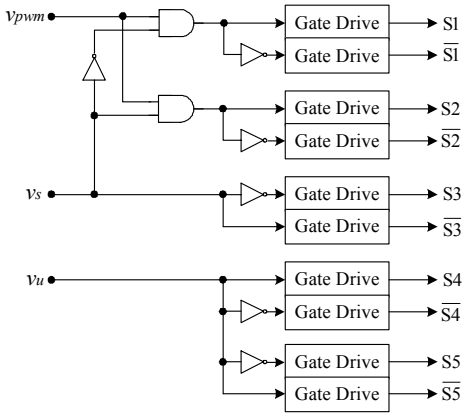

Fig. 4. Interface between control signals and power switches.

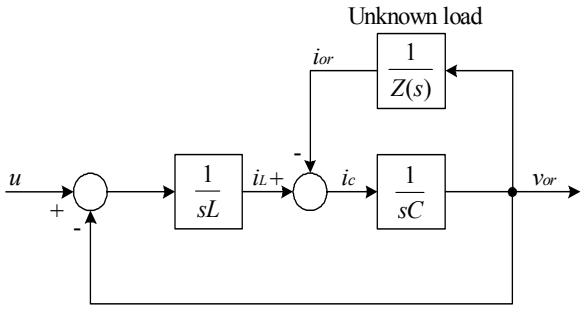

Fig. 5. Continuous-time model of the BHFL inverter.

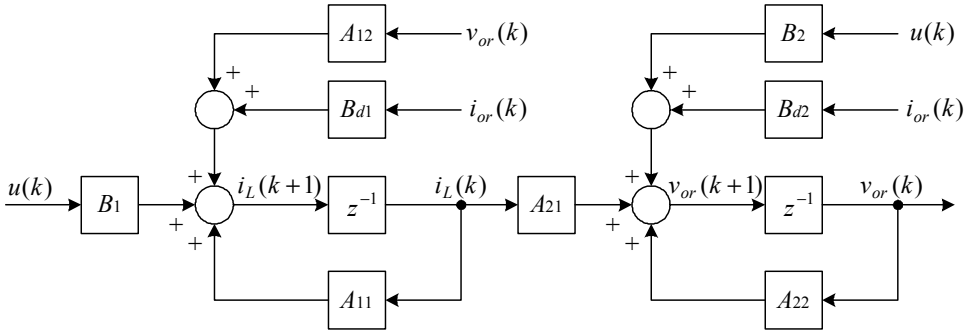

Fig. 6. Discrete-time model of the BHFL inverter.

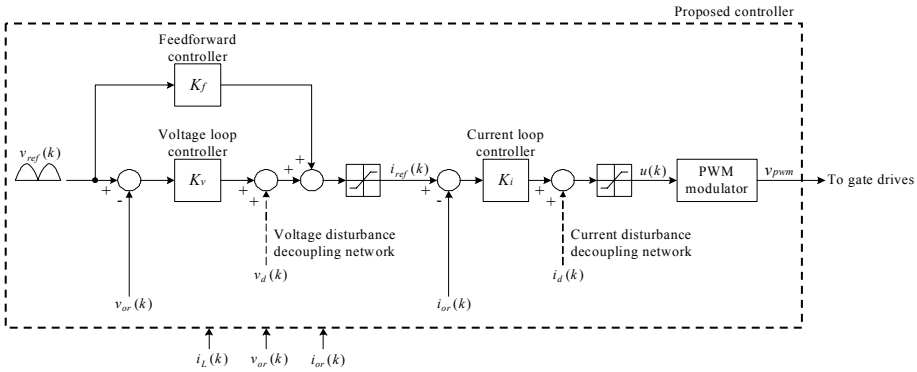

Fig. 7. Proposed Deadbeat controller for the BHFL inverter.

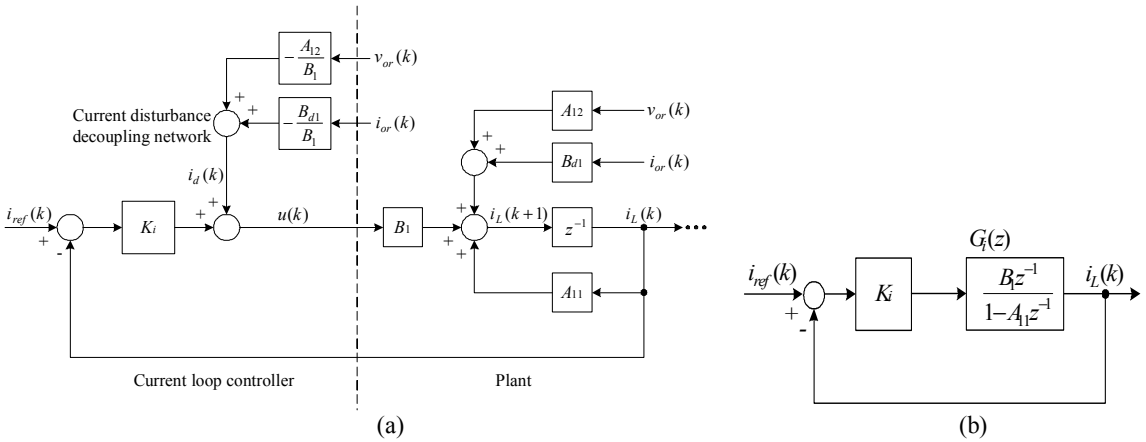

Fig. 8. Current controller (a) current loop (b) simplified current loop.

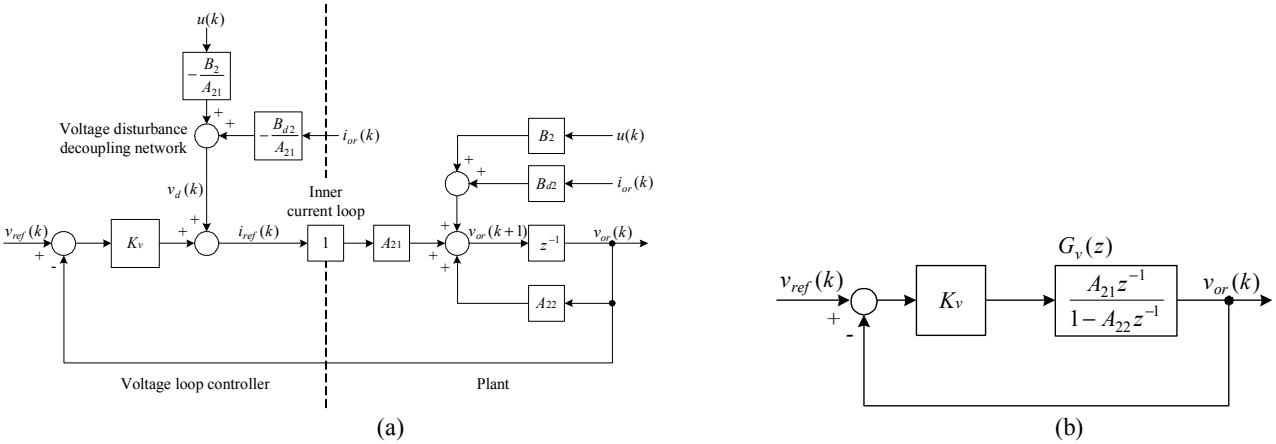

Fig. 9. Voltage controller (a) voltage loop (b) simplified voltage loop.

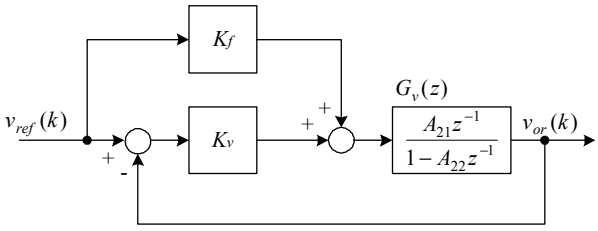

Fig. 10. Voltage loop with feed forward controller.

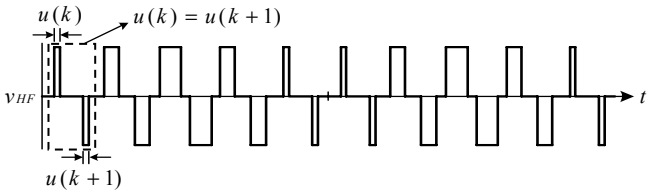

Fig. 11. Timing diagram of v_{HF} without pulse equalization.

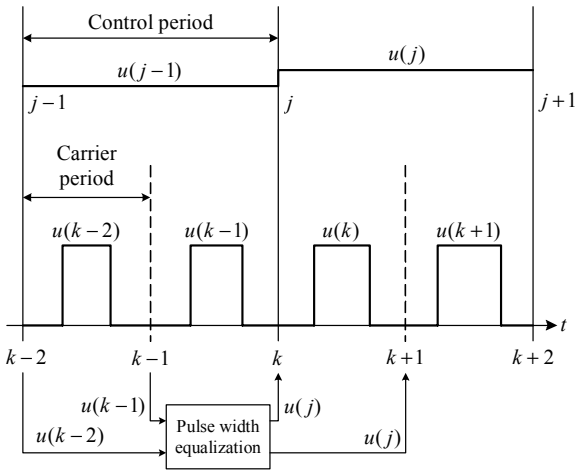

Fig. 12. Timing diagram of equalized pulse PWM generation.

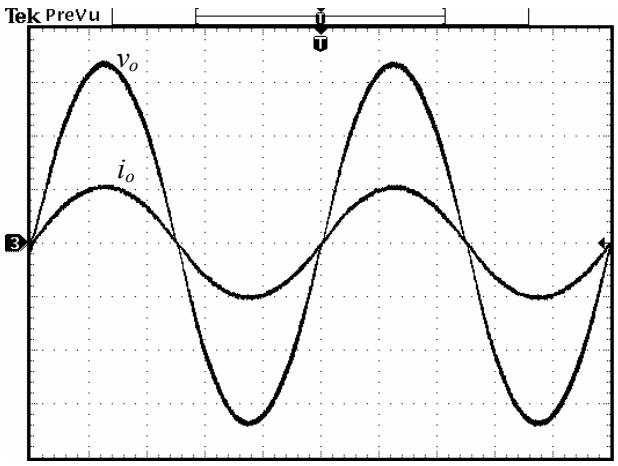

Fig. 13. Output voltage and current for resistive load.
Vertical scale: output voltage 100V/div,
output current 5A/div, Time scale: 4ms/div

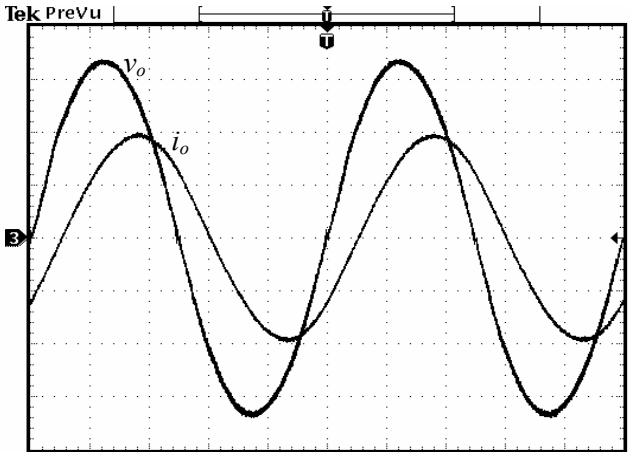

Fig. 14. Output voltage and current for inductive load.
Vertical scale: output voltage 100V/div,
output current 2A/div, Time scale: 4ms/div

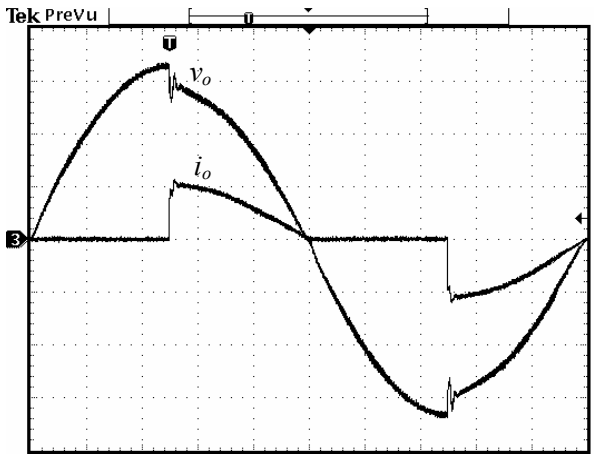

Fig. 15. Output voltage and current for triac load.
Vertical scale: output voltage 100V/div,
output current 5A/div, Time scale: 2ms/div

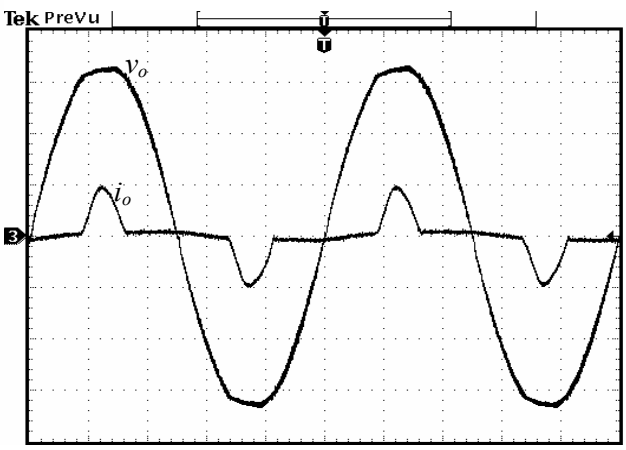

Fig. 16. Output voltage and current for rectifier load.
Vertical scale: output voltage 100V/div,
output current 5A/div, Time scale: 4ms/div