Low voltage CMOS Schmitt Trigger in 0.18μm technology

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Abstract: This paper presents the effect of source voltage on performance of proposed Schmitt Trigger circuit. The proposed circuit was designed based on Conventional Schmitt Trigger by manipulating the arrangement of transistors and the width-length ratio. The simulation results have been carried out based on Mentor Graphics software in term of propagation delay. The circuit layout has been designed and checked by using design rule check (DRC) and layout versus schematic (LVS) method. From these results, the proposed full swing CMOS Schmitt Trigger was able to operate at low voltage (0.8V-1.5V)

Keywords: DRC, LVS, mentor graphic, schmitt trigger, width-length ratio.

I.   INTRODUCTION

The Schmitt Trigger circuit is widely used in analogue and digital circuit to solve the noise problem. Beside that this circuit is widely design in various styles in order to drive the load with fast switching, low power dissipation and low-supply voltage, especially for high capacitive load problem [1].

Conventional Schmitt Trigger is shown in Fig. 1 and the detail design is presented in [2] where the switching thresholds are dependent on the ratio of NMOS and PMOS. However, this circuit will exhibit racing phenomena after the transition starts. Therefore in this paper, we proposed CMOS Schmitt Trigger circuit which is capable to operate in low voltage (0.8V-1.5V) at high capacitance, less propagation delay and stable hysteresis width. By lowering the supply voltage is an effective method to achieve low power operation [3]-[4].
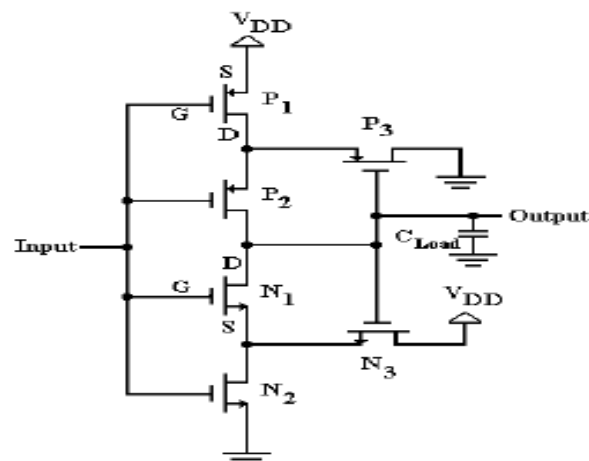

Figure 1: The Conventional Schmitt Trigger

1.1. CIRCUIT DESCRIPTION

The proposed Schmitt Trigger [5] is shown in Fig. 2 and is categorized into two parts which is Part 1 and Part 2. Similarly to Conventional Schmitt Trigger, the proposed circuit is formed by a combination of two sub-circuit, P sub-circuit (which consists of P1, P2 and P3) and N sub-circuit (which consists of N1, N2 and N3). There is no direct connection between the source voltage and ground as P sub-circuit is connected to the path between the source voltage and output while the N sub-circuit is connected between the path of output and ground. Therefore, there is no static power consumption due to no direct path between source voltage and ground.
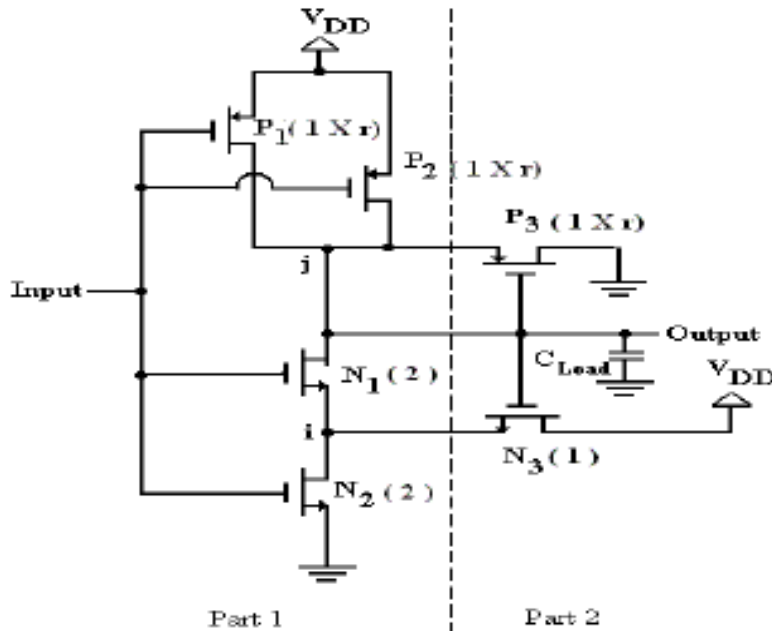
Figure 2: The Proposed Schmitt Trigger

Part 1 of the proposed circuit forms a NAND gate is designed according to De Morgan`s Theorem. Two PMOS (P1 and P2) are formed by a parallel connection while two NMOS (N1 and N2) are formed by a series connection. By designing the PMOS in parallel, the resistance of the P sub-circuit will be reduced by halves. Thus, the propagation delay can be reduced as shown in equation (1).

$$t_p = 0.69RC_L = \frac{t_{PHL} + t_{PLJH}}{2} \tag{1}$$

It is preferably to reduce PMOS delay because delay is more concentrated to PMOS due to high mobility of PMOS compare to NMOS. Part 2 of the Proposed Schmitt Trigger consists of a PMOS, (P3) and a NMOS, (N3) where both the MOSFET is directly connected through the gate terminal of each. The P3 act as pull up while the N3 act as a pull down for the output at each case.

The sizings of the transistor are set by locating the minimum component path of each sub-circuit. Each of the transistors is sized accordingly to their arrangement. For transistors that are in series, they are scaled by factor of 2 each while transistors in parallel are scaled by a factor of 1each. The PMOS and NMOS ratio is set according to equation 2 with the effective length, $L_{eff} = 0.18\mu m$ (for 0.18 technologies).

$$\left(\frac{W}{L_{eff}}\right) PMOS = r \left(\frac{W}{L_{eff}}\right) NMOS \tag{2}$$

It is recommended to widen the PMOS transistor to allow the resistance matches the pull down NMOS device. Typically, $r = 3 \rightarrow 3.5$ [6].Therefore, the ratio is set to be three maximize the noise margin and to create a circuit with symmetrical voltage-transfer characteristic (VTC). By increasing the width of PMOS, it moves the switching threshold voltage towardsV_{DD}, which makes the hysteresis width more rectangles which are desirable in a Schmitt Trigger design.

When the input is low, only the P sub-circuit will be considered and causes the output to be high (equal toV_{DD}). During this condition, both P1 and P2 are on, but P3 is off (because $V_{SG} < |V_{tp}|$ as P3`s source voltage and gate voltage is equal). Therefore, the output voltage is pull toV_{DD}. When the input increases toV_{DD}, N1 and N2 is turned on while is off. Thus, the output voltage is pull down to GND.

1.2 MENTOR GRAPHICS

Today, ICs are fabricated with multimillion transistors and increasingly more metal layers as well as more routing on each layer. Their performance is determined by logic, interconnection, and other contributors.

Interconnects have become the most crucial especially, in deep and very deep submicron designs, where it can easily account for up to 90% of the global signal delay in a chip. Metal line parasitic resistances, capacitances, inductances, substrate losses from metal to ground and proximity effects, all lead to signal distortion, energy dissipation, voltage shifts, cross-talk, noise, and undesirable delays.

Mentor Graphics has developed the IC Station® Tool Suite, a complete IC design flow, from schematic capture to physical layout and verification. Thus, this software is the most suitable for ensuring immediate access to essential data and supports multiple hardware platforms that can make computing environment choices based on unique cost and performance needs. Besides, it also accurately predict the circuit performance, high performance, fast, and scalable interconnect models is necessary at all stages of the circuit analysis.

ADK3 is an ASIC Design Kit for Mentor Graphic design tools that enables a designer to prepare an IC design which qualifies to be fabricated. There are 2 main tools in ADK3:

- Design Architect IC (DA-IC)
- IC Station

II. METHODOLOGY

Design Architect-IC (DA-IC) is a full schematic capture application with a multilevel environment designed to optimize the creation of integrated circuits. DA-IC is used to create and simulate analog, RF, and mixed signal schematic designs. DA-IC provides an open architecture which allows to customize the application to fit specific needs. Fig. 3 shows the flow chart of Design Architect .
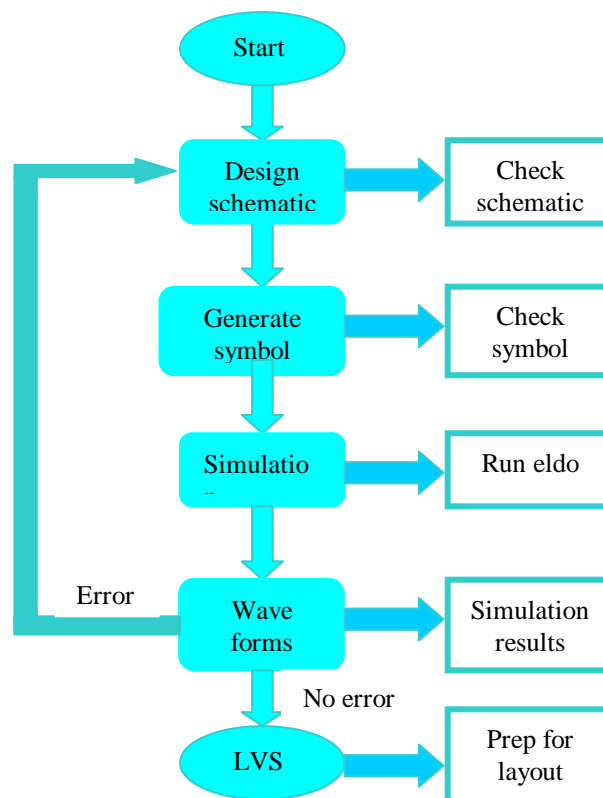

**Figure 3: Design Architect flow chart**

III. RESULTS AND DISCUSSION

Three designs (1st, 2nd and 3rd Design) are simulated with $0.18\mu m$ technologies using Mentor Graphic software. The 1st Design represent the Conventional Schmitt Trigger with the ratio of transistor is set according to [7], 2nd Design represent the Conventional Schmitt Trigger with the ratio of transistor are set similarly with the 3rd Design which is the proposed Schmitt Trigger. The respective transistor dimensions for the three designs are shown in Table 1. The comparison is made in term of propagation delay.

TABLE 1: The Transistors Dimension

$\dfrac{W}{L_{eff}}$	1st Design	2nd Design	3rd Design
P1	$\dfrac{1.44}{0.18}$	$\dfrac{1.08}{0.18}$	$\dfrac{0.54}{0.18}$
P2	$\dfrac{1.44}{0.18}$	$\dfrac{1.08}{0.18}$	$\dfrac{0.54}{0.18}$
P3	$\dfrac{0.18}{0.18}$	$\dfrac{0.54}{0.18}$	$\dfrac{0.54}{0.18}$
N1	$\dfrac{1.8}{0.18}$	$\dfrac{0.36}{0.18}$	$\dfrac{0.36}{0.18}$
N2	$\dfrac{1.8}{0.18}$	$\dfrac{0.36}{0.18}$	$\dfrac{0.36}{0.18}$
N3	$\dfrac{1.44}{0.18}$	$\dfrac{0.18}{0.18}$	$\dfrac{0.18}{0.18}$

The proposed schematic circuit is designed and checked by using Mentor Graphic software. The wire connection is connected and all the parameter such as voltage, width and effective length is settled as shown in Fig. 4. The test bench as shown in Fig. 5 is designed including the other external schematic circuit support parts. For base line, the source voltage is set to be 0.8V. The results are view as waveform to verify the performance of schematic circuit. Fig. 6-9 shows the circuit simulation result of 0.8V, 1.0V, 1.2V and 1.5V. The results show that the proposed Schmitt Trigger is successfully operated and can be used in low source voltage operation condition [8]. The compilation of the simulation results is shown in Fig. 10. The propagation delays are less in high voltage source compare to low voltage due to the transistor effective resistance and wire.
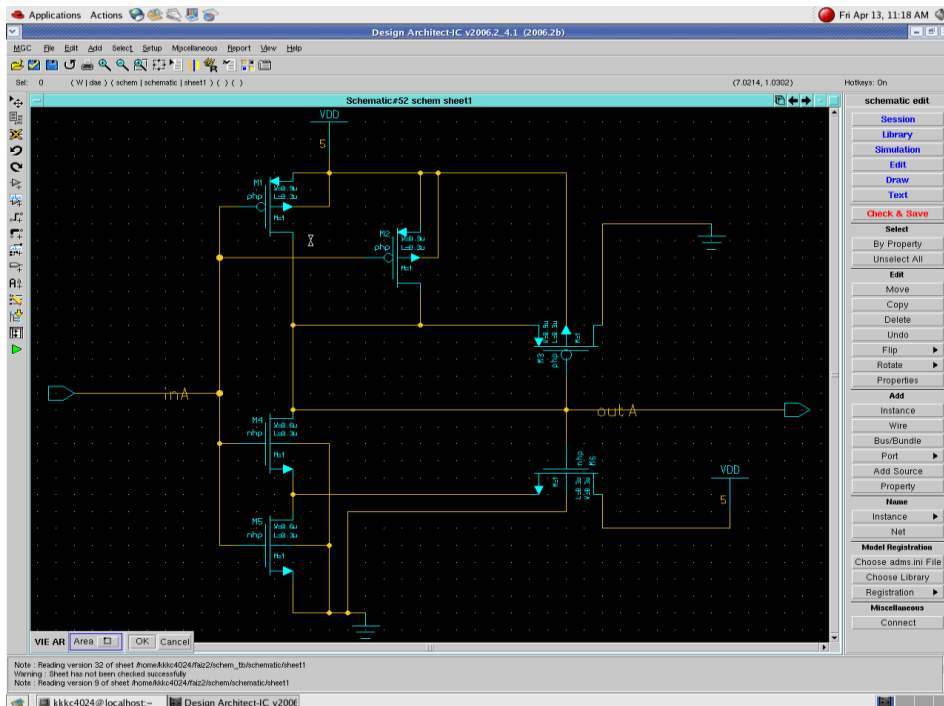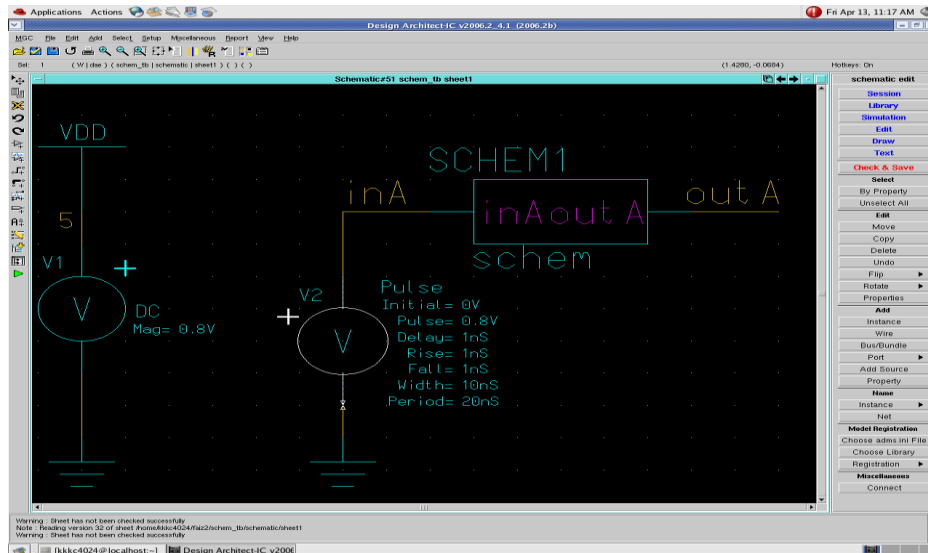

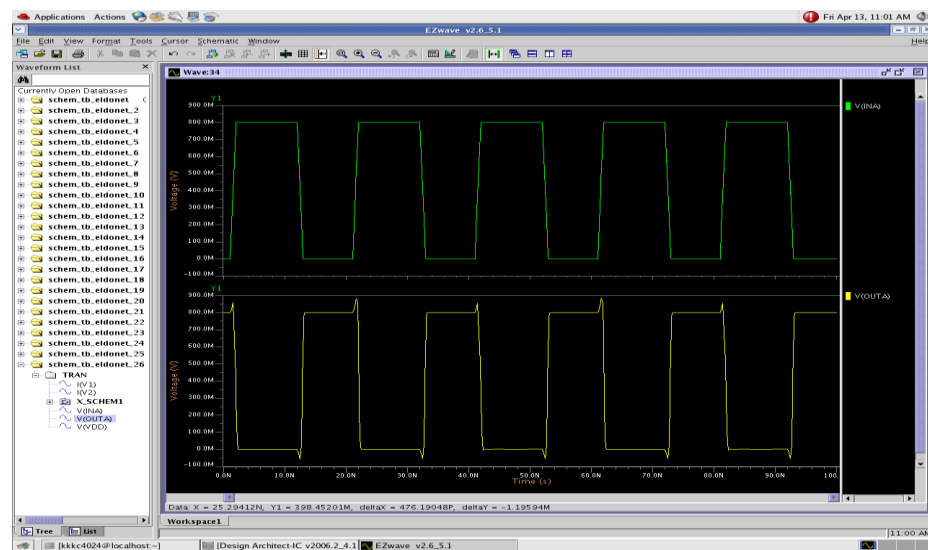**Figure 4: Schematic Circuit**

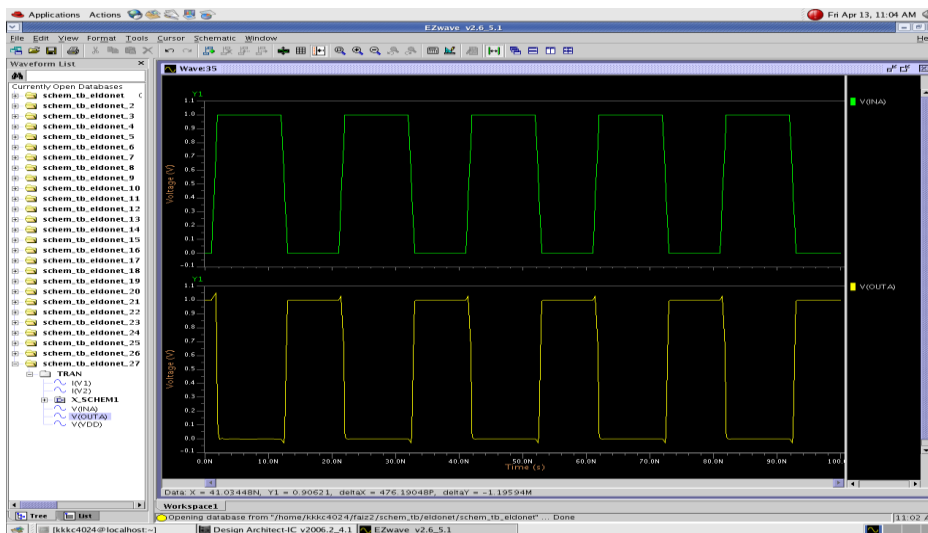**Figure 5: Test Bench**

Figure 6: Simulation result (0.8V)

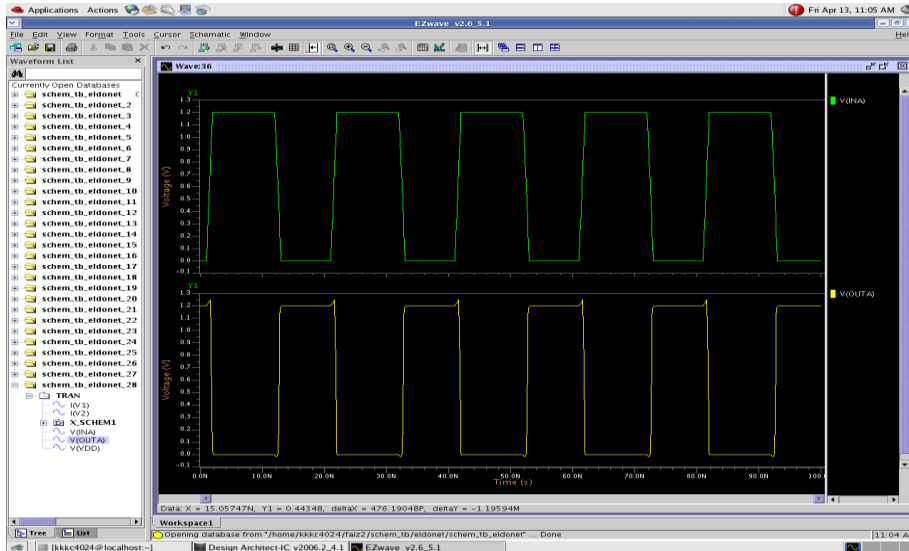**Figure 7: Simulation results (1.0V)**

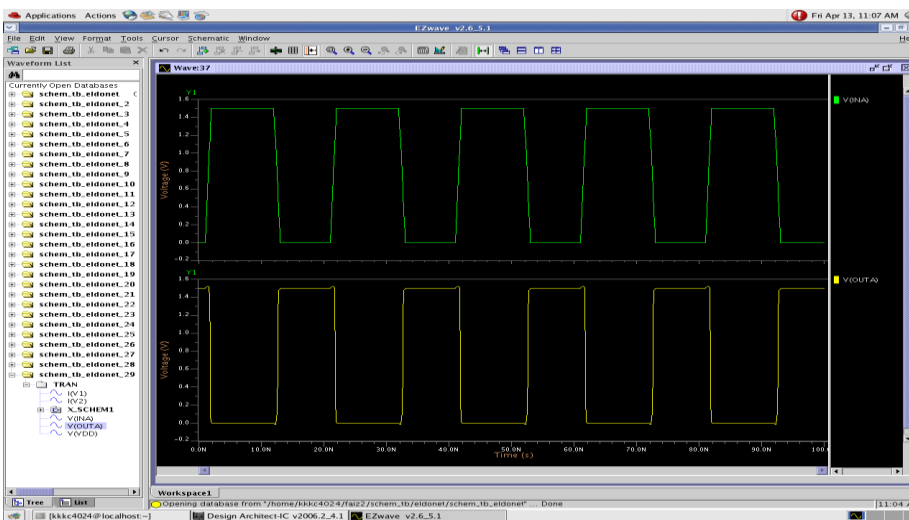**Figure 8: Simulation results (1.2V)**
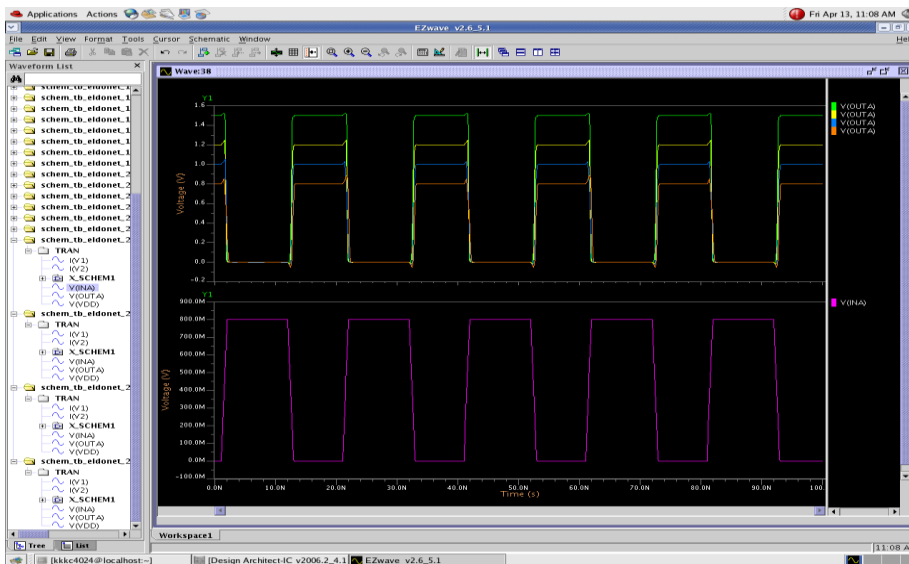

Figure 9: Simulation results (1.5V)

Figure 10: Compilation of simulation results

The comparison of the propagation delay between those designs is showed in Fig 11 [9]. These results show that the 3rd design (proposed circuit) is the best circuit in low source voltage in term of propagation delay.
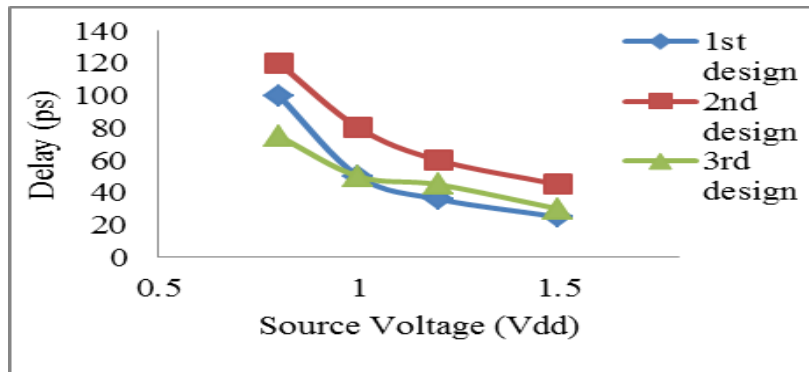

Figure 11: Comparison of Propagation Delay

Then, circuit layout is designed according to the schematic circuit that has been created before as shown in Fig. 12. Circuit stick diagram is created as a base line to design the layout. The layout is checked by using DRC (Design Rule Check). Fundamentally, these design rules represent the physical limits of the manufacturing process. Fig. 13 shows the DRC successful result. Finally both schematic circuit and layout been checked by using LVS (Layout Versus Schematic) in term of connectivity, sizing and to identify any extra component that is needed. Fig. 14 shows that the combination of both schematic circuits and layout is confirmed and exactly suitable to be sending to be manufacture in industry.
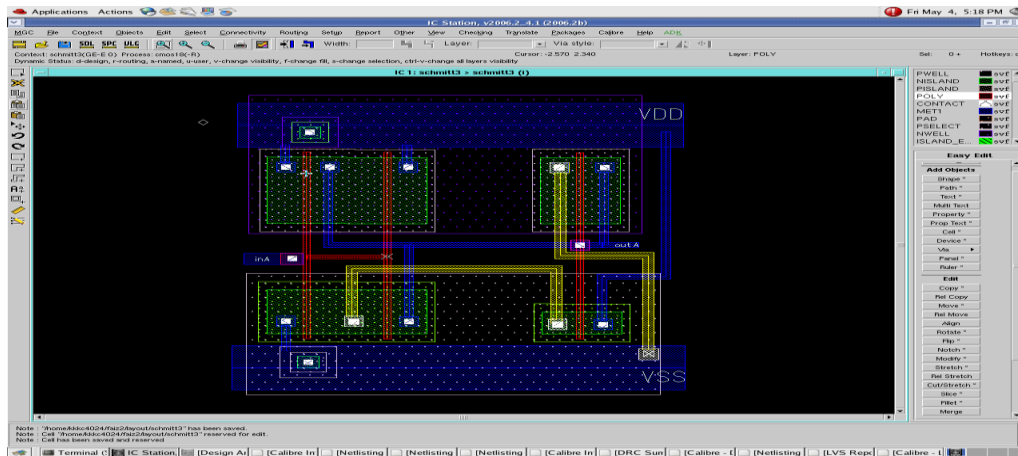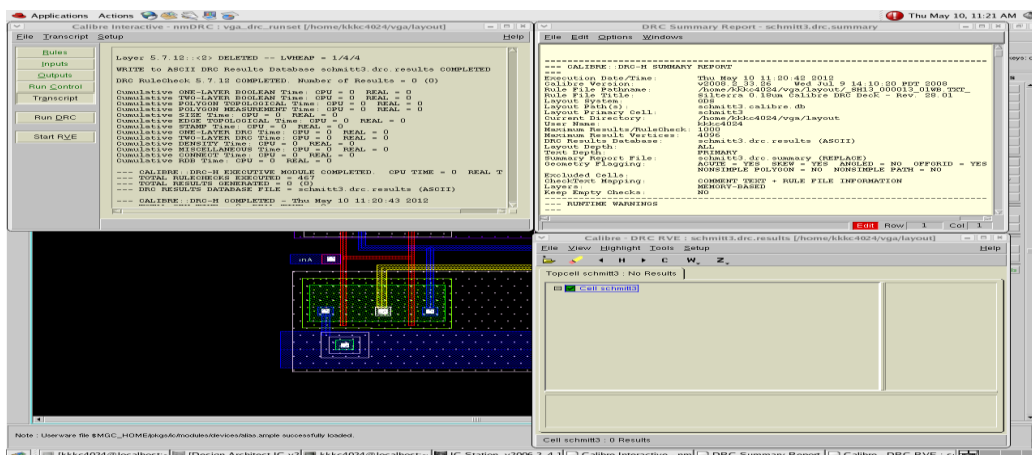

Figure 12: Circuit Layout

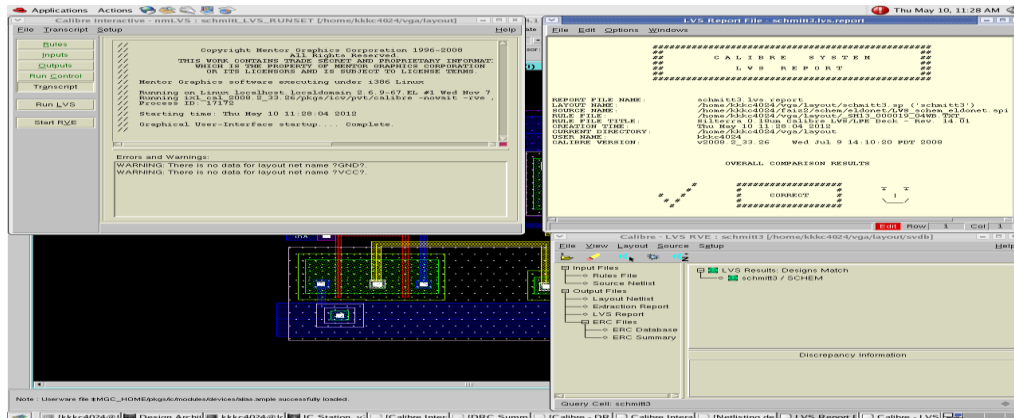**Figure 13: Layout DRC simulation results**

Figure 14: Layout LVS simulation result

IV. CONCLUSION

A new proposed CMOS Schmitt Trigger is presented which is capable to function under low voltage as much as 0.8V. The circuit gives less propagation delay compare to the conventional circuit. The proposed circuit passed the DRC (Design Rule Check) and LVS (Layout Versus Schematic) checking method. Therefore the circuit is successfully implemented and confirmed to be manufactured in the industry.

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